

# PMWD22XN

Dual N-channel  $\mu$ TrenchMOS extremely low level FET

Rev. 01 — 15 August 2005

Product data sheet

## 1. Product profile

### 1.1 General description

Dual common drain N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Low threshold voltage
- Fast switching
- Common drain

### 1.3 Applications

- Portable appliances
- Battery management

### 1.4 Quick reference data

- $V_{DS} \leq 20$  V
- $R_{DS(on)} \leq 26$  m $\Omega$
- $I_D \leq 9.2$  A
- $Q_{GD} = 2.7$  nC (typ)

## 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 8	drain (D)	<p>SOT530-1 (TSSOP8)</p>	<p>mb1600</p>
2, 3	source1 (S1)		
4	gate1 (G1)		
5	gate2 (G2)		
6, 7	source2 (S2)		

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### 3. Ordering information

**Table 2: Ordering information**

Type number	Package		
	Name	Description	Version
PMWD22XN	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1

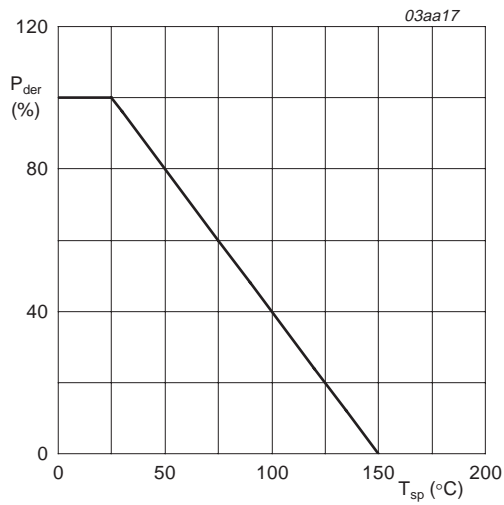
### 4. Limiting values

**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

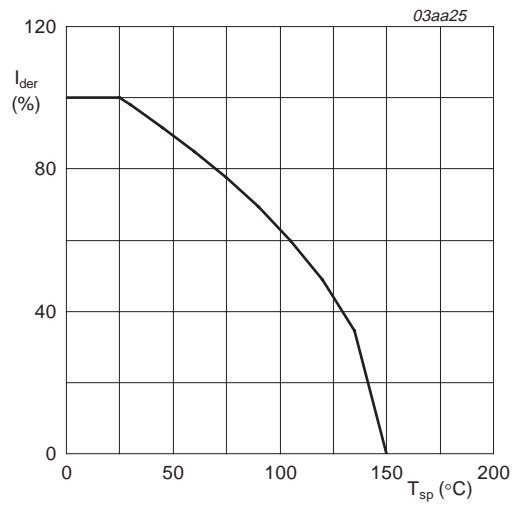
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	20	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	20	V
$V_{GS}$	gate-source voltage		-	$\pm 12$	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = 4.5\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a> <sup>[1]</sup>	-	9.2	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = 4.5\text{ V}$ ; see <a href="#">Figure 2</a> <sup>[1]</sup>	-	5.8	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a> <sup>[1]</sup>	-	37	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	3.5	W
$T_{stg}$	storage temperature		-55	+150	$^{\circ}\text{C}$
$T_j$	junction temperature		-55	+150	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 25\text{ °C}$	<sup>[1]</sup> -	2.9	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	<sup>[1]</sup> -	11.9	A

[1] Single device conducting.



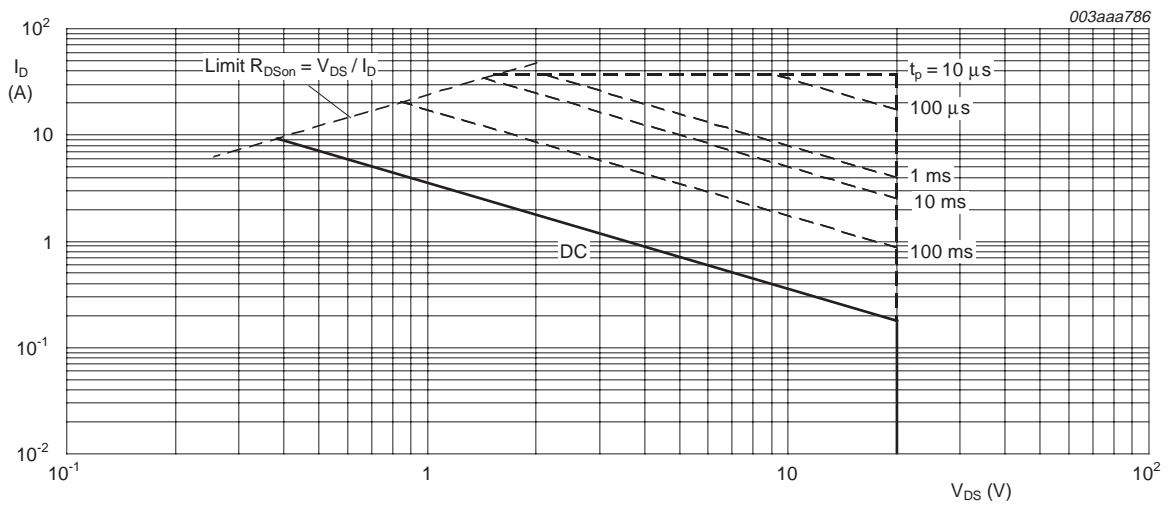
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



$T_{sp} = 25^\circ C$ ;  $I_{DM}$  is single pulse;  $V_{GS} = 4.5 V$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	35	K/W

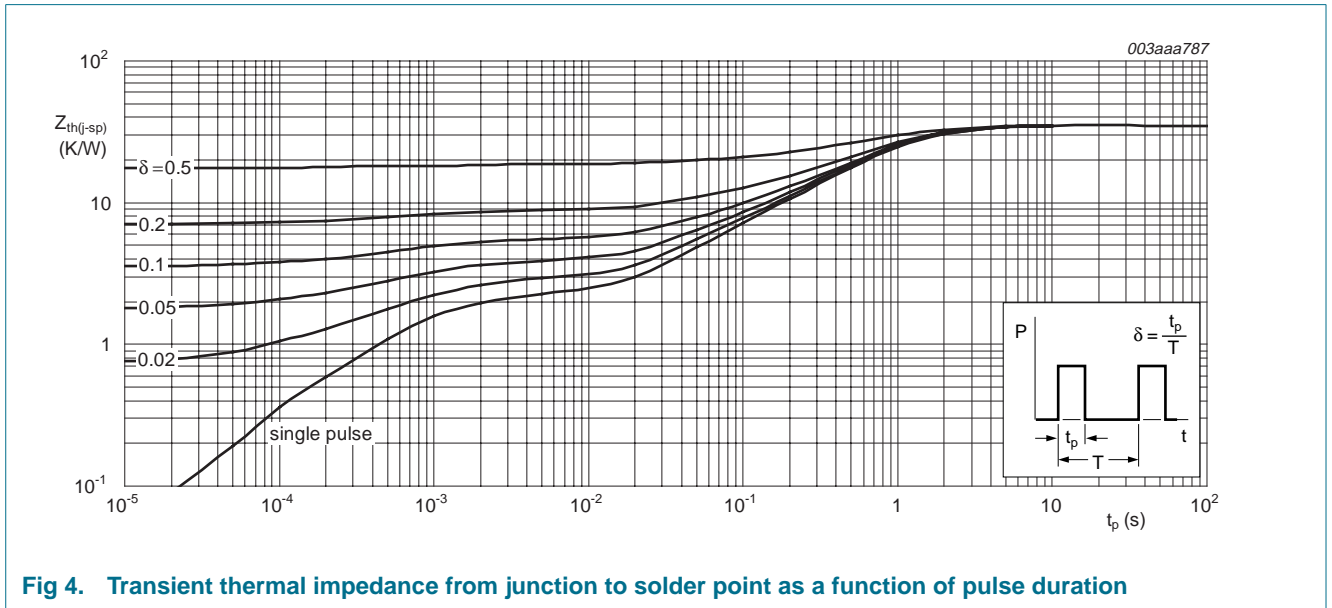
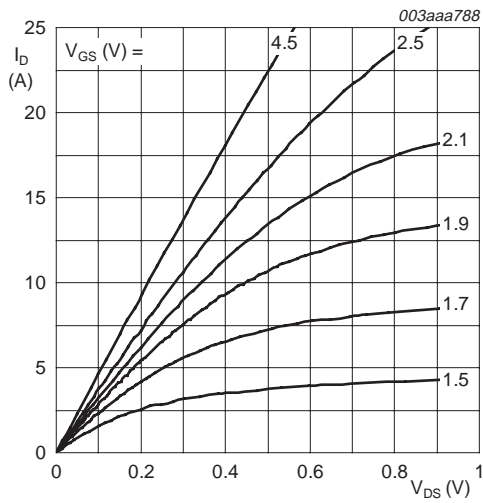


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

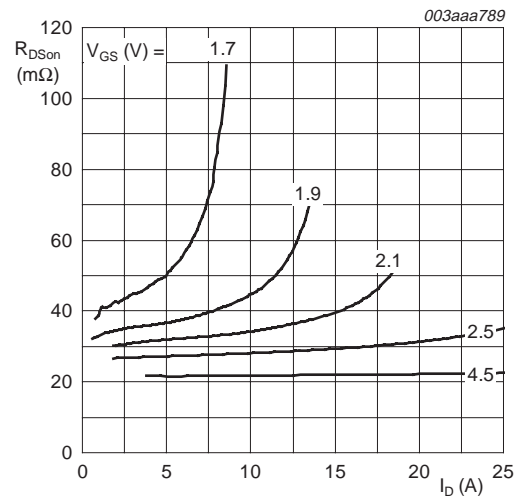
**Table 5: Characteristics**
 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	20	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>				
		$T_j = 25\text{ }^\circ\text{C}$	0.5	1	1.5	V
		$T_j = 150\text{ }^\circ\text{C}$	0.35	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	-	-	1.8	V
$I_{DSS}$	drain leakage current	$V_{DS} = 20\text{ V}$ ; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$T_j = 150\text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 12\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	100	nA
$R_G$	gate resistance	$f = 1\text{ MHz}$	-	1.3	-	$\Omega$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 4\text{ A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>				
		$T_j = 25\text{ }^\circ\text{C}$	-	21	26	m $\Omega$
		$T_j = 150\text{ }^\circ\text{C}$	-	35.7	42	m $\Omega$
		$V_{GS} = 2.5\text{ V}$ ; $I_D = 3\text{ A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	27	35	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 4.2\text{ A}$ ; see <a href="#">Figure 8</a>	-	19	24	m $\Omega$
$R_{S1S2(on)}$	source1-source2 on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 4\text{ A}$	-	36	-	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 4\text{ A}$ ; $V_{DS} = 10\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; see <a href="#">Figure 11</a>	-	8.4	-	nC
$Q_{GS}$	gate-source charge		-	1.35	-	nC
$Q_{GD}$	gate-drain charge		-	2.7	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 16\text{ V}$ ; $f = 1\text{ MHz}$ ; see <a href="#">Figure 13</a>	-	535	-	pF
$C_{oss}$	output capacitance		-	185	-	pF
$C_{rss}$	reverse transfer capacitance		-	110	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10\text{ V}$ ; $R_L = 10\text{ }\Omega$ ; $V_{GS} = 4.5\text{ V}$ ; $R_G = 6\text{ }\Omega$	-	11	-	ns
$t_r$	rise time		-	19	-	ns
$t_{d(off)}$	turn-off delay time		-	30	-	ns
$t_f$	fall time		-	23	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 2\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; see <a href="#">Figure 12</a>	-	0.75	1.2	V



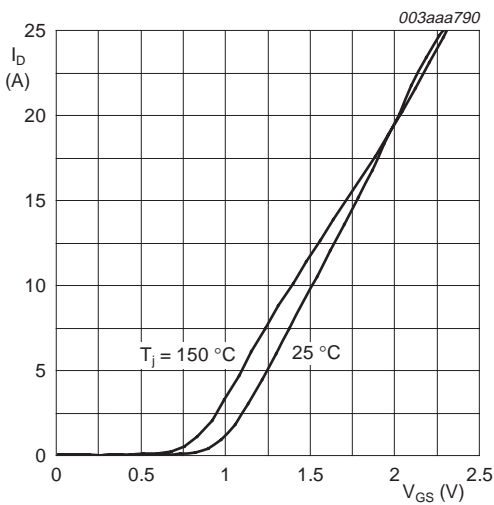
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



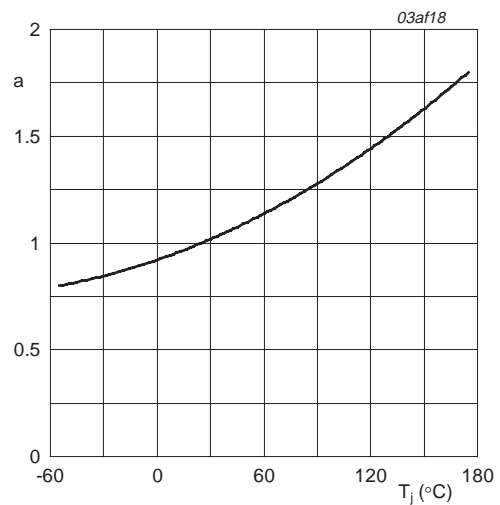
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



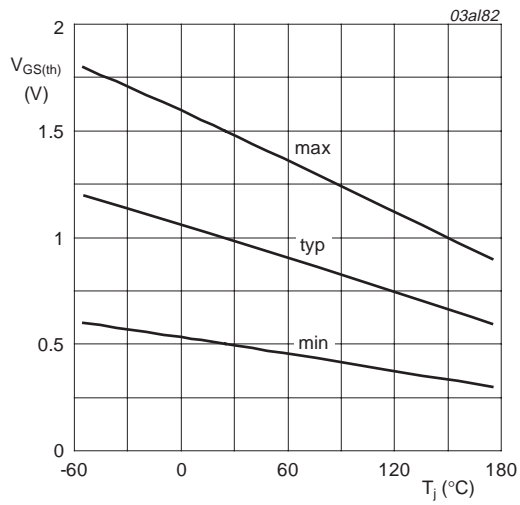
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



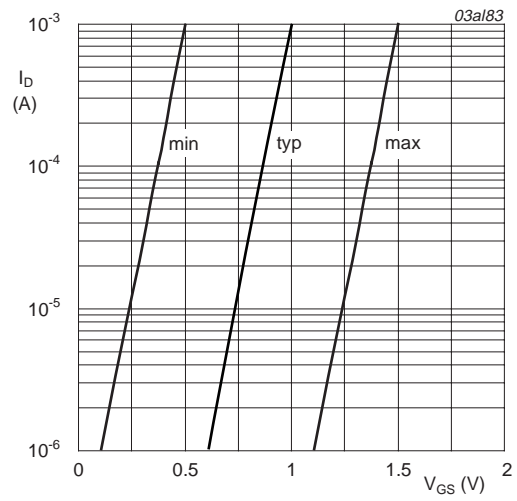
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



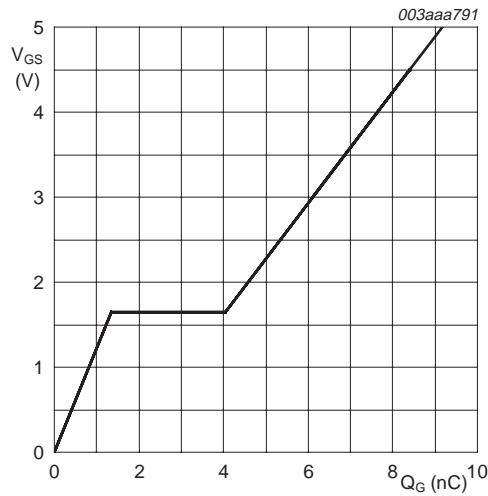
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig. 9. Gate-source threshold voltage as a function of junction temperature



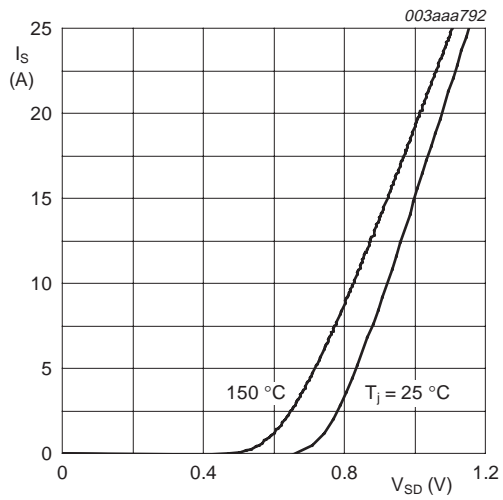
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



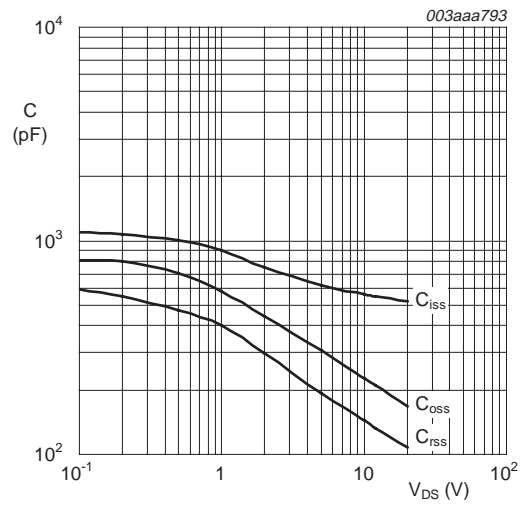
$I_D = 4 \text{ A}; V_{DS} = 10 \text{ V}$

Fig. 11. Gate-source voltage as a function of gate charge; typical values



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm

SOT530-1

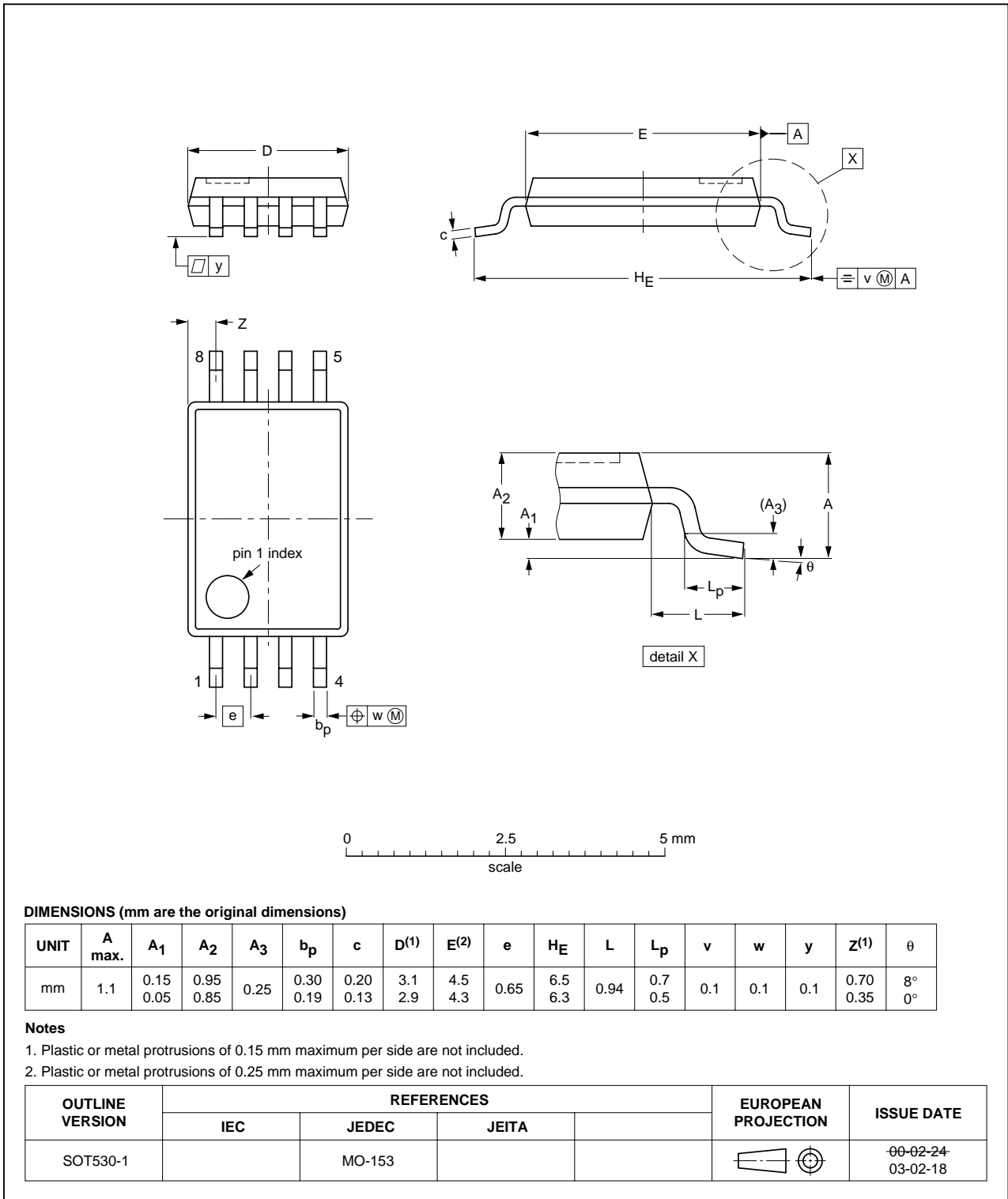


Fig 14. Package outline SOT530-1 (TSSOP8)

## 8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMWD22XN_1	20050815	Product data sheet	-	9397 750 15093	-

## 9. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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## 14. Contents

<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	General description .....	1
1.2	Features .....	1
1.3	Applications .....	1
1.4	Quick reference data .....	1
<b>2</b>	<b>Pinning information</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Limiting values</b> .....	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> .....	<b>4</b>
<b>6</b>	<b>Characteristics</b> .....	<b>5</b>
<b>7</b>	<b>Package outline</b> .....	<b>9</b>
<b>8</b>	<b>Revision history</b> .....	<b>10</b>
<b>9</b>	<b>Data sheet status</b> .....	<b>11</b>
<b>10</b>	<b>Definitions</b> .....	<b>11</b>
<b>11</b>	<b>Disclaimers</b> .....	<b>11</b>
<b>12</b>	<b>Trademarks</b> .....	<b>11</b>
<b>13</b>	<b>Contact information</b> .....	<b>11</b>



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