

PMWD26UN

Dual N-channel μ TrenchMOS ultra low level FET

Rev. 02 — 19 May 2005

Product data sheet

1. Product profile

1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Surface-mounted package
- Very low threshold voltage
- Low profile
- Fast switching

1.3 Applications

- Portable appliances
- Battery management
- PCMCIA cards
- Load switching

1.4 Quick reference data

- $V_{DS} \leq 20 \text{ V}$
- $P_{tot} \leq 3.1 \text{ W}$
- $I_D \leq 7.8 \text{ A}$
- $R_{DS(on)} \leq 30 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1	drain1 (D1)	SOT530-1 ((TSSOP8))	msd901
2, 3	source1 (S1)		
4	gate1 (G1)		
5	gate2 (G2)		
6, 7	source2 (S2)		
8	drain2 (D2)		

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3. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
PMWD26UN	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage		-	± 10	V
I_D	drain current (DC)	$T_{sp} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 4.5\text{ V}$; Figure 2 and 3	[1] -	7.8	A
		$T_{sp} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 4.5\text{ V}$; Figure 2	[1] -	4.7	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	[1] -	31.3	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$; Figure 1	[1] -	3.1	W
T_{stg}	storage temperature		-55	+150	$^{\circ}\text{C}$
T_j	junction temperature		-55	+150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	2.6	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	10.3	A

[1] Single device conducting.

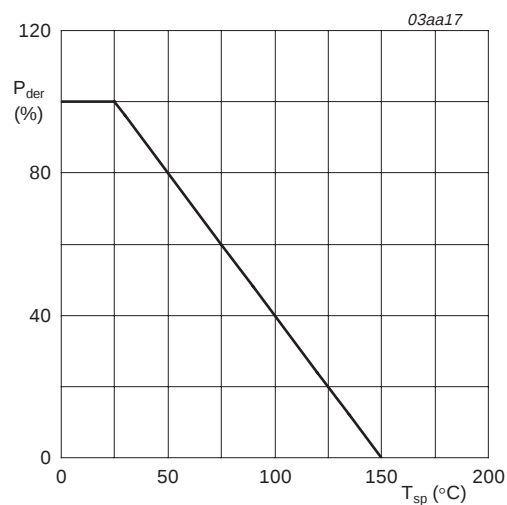


Fig 1. Normalized total power dissipation as a function of solder point temperature

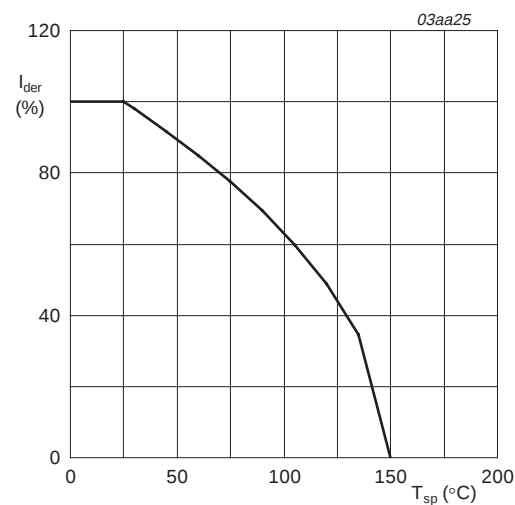


Fig 2. Normalized continuous drain current as a function of solder point temperature

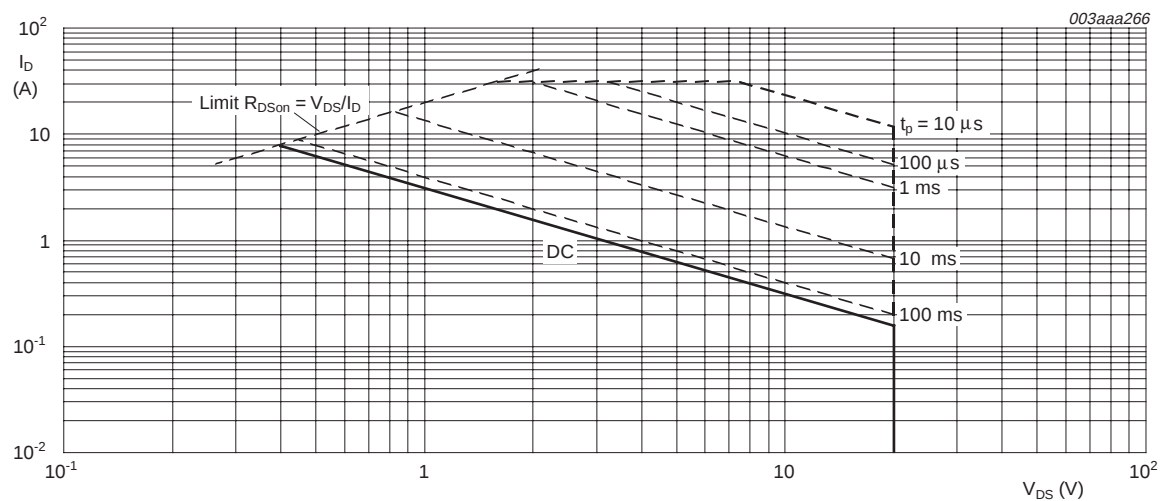


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	40	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	100	-	K/W

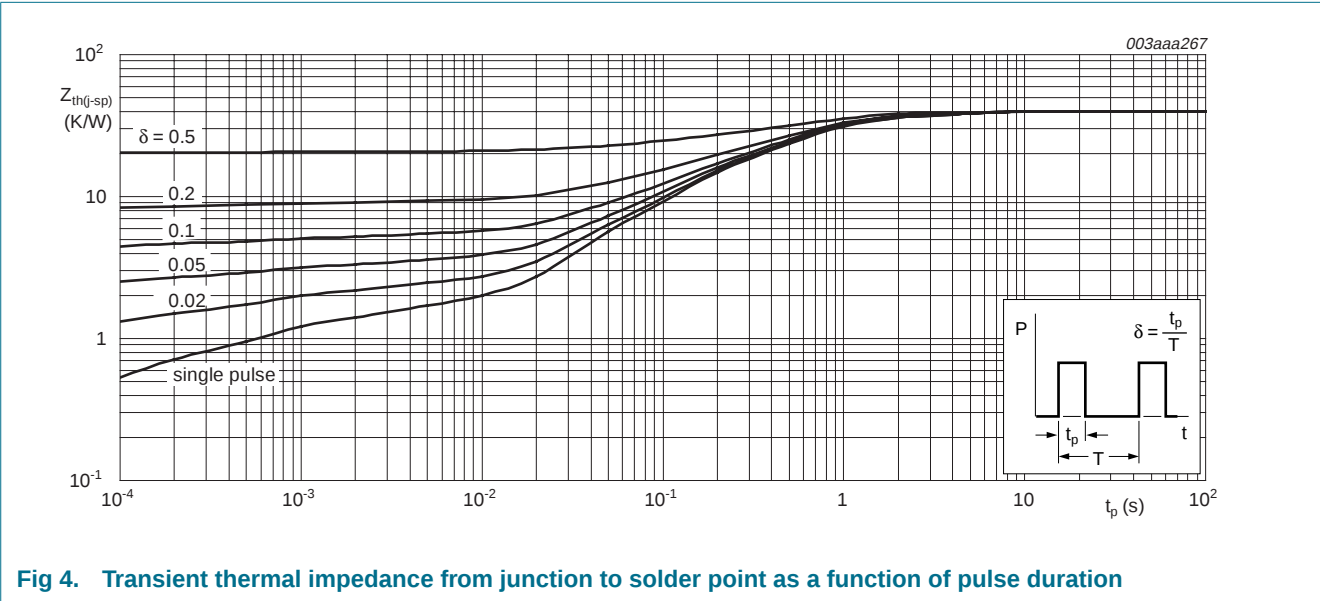


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics
 $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	20	-	-	V
		$T_j = -55\text{ }^{\circ}\text{C}$	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9 and 10	0.45	0.7	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 20\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^{\circ}\text{C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 3.5\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ }^{\circ}\text{C}$	-	26	30	m Ω
		$T_j = 150\text{ }^{\circ}\text{C}$	-	44	51	m Ω
		$V_{GS} = 1.8\text{ V}$; $I_D = 3.5\text{ A}$; Figure 7 and 8	-	34	40	m Ω
		$V_{GS} = 2.5\text{ V}$; $I_D = 3.5\text{ A}$; Figure 7 and 8	-	29	35	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 4\text{ A}$; $V_{DS} = 16\text{ V}$; $V_{GS} = 4.5\text{ V}$; Figure 13	-	23.6	-	nC
Q_{gs}	gate-source charge		-	2.1	-	nC
Q_{gd}	gate-drain (Miller) charge		-	6.7	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 16\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	1366	-	pF
C_{oss}	output capacitance		-	399	-	pF
C_{rss}	reverse transfer capacitance		-	239	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10\text{ V}$; $R_L = 1\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	14	-	ns
t_r	rise time		-	22	-	ns
$t_{d(off)}$	turn-off delay time		-	56	-	ns
t_f	fall time		-	33	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 4\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.67	1.2	V
t_{rr}	reverse recovery time	$I_S = 4\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	45	-	ns
Q_r	recovered charge	$V_R = 20\text{ V}$	-	13	-	nC

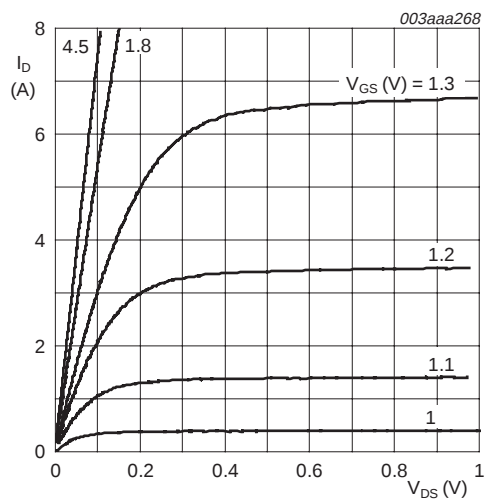


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

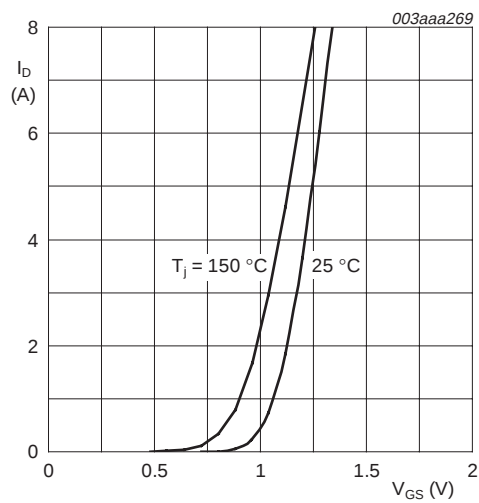


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

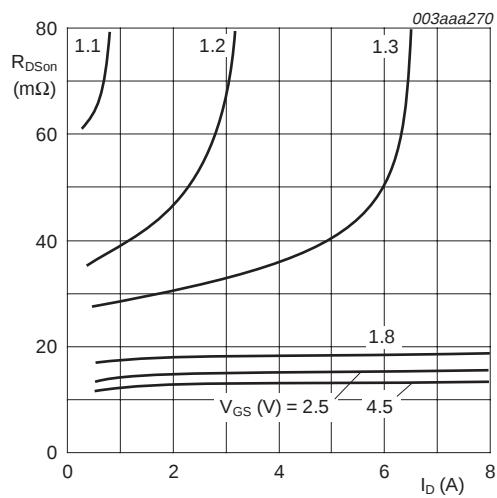


Fig 7. Drain-source on-state resistance as a function of drain current; typical values

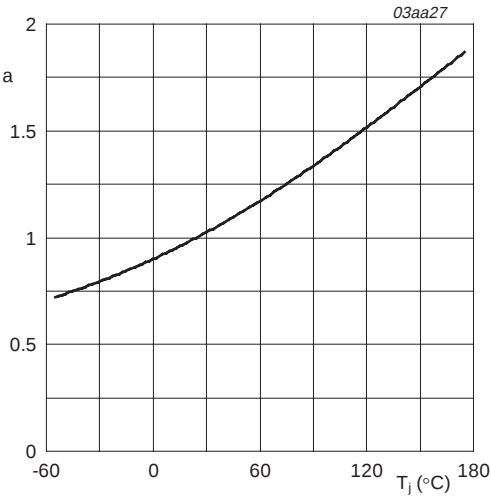
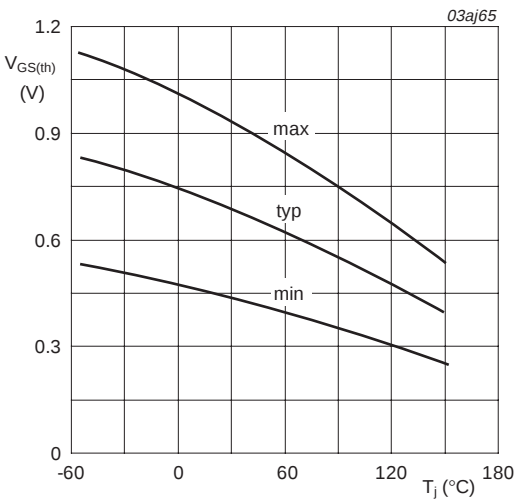
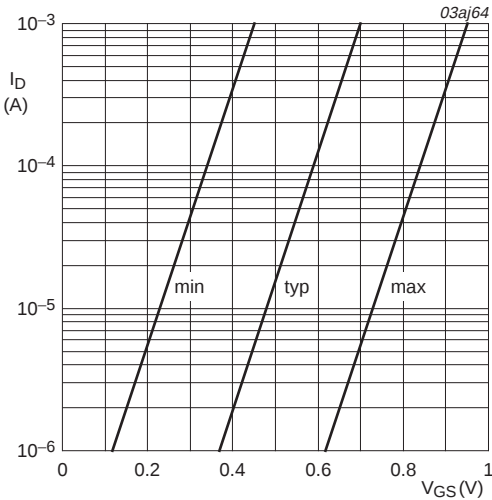


Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



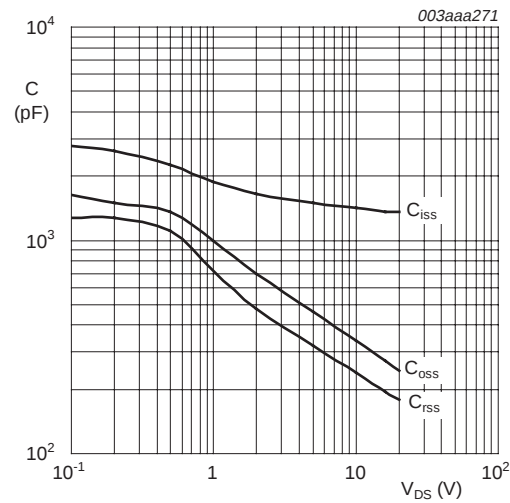
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



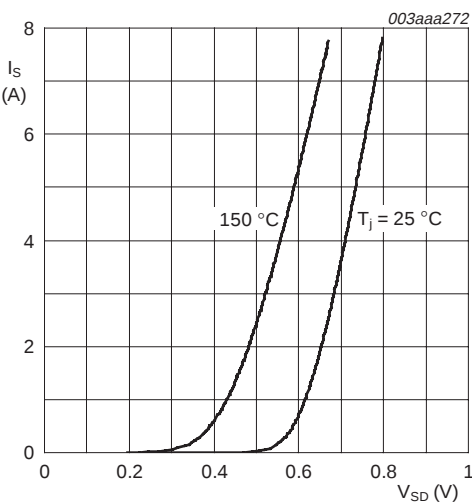
$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



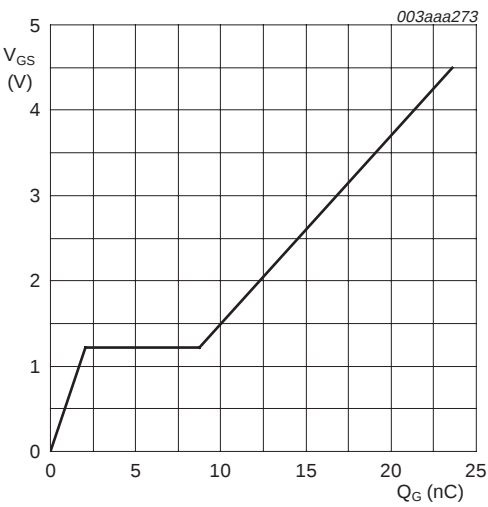
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_J = 25 \text{ }^\circ\text{C} \text{ and } 150 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



I_D = 4 A; V_{DD} = 16 V

Fig 13. Gate-source voltage as a function of gate charge; typical values

7. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm

SOT530-1

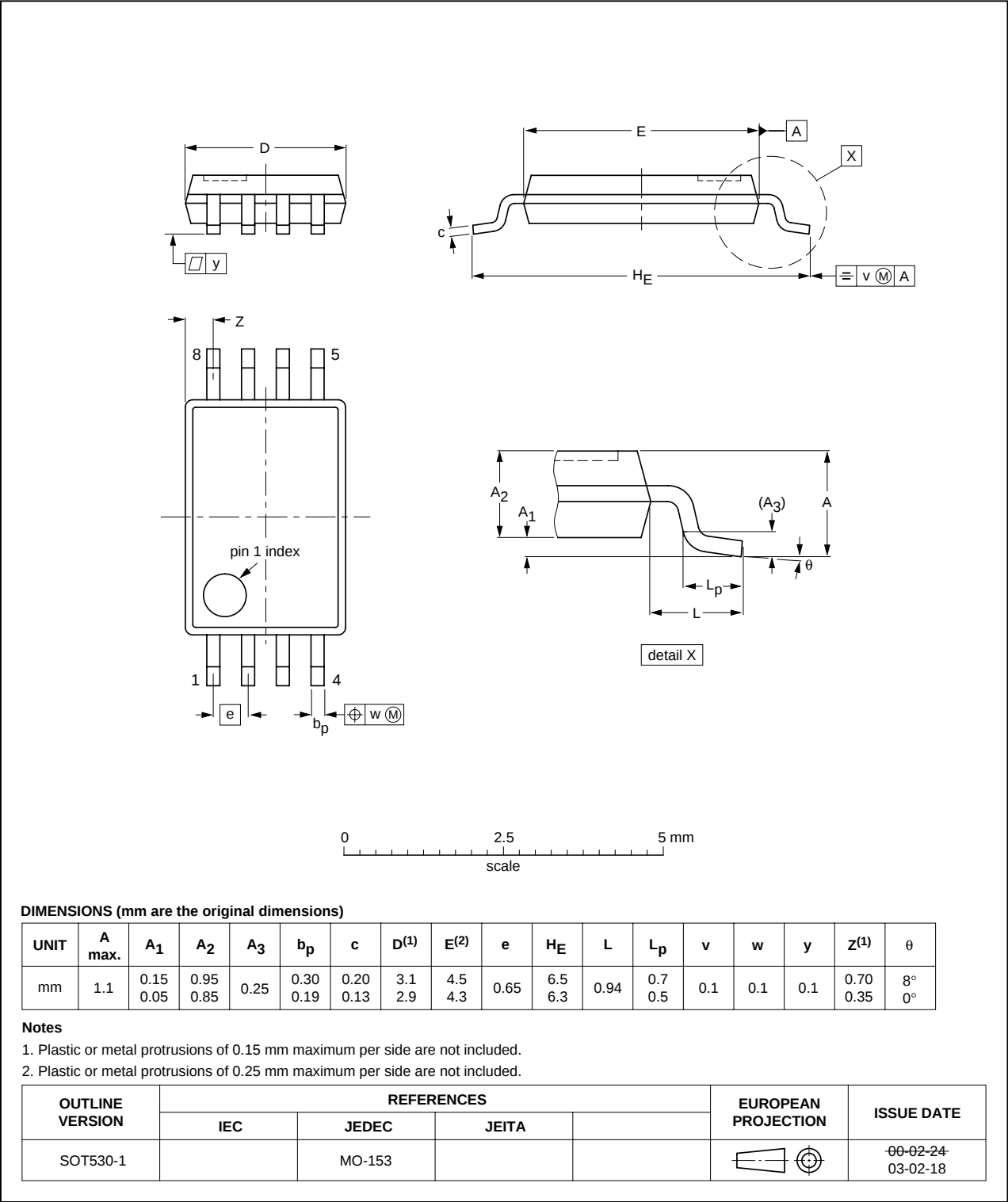


Fig 14. Package outline SOT530-1 (TSSOP8)

8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMWD26UN_2	20050519	Product data sheet	-	9397 750 14982	PMWD26UN-01
Modifications:					
- The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. P_{tot} and I_D data revised in Section 1.4 "Quick reference data" Section 3 "Ordering information" added P_{tot}, I_D, I_S, I_{DM} and I_{SM} data revised in Table 3 "Limiting values" $R_{th(j-sp)}$ data revised in Table 4 "Thermal characteristics" Figure 3, 4, 5, 6, 7 and 12 revised.					
PMWD26UN-01	20030122	Product data	-	9397 750 10834	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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