PMXB350UPE

20 V, P-channel Trench MOSFET

19 September 2013 **Product data sheet**

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: 1.1 × 1.0 × 0.37 mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1 kV HBM
- Drain-source on-state resistance R_{DSon} = 100 mΩ

3. Applications

- High-side load switch and charging switch for portable devices
- Power management in battery driven portables
- LED driver
- DC-to-DC converter

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	-20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-	-1.2	A
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -1.2 A; T_j = 25 °C		-	350	447	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

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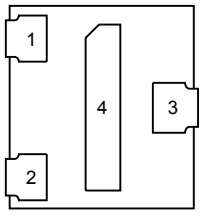
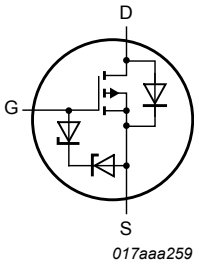
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view **DFN1010D-3 (SOT1215)**	
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB350UPE	DFN1010D-3	plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB350UPE	11 10 00

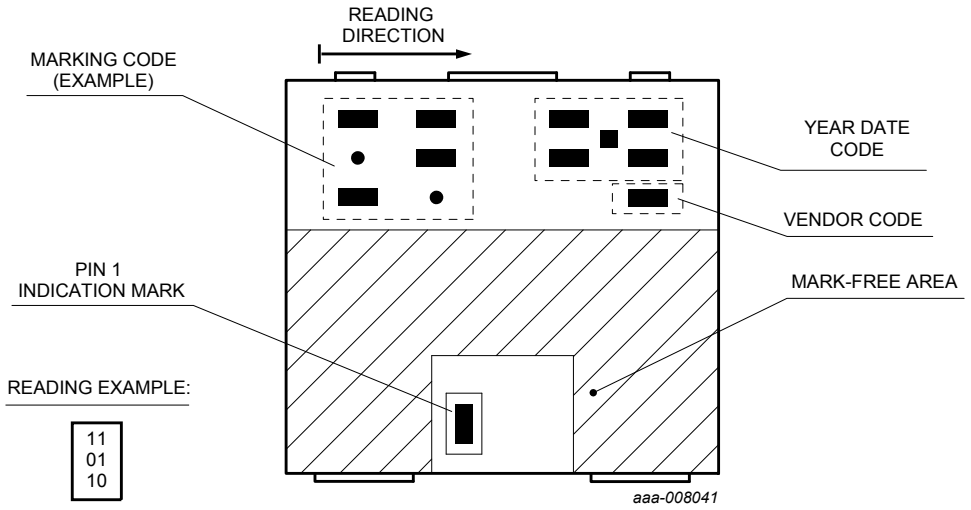


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = -4.5 V; T_{amb} = 25 °C	[1]	-	-1.2	A
		V_{GS} = -4.5 V; T_{amb} = 100 °C	[1]	-	-1	A
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; $t_p \leq 10$ µs		-	-5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	360	mW
			[1]	-	930	mW
		T_{sp} = 25 °C		-	5680	mW
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	-0.9	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

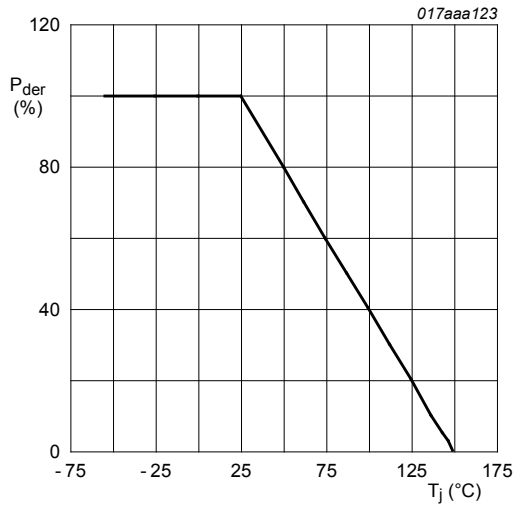

Fig. 2. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

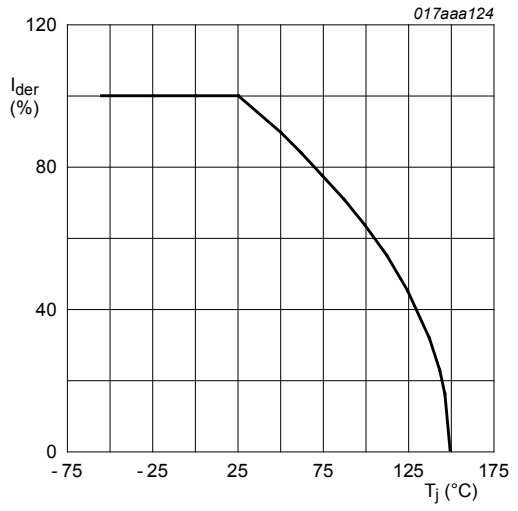

Fig. 3. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

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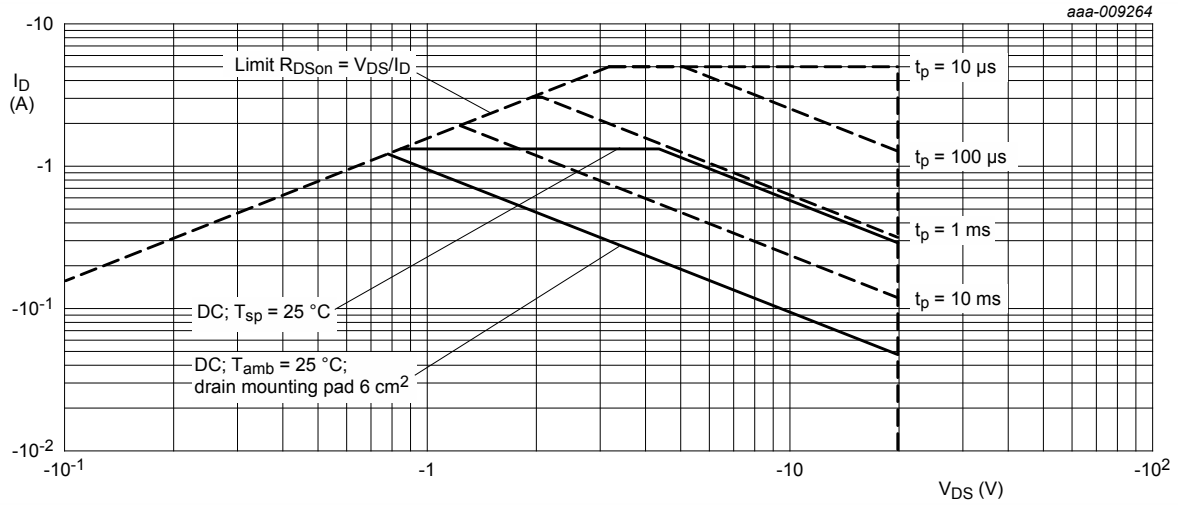

I_{DM} = single pulse

Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	303	348	K/W
			[2]	-	116	134	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	17	22	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2.

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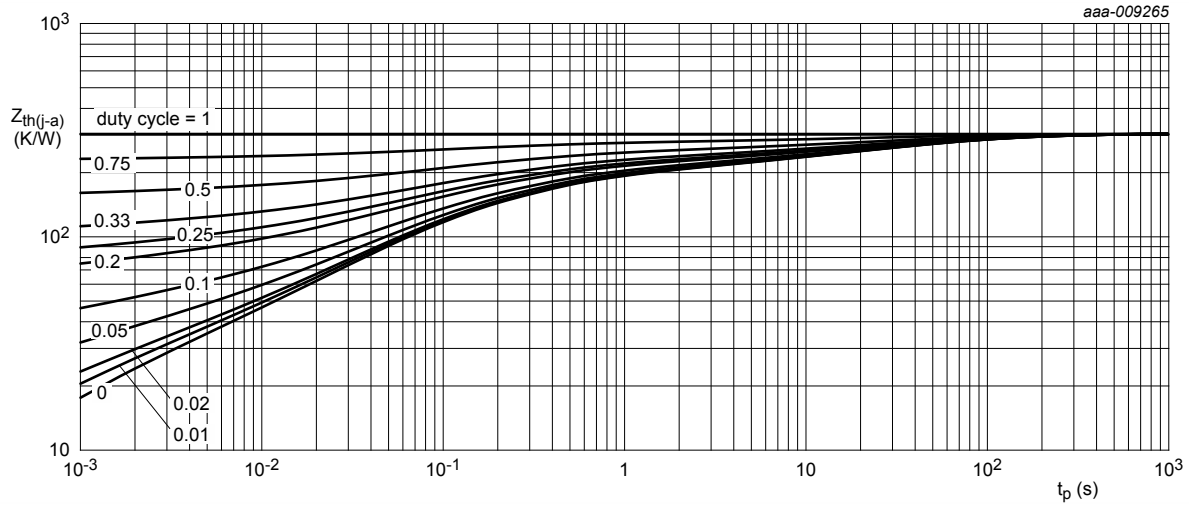
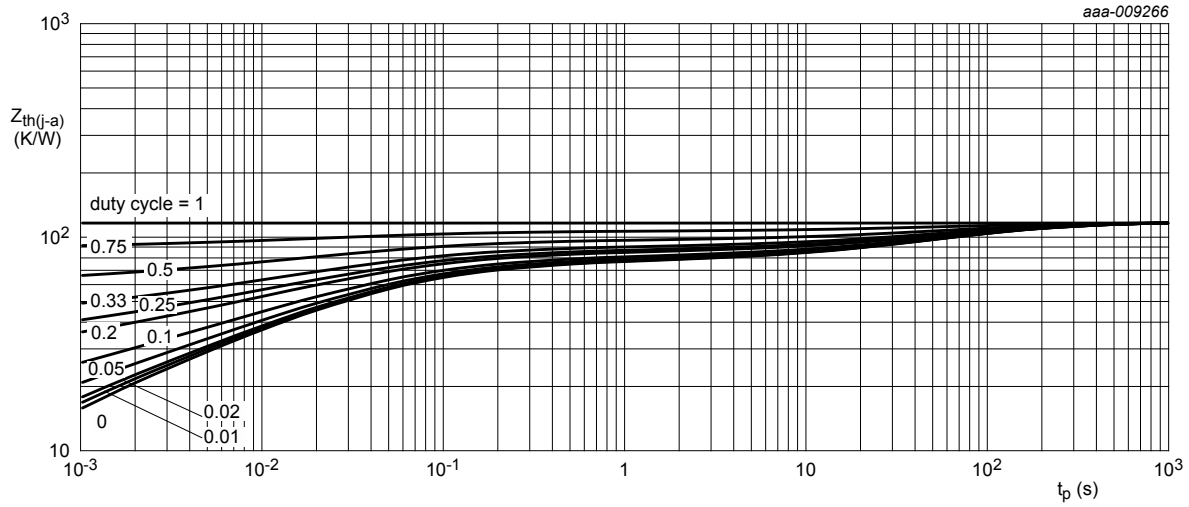


FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm^2

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = -250 µA; V_{GS} = 0 V; T_j = 25 °C		-20	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = -250 µA; V_{DS} = V_{GS}; T_j = 25 °C		-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 °C		-	-	-1	µA
I_{GSS}	gate leakage current	V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-10	µA
		V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	10	µA
R_{DSon}	drain-source on-state resistance	V_{GS} = -4.5 V; I_D = -1.2 A; T_j = 25 °C		-	350	447	mΩ
		V_{GS} = -4.5 V; I_D = -1.2 A; T_j = 150 °C		-	508	650	mΩ
		V_{GS} = -2.5 V; I_D = -1 A; T_j = 25 °C		-	450	645	mΩ
		V_{GS} = -1.8 V; I_D = -0.4 A; T_j = 25 °C		-	600	940	mΩ
		V_{GS} = -1.5 V; I_D = -10 mA; T_j = 25 °C		-	760	2000	mΩ
		V_{GS} = -1.2 V; I_D = -1 mA; T_j = 25 °C		-	1200	-	mΩ
g_{fs}	forward transconductance	V_{DS} = -5 V; I_D = -1.2 A; T_j = 25 °C		-	5.2	-	S
R_G	gate resistance	f = 1 MHz		-	0.8	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = -10 V; I_D = -1.2 A; V_{GS} = -4.5 V; T_j = 25 °C		-	1.25	2.3	nC
Q_{GS}	gate-source charge			-	0.27	-	nC
Q_{GD}	gate-drain charge			-	0.28	-	nC
C_{iss}	input capacitance	V_{DS} = -10 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	116	-	pF
C_{oss}	output capacitance			-	16.5	-	pF
C_{rss}	reverse transfer capacitance			-	12.2	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = -10 V; I_D = -1.2 A; V_{GS} = -4.5 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	3	-	ns
t_r	rise time			-	9	-	ns
$t_{d(off)}$	turn-off delay time			-	18	-	ns
t_f	fall time			-	6	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = -0.9 A; V_{GS} = 0 V; T_j = 25 °C		-	-0.8	-1.2	V

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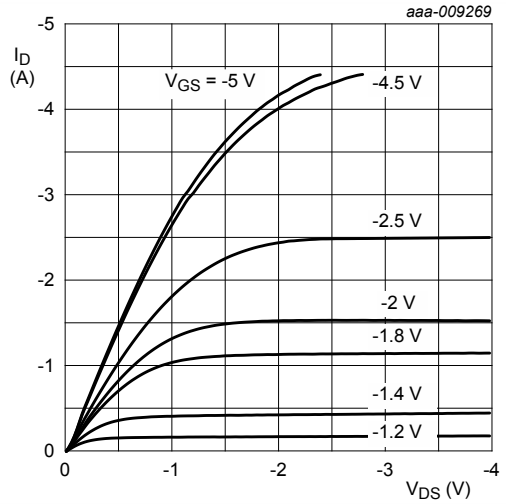
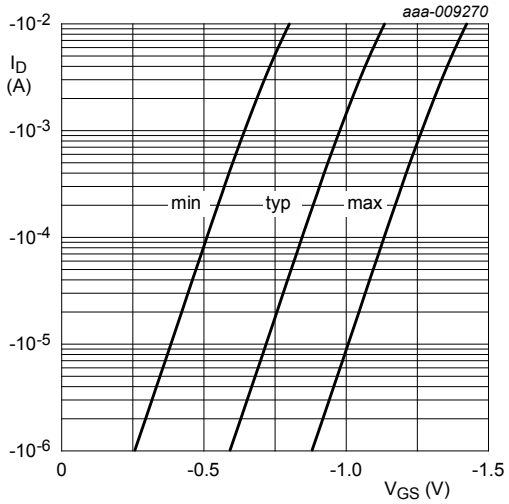


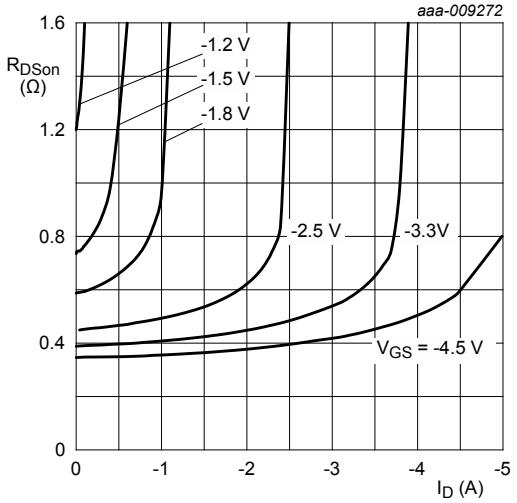
T_j = 25 °C

Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



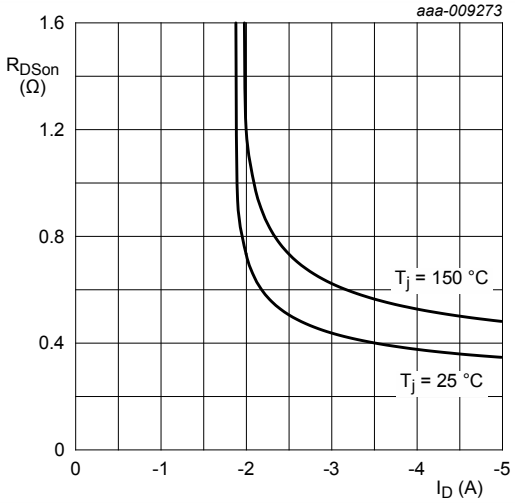
T_j = 25 °C; V_{DS} = -5 V

Fig. 8. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



I_D = -1.2 A

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

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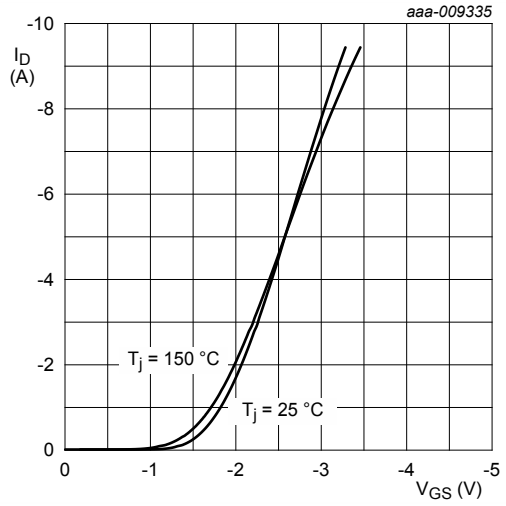


$V_{DS} > I_D \times R_{DSon}$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

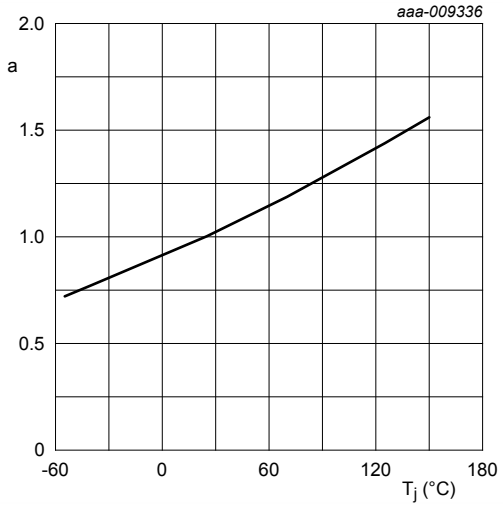
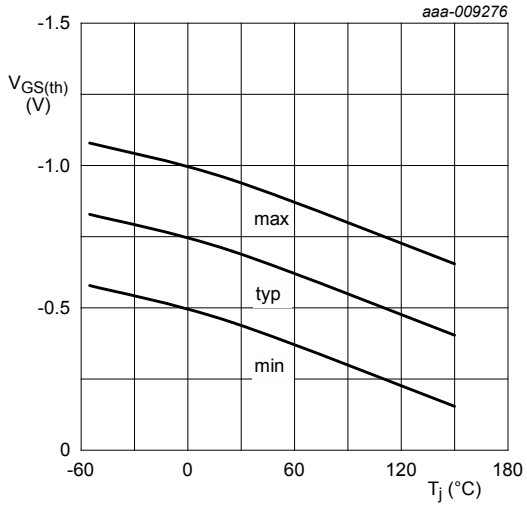


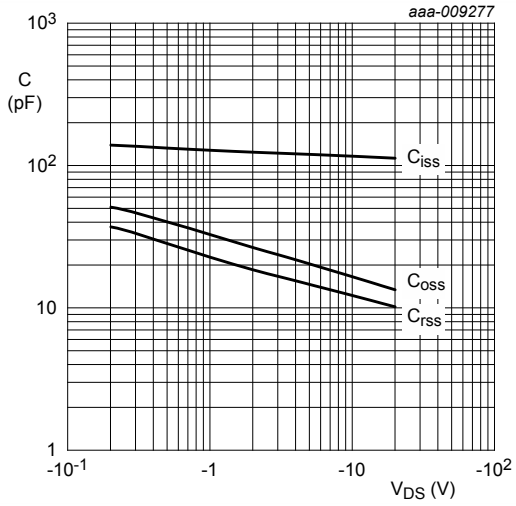
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$



I_D = -0.25 mA; $V_{DS} = V_{GS}$

Fig. 13. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

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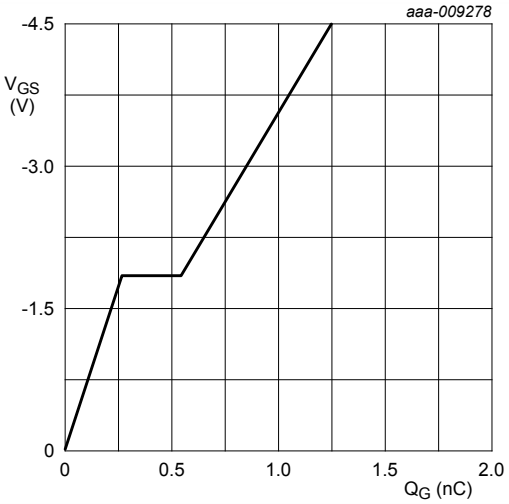


I_D = -1.2 A; V_{DS} = -10 V; T_{amb} = 25 °C

Fig. 15. Gate-source voltage as a function of gate charge; typical values

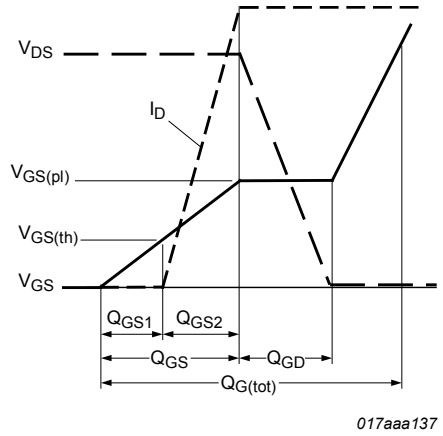
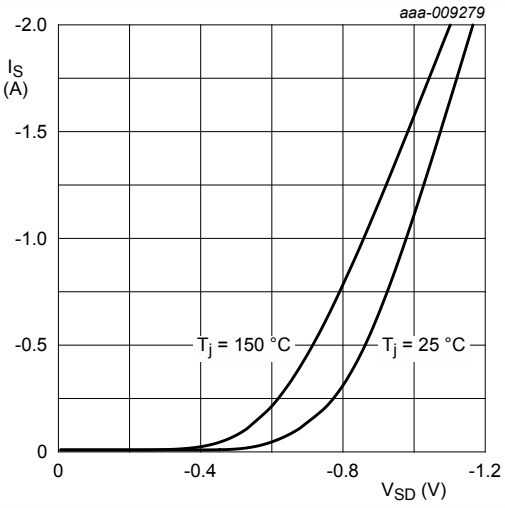


Fig. 16. MOSFET transistor: Gate charge waveform definitions



V_{GS} = 0 V

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

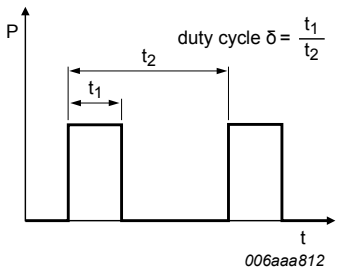


Fig. 18. Duty cycle definition

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12. Package outline

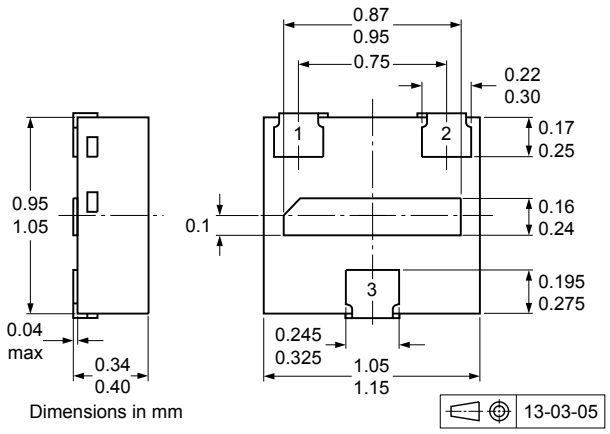

Fig. 19. Package outline DFN1010D-3 (SOT1215)

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13. Soldering

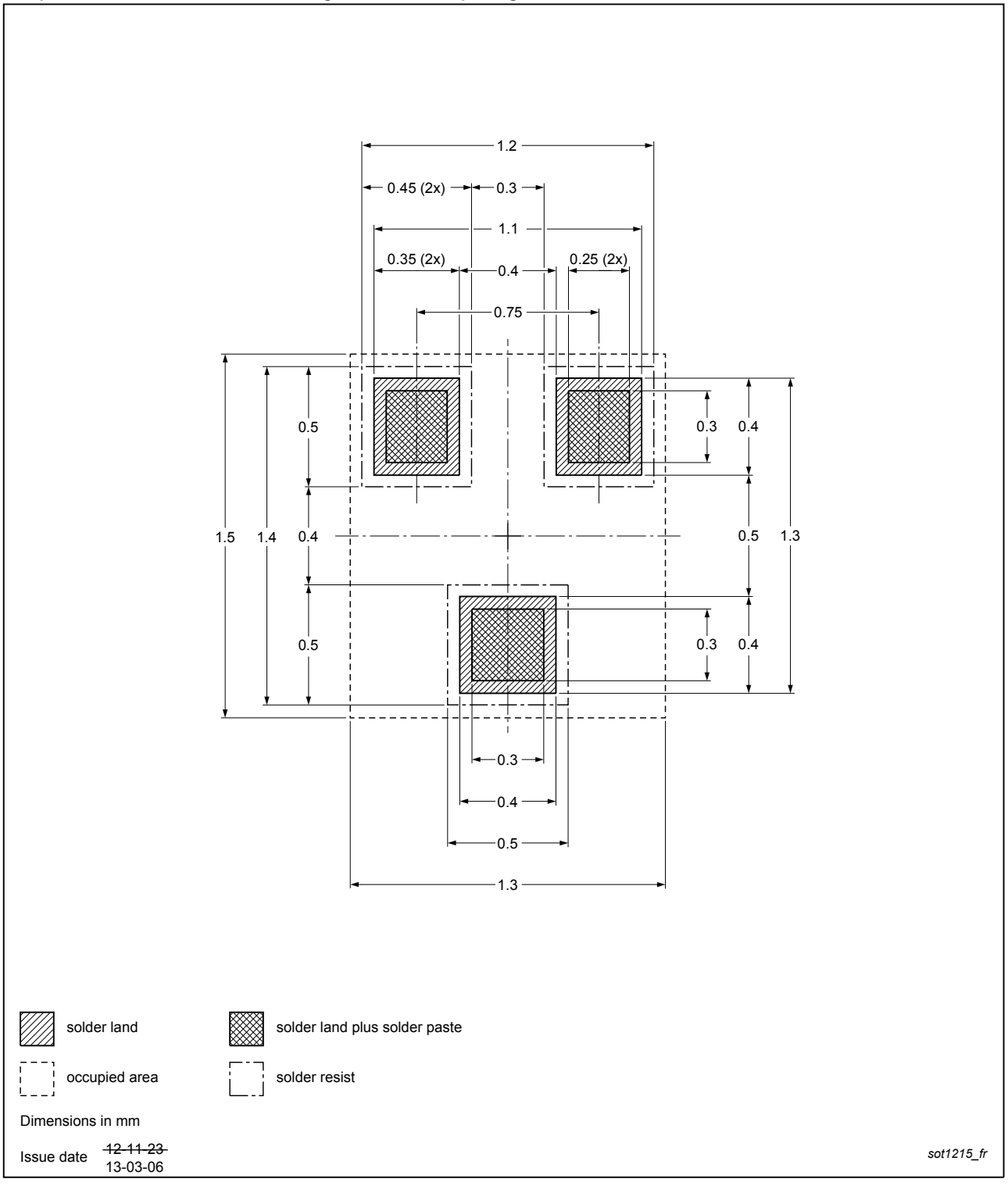

Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

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14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB350UPE v.1	20130919	Product data sheet	-	-

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15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
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