



# PMXB40UNE

12 V, N-channel Trench MOSFET

27 September 2013

Product data sheet

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and thin SMD plastic package:  $1.1 \times 1.0 \times 0.37$  mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1 kV
- Very low Drain-Source on-state resistance  $R_{DSon} = 34$  m $\Omega$
- Very low threshold voltage of 0.65 V for portable applications

## 3. Applications

- Low-side load switch and charging switch for portable devices
- Power management in battery-driven portables
- LED driver
- DC-to-DC converters

## 4. Quick reference data

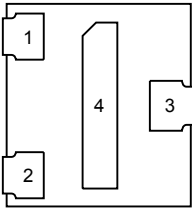
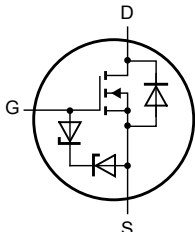
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25$ °C		-	-	12	V
$V_{GS}$	gate-source voltage			-8	-	8	V
$I_D$	drain current	$V_{GS} = 4.5$ V; $T_{amb} = 25$ °C	[1]	-	-	3.2	A
<b>Static characteristics</b>							
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 3.2$ A; $T_j = 25$ °C		-	34	45	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN1010D-3 (SOT1215)	 017aaa255
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB40UNE	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB40UNE	10 00 00

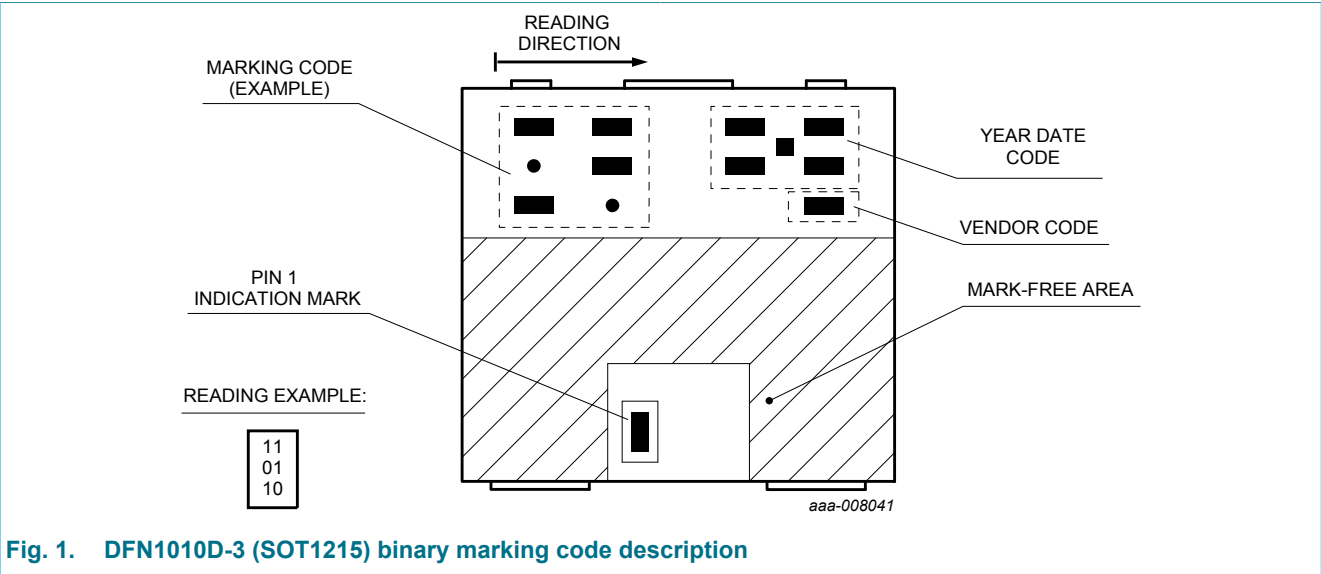


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

## 8. Limiting values

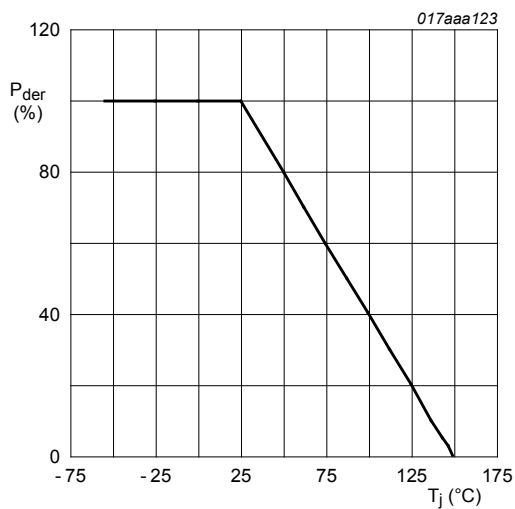
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	12	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	3.2	A
		V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	2.5	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	15	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	0.4	W
			[1]	-	1.07	W
		T <sub>sp</sub> = 25 °C		-	8.33	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	1	A

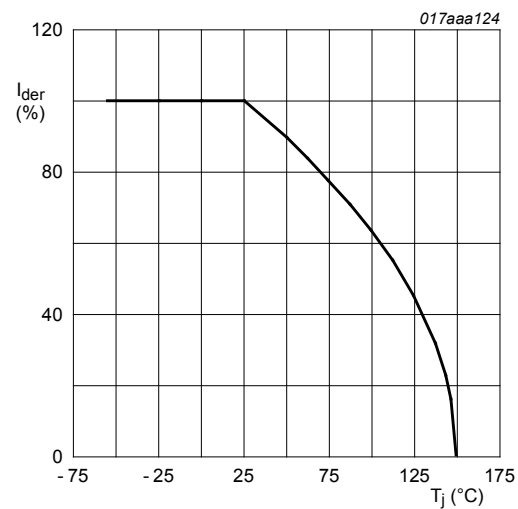
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



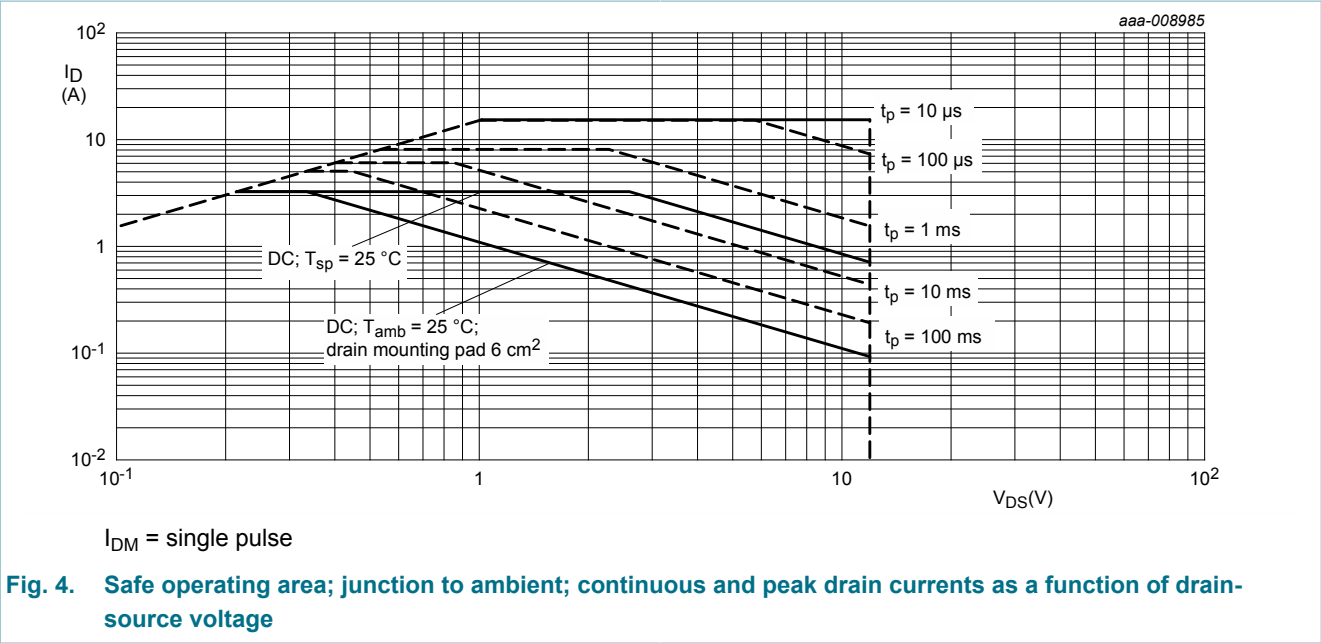
**Fig. 2. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$



**Fig. 3. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

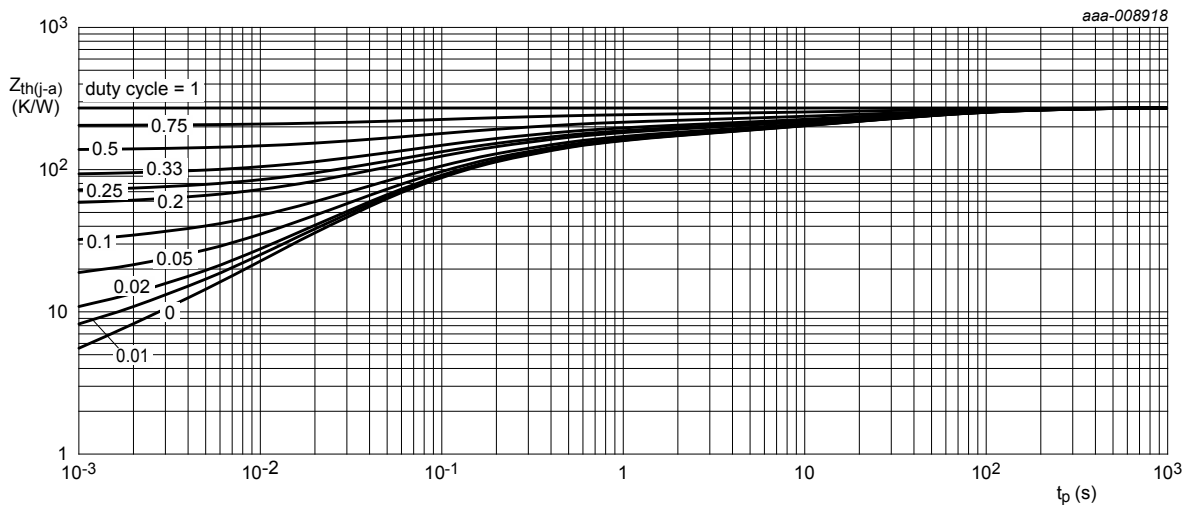


9. Thermal characteristics

Table 6. Thermal characteristics

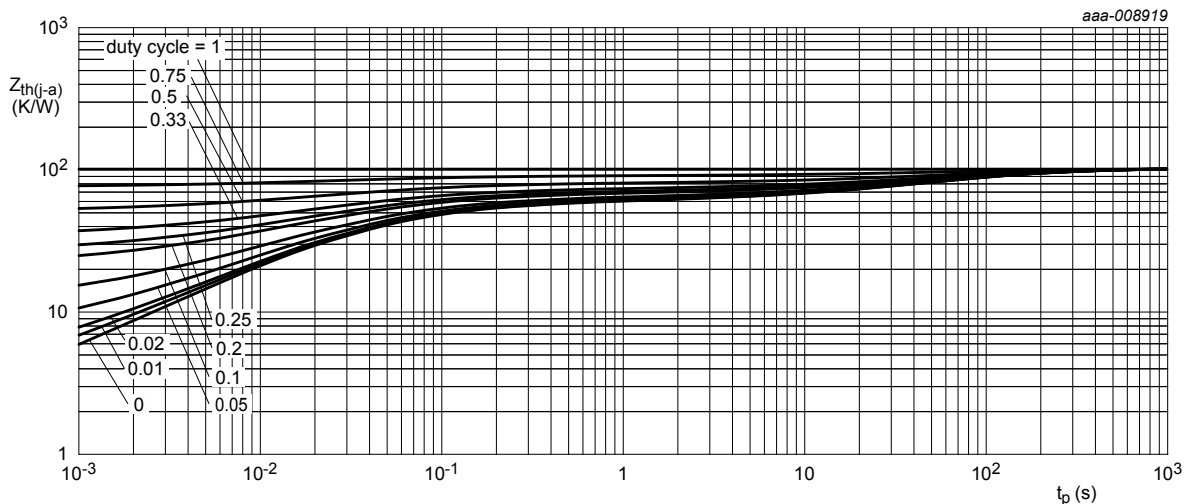
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	311	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		12	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		0.4	0.65	0.9	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 12 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	10	μA
		V <sub>GS</sub> = -8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-10	μA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 3.2 A; T <sub>j</sub> = 25 °C		-	34	45	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 3.2 A; T <sub>j</sub> = 150 °C		-	49	67	mΩ
		V <sub>GS</sub> = 2.5 V; I <sub>D</sub> = 3.2 A; T <sub>j</sub> = 25 °C		-	39	64	mΩ
		V <sub>GS</sub> = 1.8 V; I <sub>D</sub> = 1 A; T <sub>j</sub> = 25 °C		-	46	85	mΩ
		V <sub>GS</sub> = 1.5 V; I <sub>D</sub> = 0.1 A; T <sub>j</sub> = 25 °C		-	50	100	mΩ
		V <sub>GS</sub> = 1.2 V; I <sub>D</sub> = 1 mA; T <sub>j</sub> = 25 °C		-	121	-	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 2 A; T <sub>j</sub> = 25 °C		-	1.2	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz		-	1	-	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 3.2 A; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C		-	6.6	11.6	nC
Q <sub>GS</sub>	gate-source charge			-	0.6	-	nC
Q <sub>GD</sub>	gate-drain charge			-	1.7	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 10 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	556	-	pF
C <sub>oss</sub>	output capacitance			-	107	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	94	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 3.2 A; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C		-	6	-	ns
t <sub>r</sub>	rise time			-	21	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	18	-	ns
t <sub>f</sub>	fall time			-	9	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 1 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	0.8	1.2	V

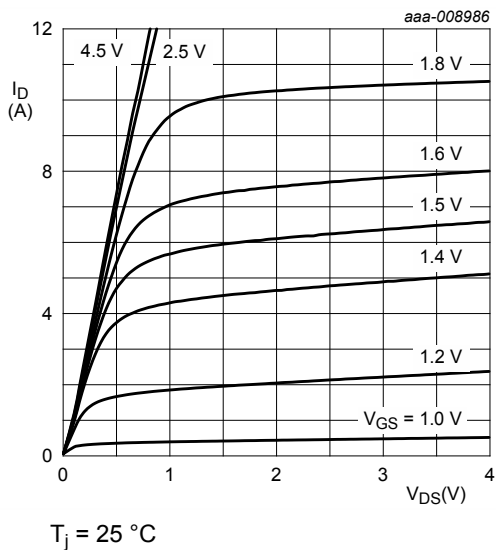


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

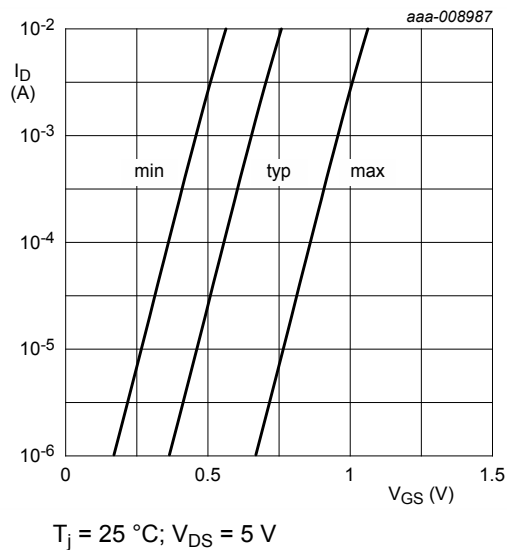


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

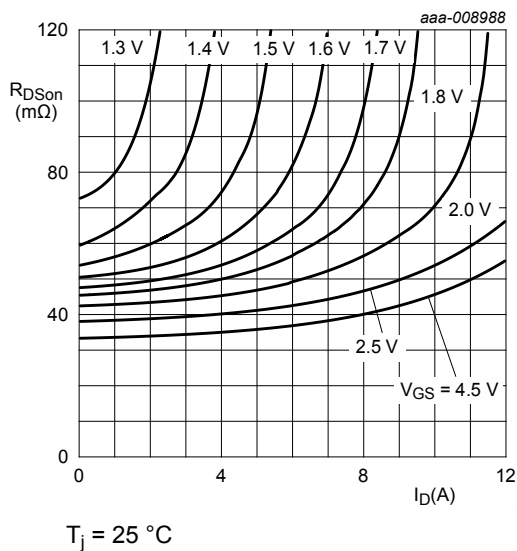


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

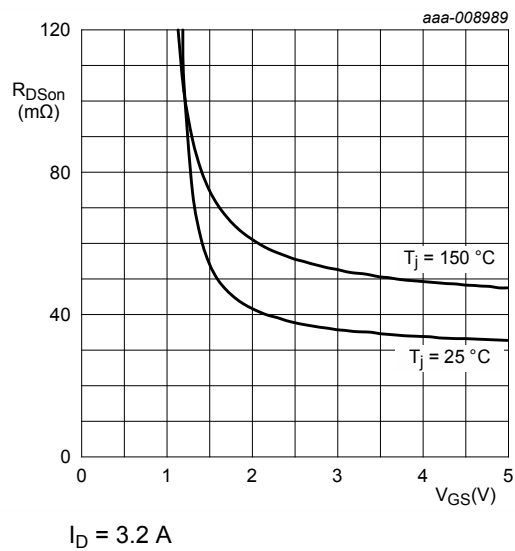


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

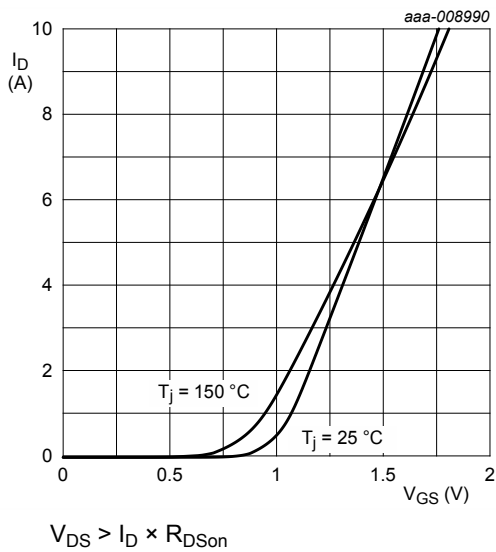


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

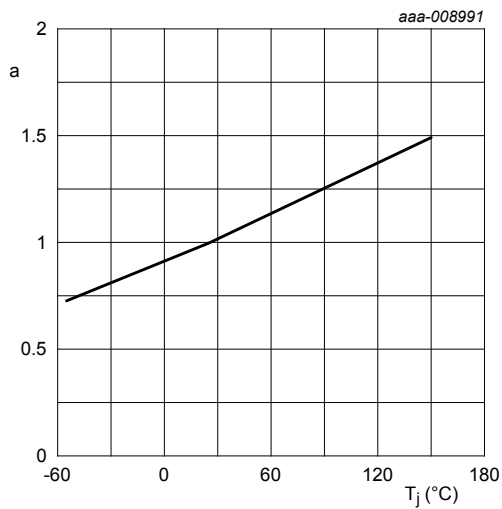


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

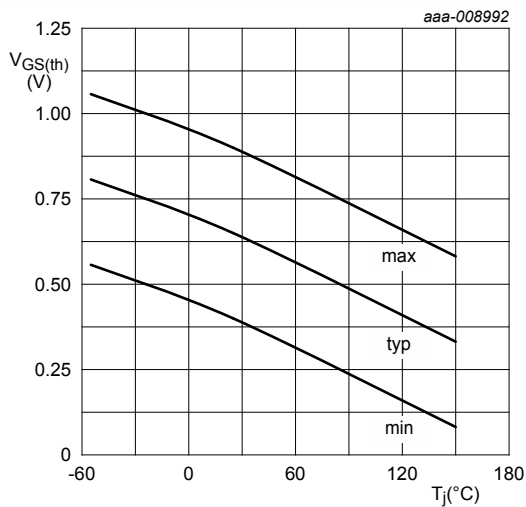


Fig. 13. Gate-source threshold voltage as a function of junction temperature

$$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$$

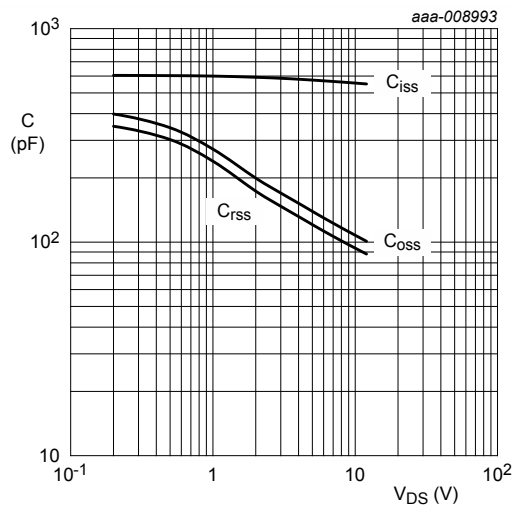


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$$



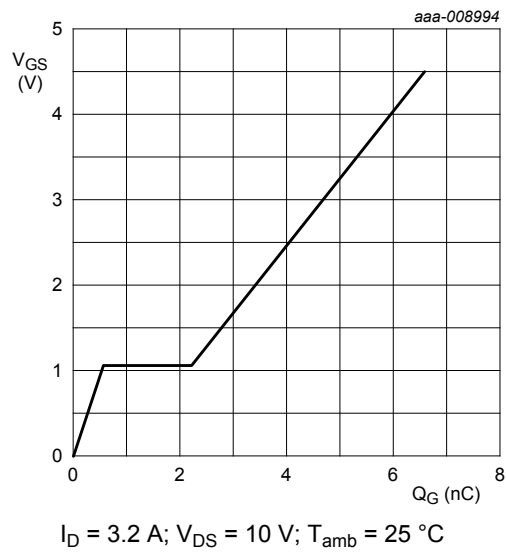


Fig. 15. Gate-source voltage as a function of gate charge; typical values

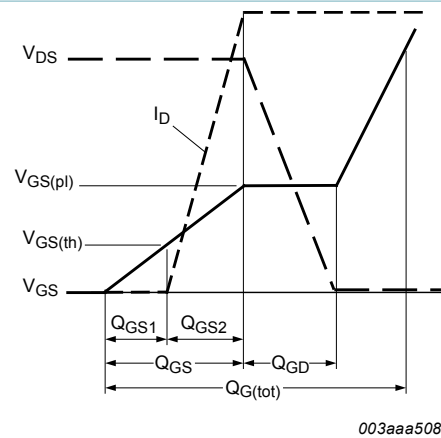


Fig. 16. MOSFET transistor: Gate charge waveform definitions

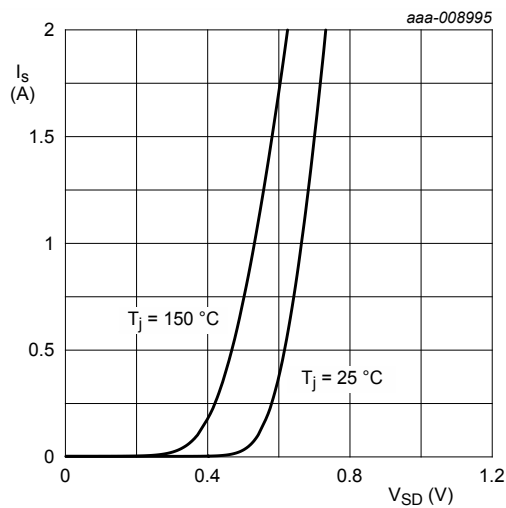


Fig. 17. Source current as a function of source-drain voltage; typical values

## 11. Test information

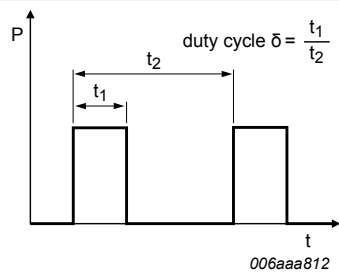


Fig. 18. Duty cycle definition

12. Package outline

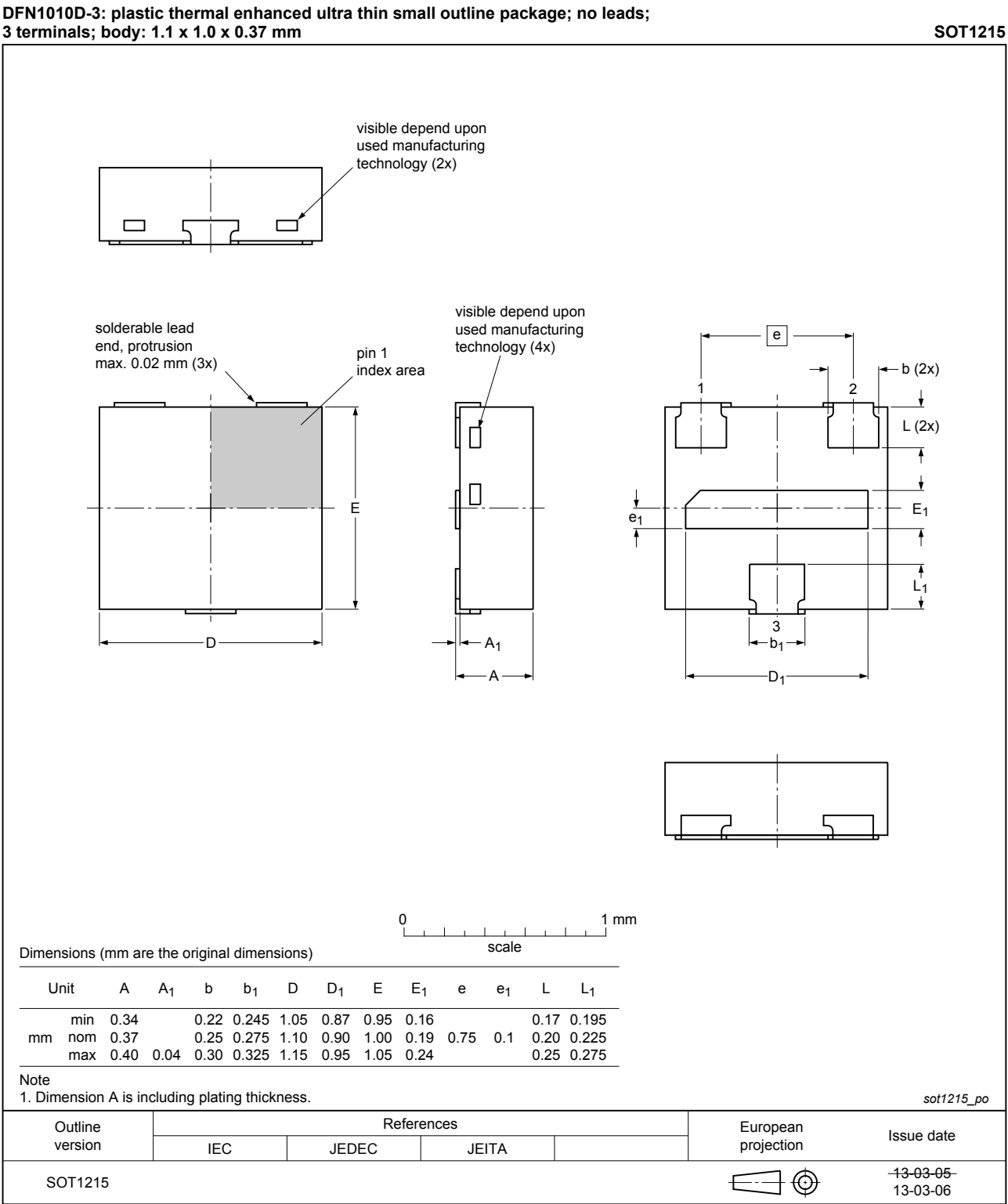


Fig. 19. Package outline DFN1010D-3 (SOT1215)

13. Soldering

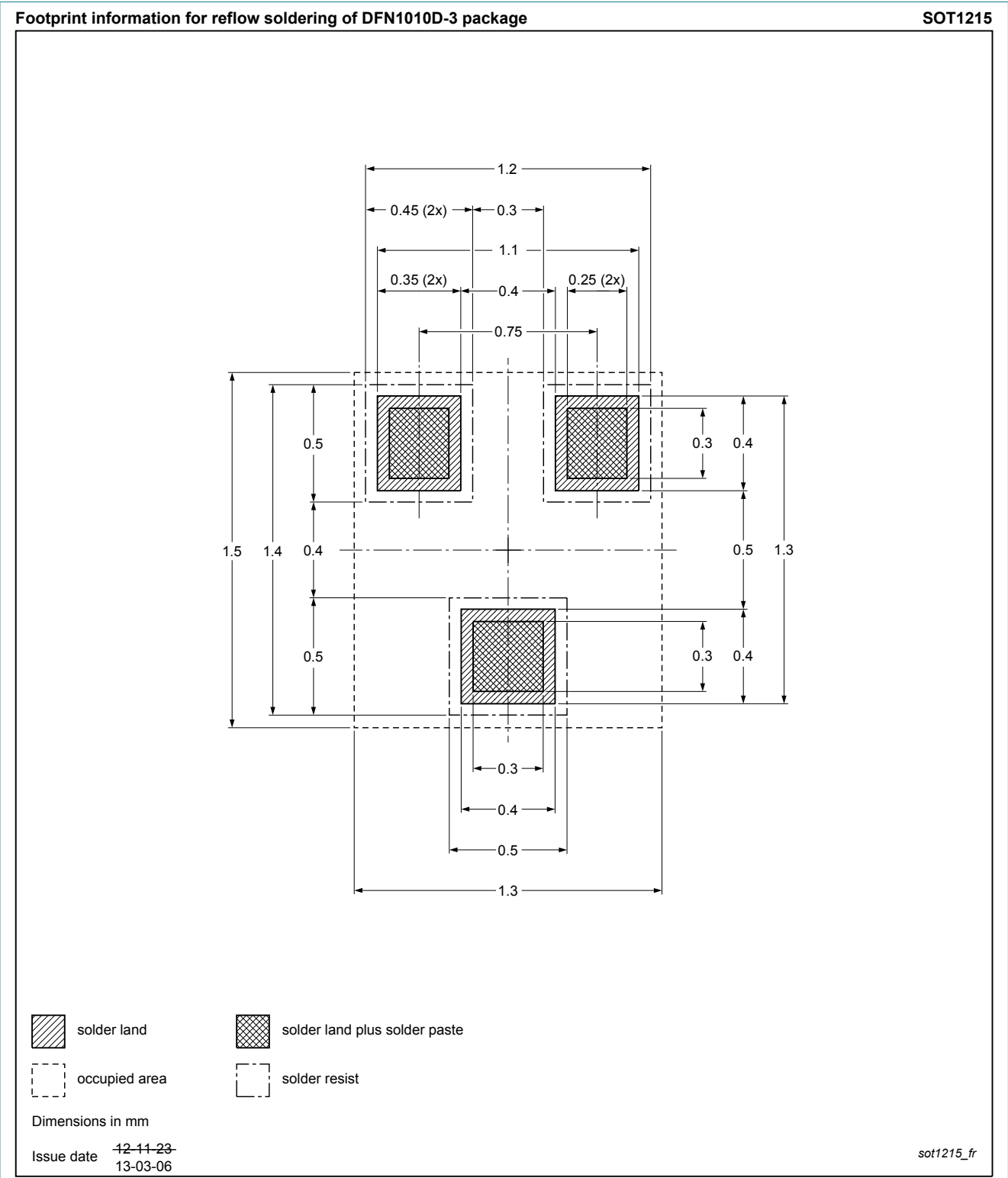


Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB40UNE v.1	20130927	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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