



# PMXB75UPE

20 V, P-channel Trench MOSFET

8 July 2014

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package:  $1.1 \times 1.0 \times 0.37$  mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1.5 kV HBM
- Drain-source on-state resistance  $R_{DS(on)} = 69$  m $\Omega$
- Very low gate-source threshold voltage for portable applications  $V_{GS(th)} = -0.68$  V

## 3. Applications

- High-side load switch and charging switch for portable devices
- Power management in battery driven portables
- LED driver
- DC-to-DC converter

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25$ °C		-	-	-20	V
$V_{GS}$	gate-source voltage			-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5$ V; $T_{amb} = 25$ °C	[1]	-	-	-2.9	A
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5$ V; $I_D = -2.9$ A; $T_j = 25$ °C		-	69	85	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

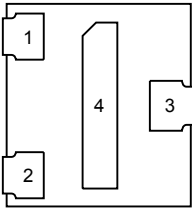
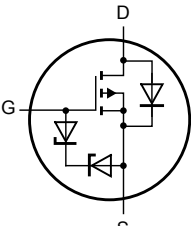


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN1010D-3 (SOT1215)	 017aaa259
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMXB75UPE	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB75UPE	00 01 00

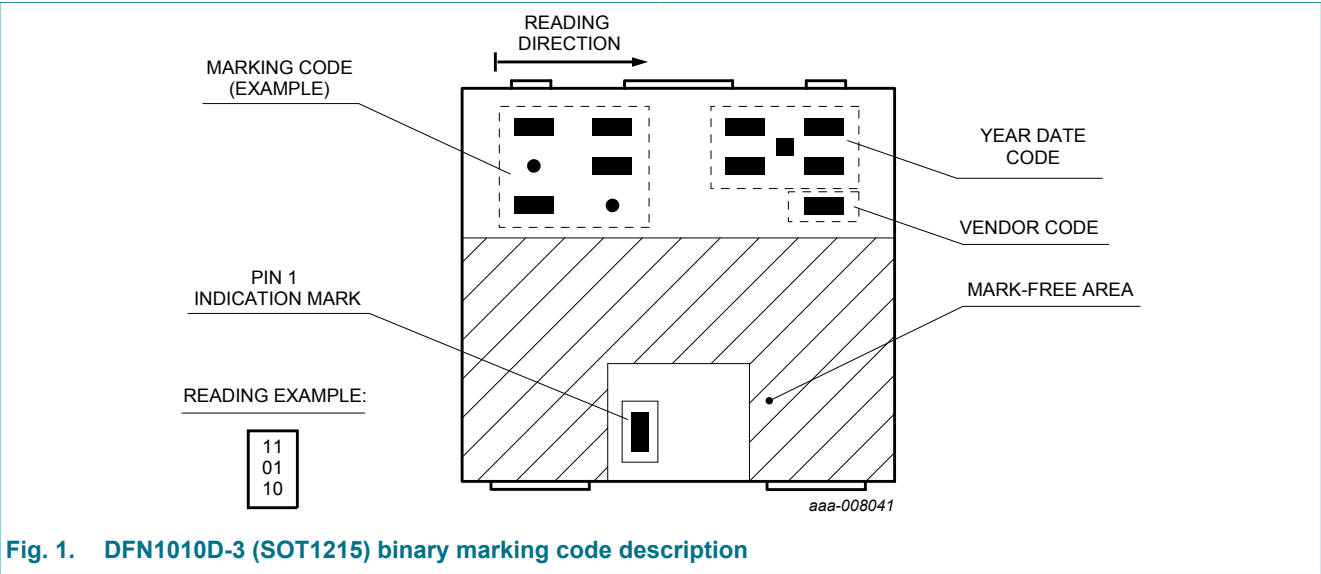


Fig. 1. DFN1010D-3 (SOT1215) binary marking code description

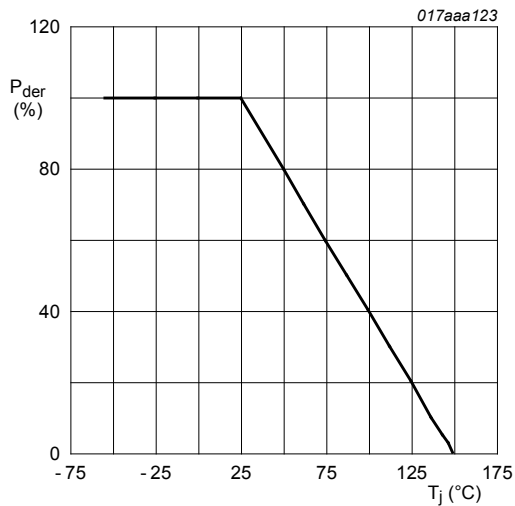
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

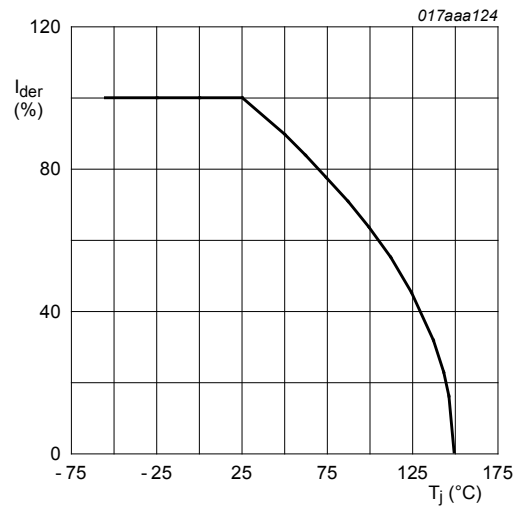
Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-20	V
V <sub>GS</sub>	gate-source voltage			-8	8	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-2.9	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-1.9	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	-12	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	317	mW
			[1]	-	1070	mW
		T <sub>sp</sub> = 25 °C		-	8330	mW
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.  
 [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



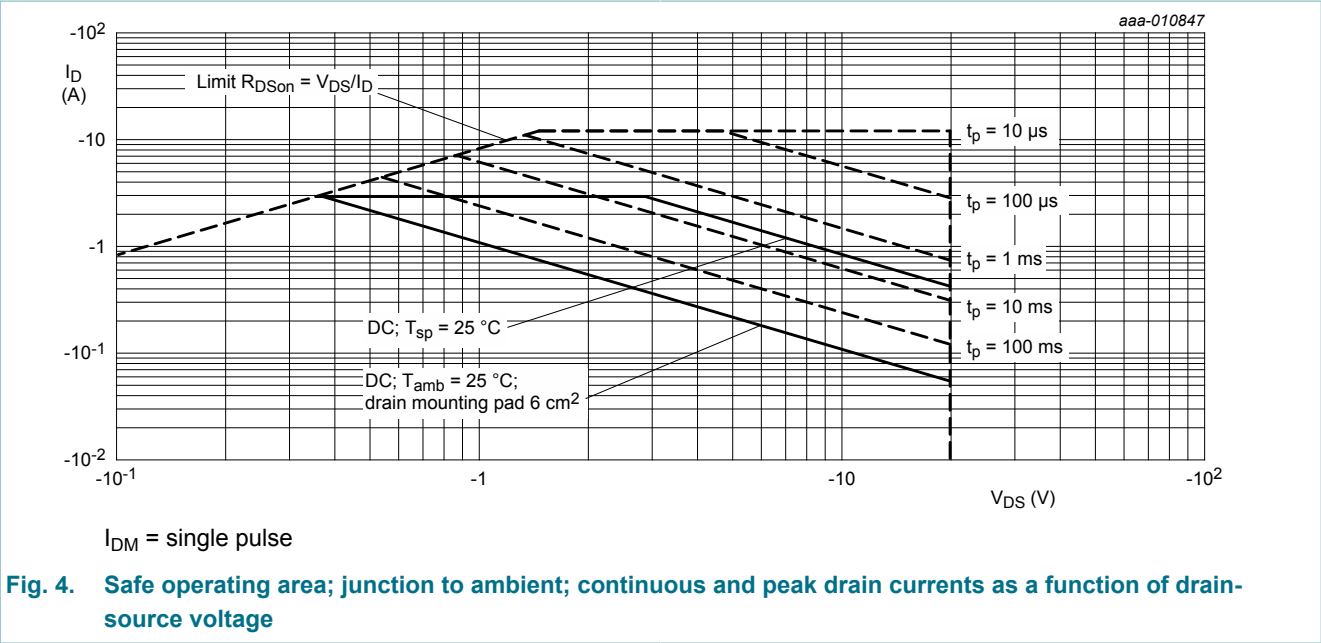
**Fig. 2. Normalized total power dissipation as a function of junction temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100 \%$$



**Fig. 3. Normalized continuous drain current as a function of junction temperature**

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100 \%$$

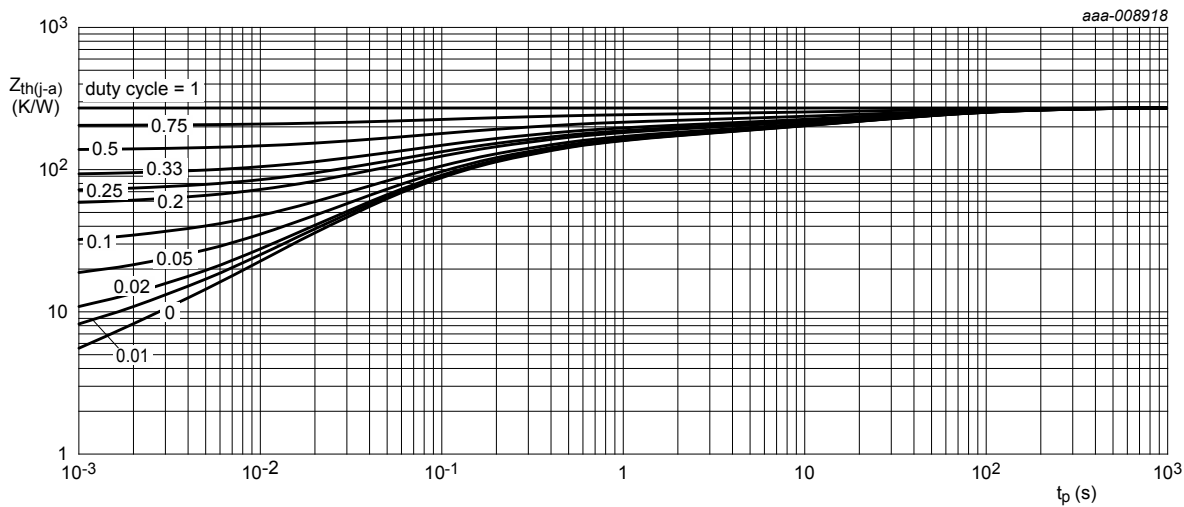


9. Thermal characteristics

Table 6. Thermal characteristics

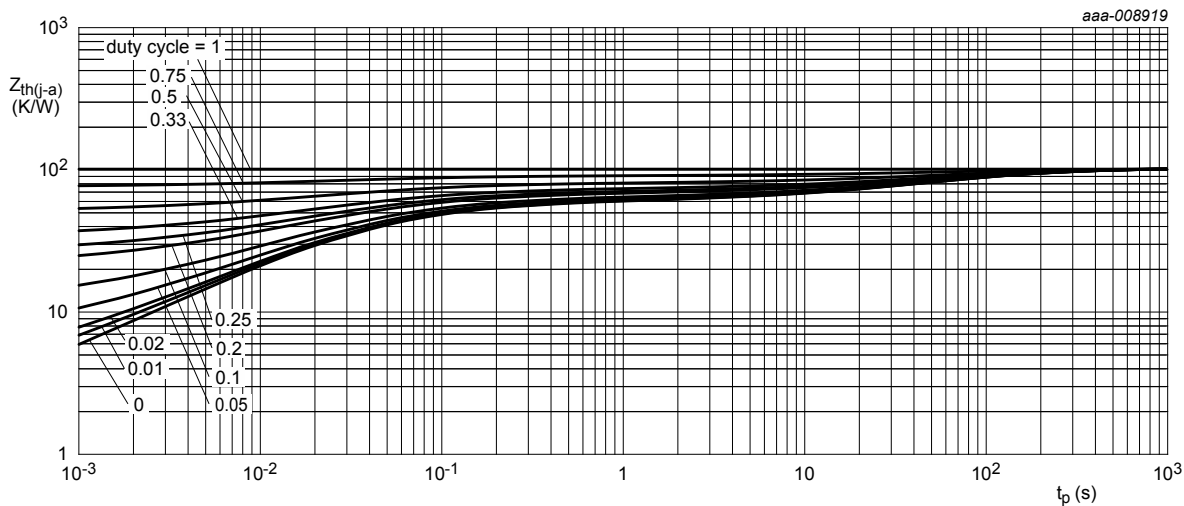
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	312	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.  
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = -250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-20	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = -250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		-0.4	-0.68	-1	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = -20 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = -8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-10	μA
		V <sub>GS</sub> = 8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	10	μA
		V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA
		V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -2.9 A; T <sub>j</sub> = 25 °C		-	69	85	mΩ
		V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -2.9 A; T <sub>j</sub> = 150 °C		-	99	122	mΩ
		V <sub>GS</sub> = -2.5 V; I <sub>D</sub> = -2.6 A; T <sub>j</sub> = 25 °C		-	86	110	mΩ
		V <sub>GS</sub> = -1.8 V; I <sub>D</sub> = -0.4 A; T <sub>j</sub> = 25 °C		-	130	200	mΩ
		V <sub>GS</sub> = -1.5 V; I <sub>D</sub> = -50 mA; T <sub>j</sub> = 25 °C		-	205	450	mΩ
		V <sub>GS</sub> = -1.2 V; I <sub>D</sub> = -10 mA; T <sub>j</sub> = 25 °C		-	950	-	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = -10 V; I <sub>D</sub> = -2 A; T <sub>j</sub> = 25 °C		-	8.4	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz		-	11.3	-	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = -10 V; I <sub>D</sub> = -2.9 A; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C		-	6.8	12	nC
Q <sub>GS</sub>	gate-source charge			-	0.9	-	nC
Q <sub>GD</sub>	gate-drain charge			-	2.1	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = -10 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	608	-	pF
C <sub>oss</sub>	output capacitance			-	75	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	64	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = -10 V; I <sub>D</sub> = -2.9 A; V <sub>GS</sub> = -4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C		-	6	-	ns
t <sub>r</sub>	rise time			-	19	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	29	-	ns
t <sub>f</sub>	fall time			-	15	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = -1 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-0.7	-1.2	V

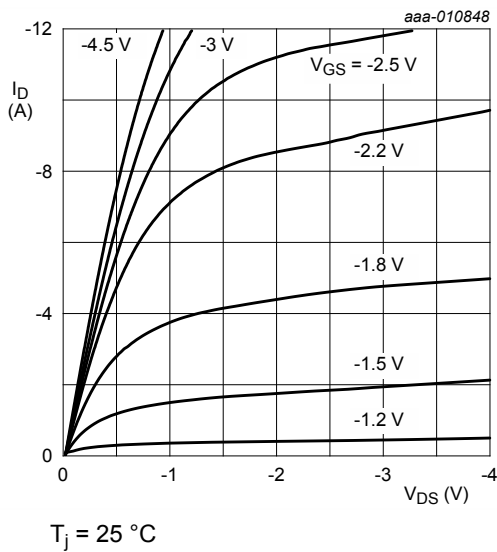


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

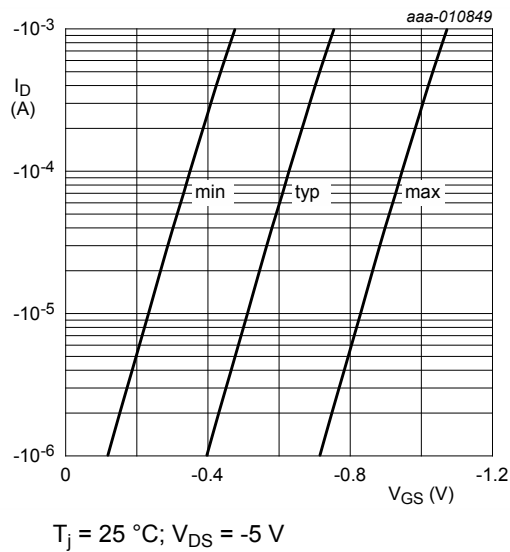


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

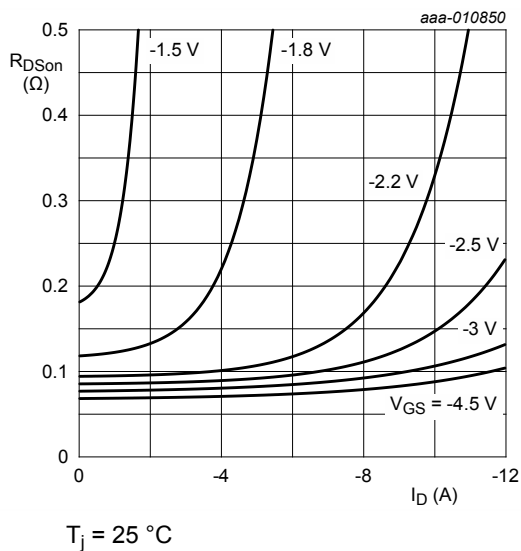


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

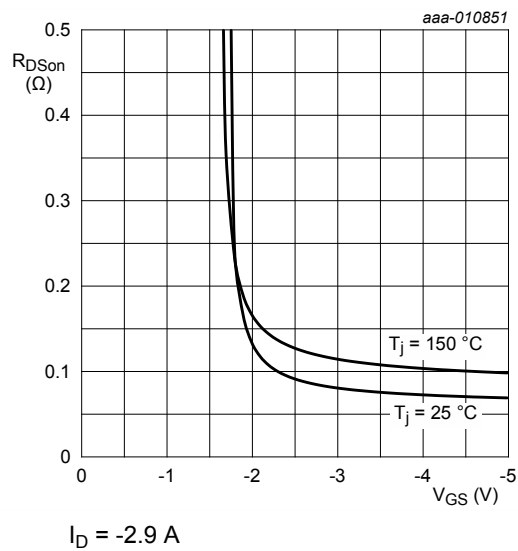


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

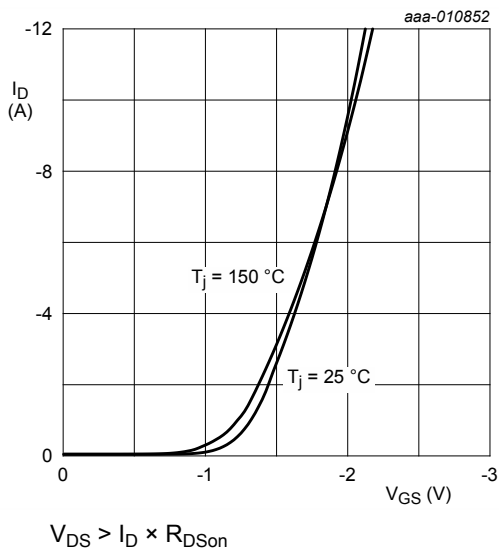


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

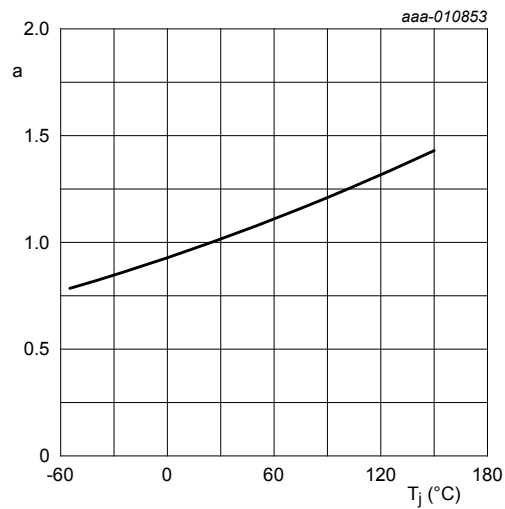


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DS(on)}}{R_{DS(on)25\text{ °C}}}$$

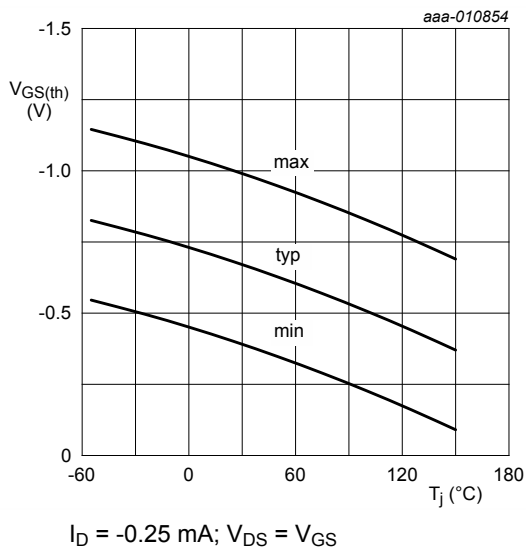


Fig. 13. Gate-source threshold voltage as a function of junction temperature

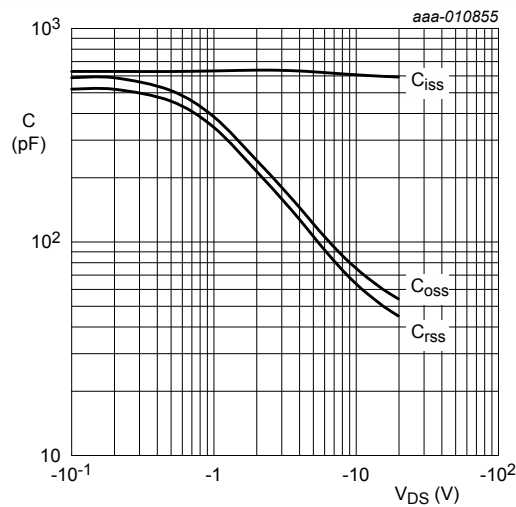


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



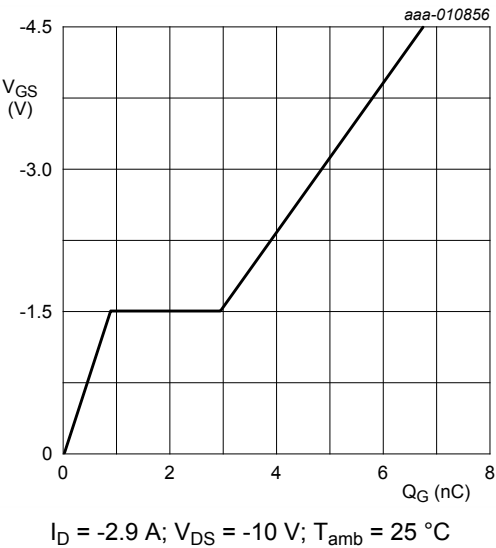


Fig. 15. Gate-source voltage as a function of gate charge; typical values

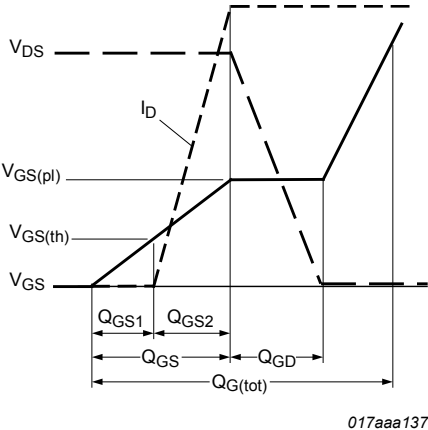


Fig. 16. MOSFET transistor: Gate charge waveform definitions

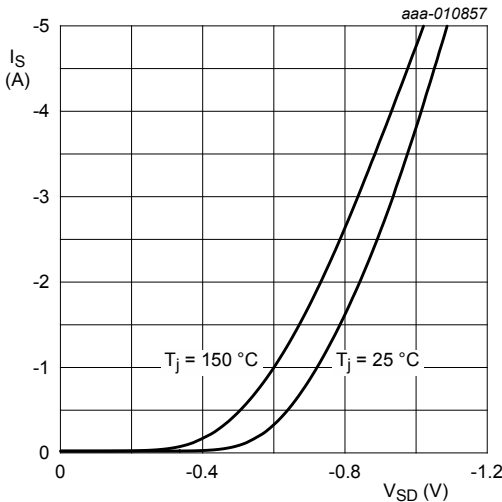


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

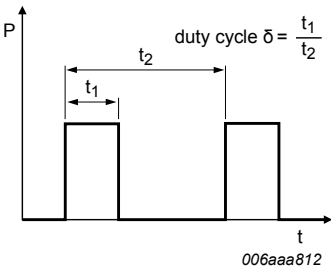


Fig. 18. Duty cycle definition

12. Package outline

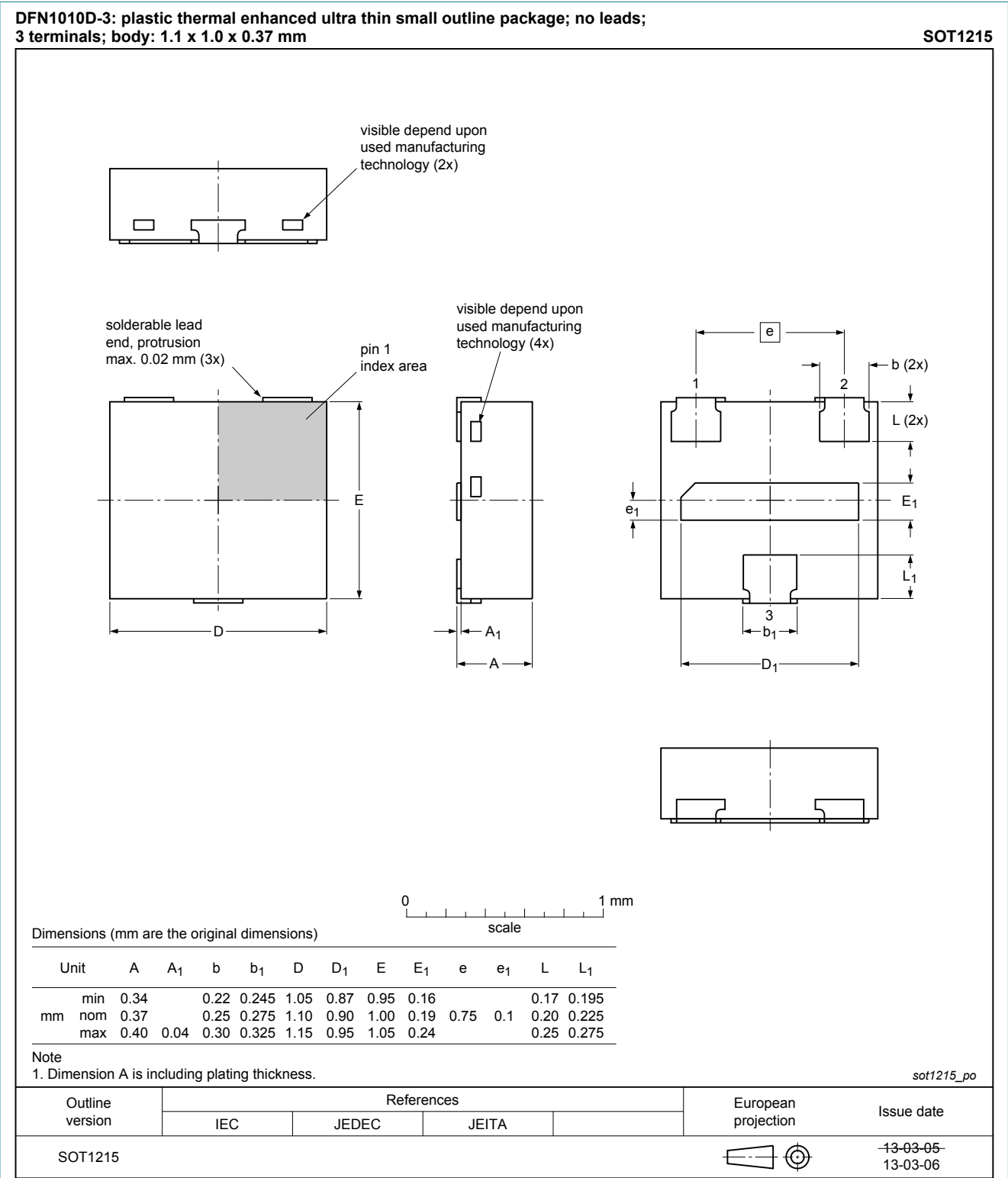


Fig. 19. Package outline DFN1010D-3 (SOT1215)

13. Soldering

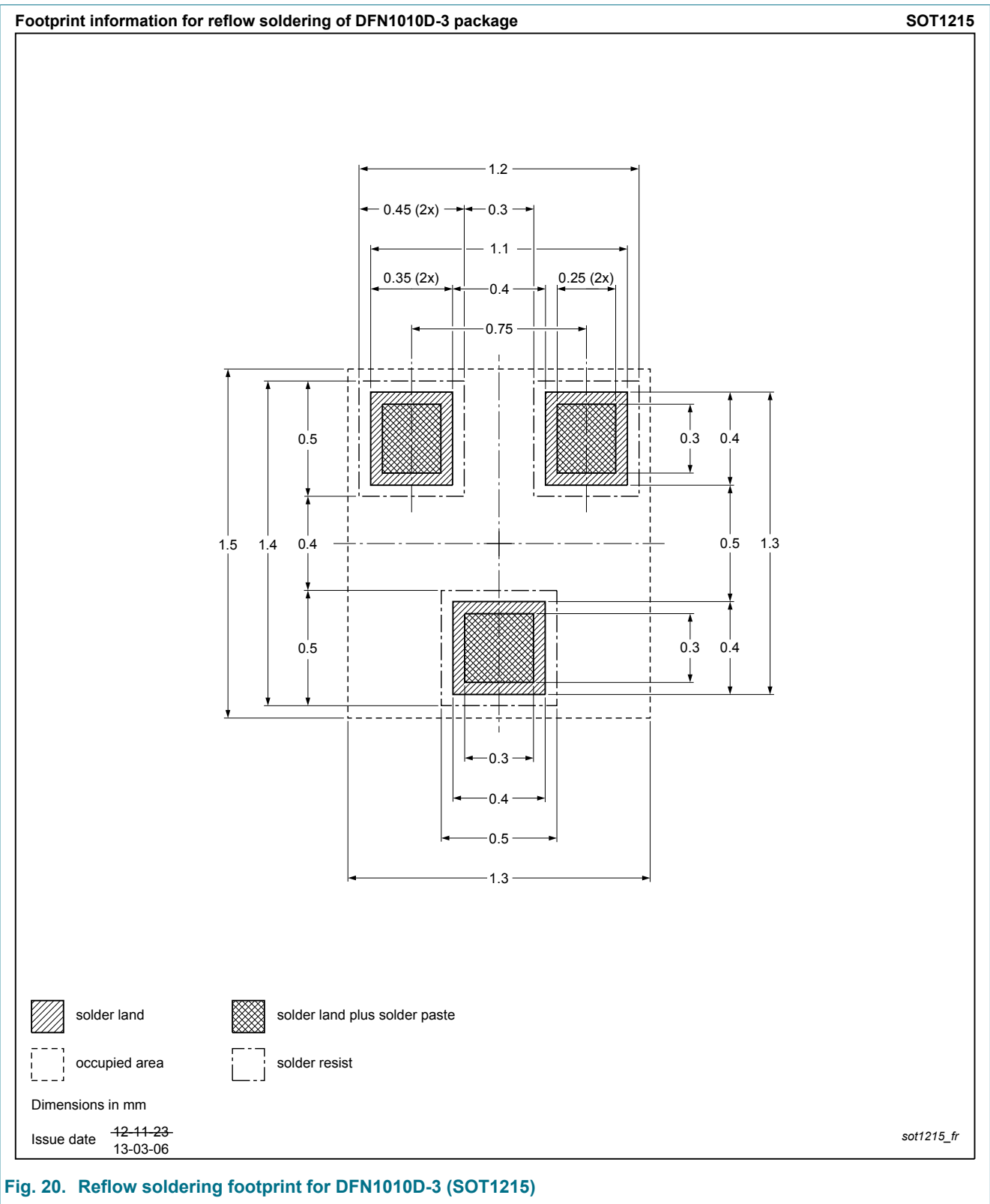


Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB75UPE v.3	20140708	Product data sheet	-	PMXB75UPE v.2
Modifications:	<ul style="list-style-type: none"><li>Product status changed</li></ul>			
PMXB75UPE v.2	20140218	Preliminary data sheet	-	PMXB75UPE v.1
PMXB75UPE v.1	20140204	Preliminary data sheet	-	-

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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