PN4302 SERIES

Siliconix incorporated

N-Channel JFETs

The PN4302 Series of multi-purpose JFETs is designed for a wide range of low cost applications. It features low gate leakage and capacitance, which makes these devices ideal for high-frequency amplifiers. This series is packaged in TO-92 for low cost and compatibility with automated assembly.

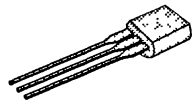
For further design information please consult the typical performance curves NPA which are located in Section 7.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$V_{(BR)GSS}$ MIN (V)	g_{fs} MIN (mS)	I_{DSS} MAX (mA)
PN4302	-4	-30	1	5
PN4303	-6	-30	2	10
PN4304	-10	-30	1	15

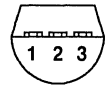
SIMILAR PRODUCTS

- TO-18, See 2N4338 Series
- SOT-23, See SST201 Series
- Chips, Order PN430XCHP

TO-92



BOTTOM VIEW



1 DRAIN
2 SOURCE
3 GATE

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS
Gate-Drain Voltage	V_{GD}	-30	V
Gate-Source Voltage	V_{GS}	-30	
Gate Current	I_G	50	mA
Power Dissipation	P_D	360	mW
Power Derating		3.27	mW/°C
Operating Junction Temperature	T_J	-55 to 135	°C
Storage Temperature	T_{stg}	-55 to 150	
Lead Temperature (1/16" from case for 10 seconds)	T_L	300	

ELECTRICAL CHARACTERISTICS[1]			LIMITS							
				PN4302		PN4303		PN4304		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[2]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-57	-30		-30		-30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 20 V, I_D = 10 nA			-4		-6		-10	V
Saturation Drain Current[3]	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V		0.5	5	4	10	0.5	15	mA
Gate Reverse Current	I_{GSS}	V_{GS} = -10 V, V_{DS} = 0 V	-0.001		-1		-1		-1	nA
		T_A = 85°C	-0.03		-100		-100		-100	
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 kHz		1		2		1		mS
Common-Source Output Conductance	g_{os}				50		50		50	µS
Common-Source Input Capacitance	C_{iss}	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	4.5		6		6		6	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		1.3		3		3		3	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz	6							$nV/\sqrt{Hz}$
Noise Figure	NF	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz, R_G = 1 MΩ	<0.1		2		2		3	dB

NOTES: 1. T_A = 25 °C unless otherwise noted.
2. For design aid only, not subject to production testing.
3. Pulse test; PW = 300 µs, duty cycle ≤ 3%.

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