PN65K

Near Field Communication (NFC) SmartConnect Module in a single package

Rev. 1.3 — 20 October 2006   **Objective short data sheet**

1. General description

PN65K combines in a single package a Near Field Communication (NFC) controller PN531 and a Secure Smart Card controller. They are tied together by the means of external connections for the S^{2}C interface and the PN531 is supplying the Smart card controller by the means of a specific internal regulator. The embedded PN531 firmware drives the supply to the Smart*MX* device when required in order to optimize the overall current consumption of the SmartConnect device.

The PN65K can behave as an NFC initiator, working in active or passive mode and when operating in passive mode it can operate as a reader/writer for Mifare or FeliCa contactless smart cards. The Peer to peer functionality is also supported in both active and passive modes.

The PN65K can also operate as a card mode and specially when the combined Smart*MX* device is enabled it can operate as a pure Mifare card or as a fully compliant ISO14443A 3&4 contactless smart card.

1.1 Naming conventions

P65xyy(y)z	SmartConnect Module
PN65	SmartConnect module based on the Smard Card IC P5CNaabb plus NFC IC
x	defines the NFC IC Pn5xx, e.g. A for PN511, B for PN512, K for PN531, L for PN532
yy(y)	Package Type: HN for HVQFN
z	Optional parameter for discrete components in the integrated in the MCM or version identification
Example:	
PN65KHN1	K: module with PN531, HN: HVQFN package, 1: pure MCM version

2. Features

2.1 General

■ SmartConnect module integrating NFC controller PN531 device and Smart*MX* (P5CN072) secure smart card controller in a single package.

■ Single package solution for size optimization; needs external antenna matching circuitry, uncoupling capacitors and crystal oscillator.

■ Fully NFC IP-1 (ISO18092) compliant

2.2 NFC controller

■ 80C51 microcontroller core with 32 Kbyte ROM and 1 Kbyte RAM

■ Highly integrated analog circuitry to demodulate and decode responses

■ Buffered output drivers to connect an antenna with minimum number of external components

■ Integrated RF Level detector

■ Integrated data mode detector

■ Supports ISO 14443A/Mifare

■ Typical operating distance in reader/writer mode for communication to a ISO 14443A/Mifare or FeliCa card up to 50 mm depending on the antenna size and tuning

■ Typical operating distance in NFCIP-1 mode up to 50 mm depending on the antenna size and tuning and power supply

■ Typical operating distance in ISO 14443A/Mifare card or FeliCa card interface mode of about 100 mm depending on the antenna size and tuning and the external field strength

■ Supports Mifare Classic encryption in reader/writer mode and Mifare higher transfer speed communication at 212 kbit/s and 424 kbit/s

■ Supports contactless communication according to the FeliCa scheme at 212 kBaud and 424 kBaud

■ Integrated RF interface for NFCIP-1 up to 424 kBaud

■ Possibility to communicate on the RF interface above 424 kBaud using external analog circuitry

■ Supported host interfaces
   ◆ SPI interface
   ◆ I^{2}C interface
   ◆ High Speed Serial UART (similar to RS232 with 0 and PVDD voltage levels)

■ Flexible interrupt using IRQ pin

■ Hard reset with low power function

■ Power-down mode per embedded firmware

■ Programmable timer

■ Internal oscillator to connect 27.12 MHz crystal

■ 3.3 V power supply when not USB bus powered

■ Power Switch for external secure component

■ Specific IO ports for external devices control

2.3 Secure smart card controller

The device used in this module is the P5CN072 Secure Dual Interface PKI Smart Card Controller which has the following features:

■ 72 Kbytes EEPROM
■ 160 Kbytes User ROM
■ 4608 bytes RAM
■ PKI (Public Key Infrastructure) co-processor
■ Dual Triple DES Key co-processor
■ S^{2}C interface to enable secure contact-less communication via NFC (Near Field Communication)
■ EEPROM data retention time: 20 years minimum

The P5CN072 is a Secure Dual interface PKI Smart Card Controller of the Smart*MX* platform featuring 160 Kbytes of user ROM, 4608 bytes of RAM and 72 Kbytes of EEPROM which can be used as data memory or as program memory. The non-volatile memory consists of high reliability memory cells to guaranty data integrity which is important especially when EEPROM memory is used as program memory.

Operated both in contact mode (ISO IEC 7816) or S^{2}C mode, the user defines the final function of the chip with his chip operating system (COS). This allows the same level of security, functionality and flexibility for the contact interface as well for the S^{2}C interface.

The S^{2}C technology provides reliable digital communication to the PN531 NFC device to enable secure contactless communication for NFC enabled devices.

The S^{2}C interface is connected internally to the internal ISO 14443 CIU. The CIU handles the modulation and demodulation of the S^{2}C signals so that a full contact-less communication should be enabled using this interface. The supply VDD is provided by the PN531 voltage regulator.

The P5CN072 offers the same features of contact and contact-less mode handling as the other members of the Smart*MX* family.

Connected via the S^{2}C interface to the PN531 NFC controller, P5CN072 is compatible with Mifare reader infrastructure and the optional free of charge emulation mode of Mifare 1K and Mifare 4K enable fast system integration and backward compatibility of standard Mifare and ProX family based cards. The communication on the S^{2}C interface support ISO IEC 14443A-3 and ISO IEC 14443A-4 parts.

The on chip hardware is software controlled through special function registers (SFRs). Their function and usage is described in the P5CN072 data sheet.

The P5CN072 is powered by the PN531 device.

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3. Applications

- ■ mobile phones
- ■ portable equipments (Personal Digital Assistants, notebooks)
- ■ accessories (keyfobs, memory cards)
- ■ consumer devices

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BUS}	Supply Voltage (non USB mode)	$V_{BUS} = D_{VDD}$ $V_{SS} = 0$ V	2.5	3.3	3.6	V
TV_{DD}, AV_{DD}, DV_{DD}	Supply Voltage	$TV_{DD} = AV_{DD} = DV_{DD}$ [1] $V_{SS} = 0$ V	2.5	3.3	3.6	V
PV_{DD}	Supply Voltage for host interface	$V_{SS} = 0$ V	1.6		3.6	V
SV_{DD}	Supply Voltage for SAM interface	$V_{SS} = 0$ V (SV_{DD} Switch Enabled)	2.4		3.6	V
IH_{PD}	Hard Power Down Current (Not powered from USB)	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, RF level detector off			10	μA
IS_{PD}	Soft Power down Current (Not powered from USB)	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, RF level detector on			30	μA
IDV_{DD}	Digital Supply Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V,RF level detector on, SVDD switch off [1]		15		mA
ISV_{DD}	SV_{DD} Supply Current	$SV_{DD} = 3$ V, SV_{DD} switch On			30	mA
IAV_{DD}	Analog Supply Current	$AV_{DD} = DV_{DD} = TV_{DD} = PV_{DD} = 3$ V, RF level detector on		6		mA
ITV_{DD}	Transmitter Supply Current	During RF Transmission, $TV_{DD} = 3$ V		60	100	mA
P_{tot}	continuous total power dissipation in non USB mode	$T_{amb} = -30$ to $+85$ °C			0.15	W
T_{amb}	operating ambient temperature		-30		+85	°C

[1] DV_{DD}, AV_{DD} and TV_{DD} shall always be at the same supply voltage.

5. Ordering information

Table 2: **Ordering information**

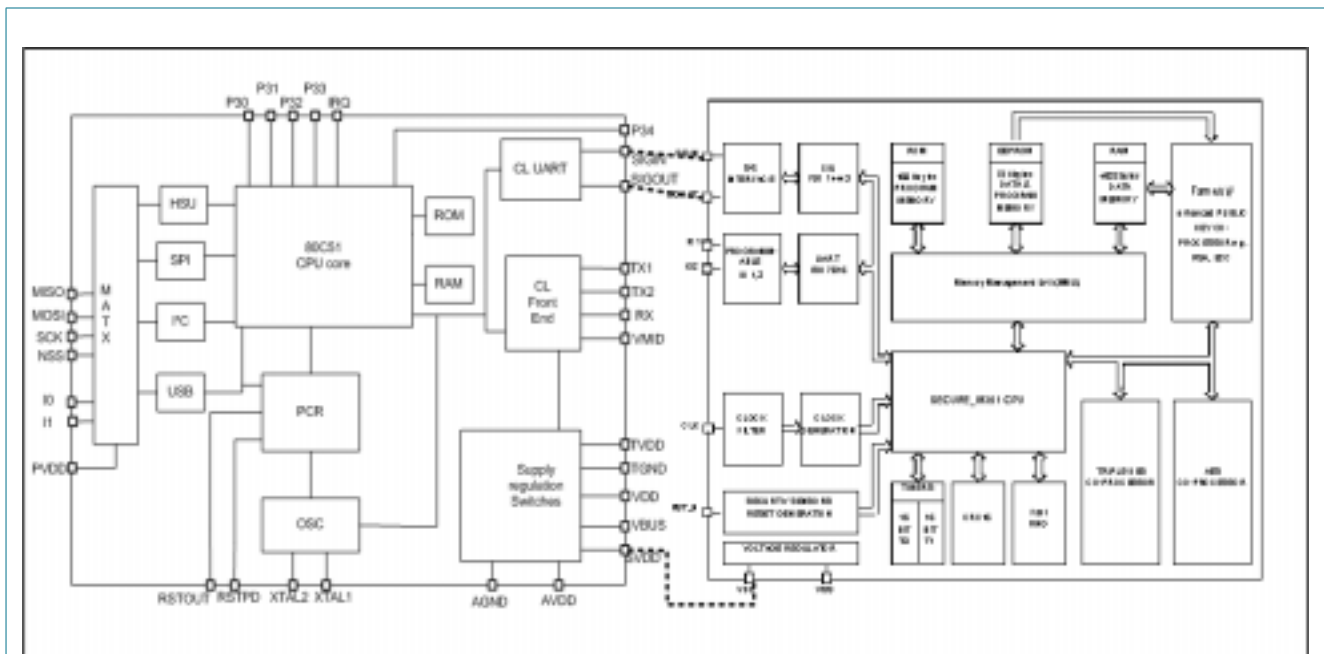| Type number	Package		Version
	Name	**Description**	
PN65KHN1/C2xxyyy	HVQFN48	Plastic thermal enhanced very thin package quad flat package; no leads 48 terminals; $7 \times 7 \times 0.85$ mm	SOT619

6. Block diagram

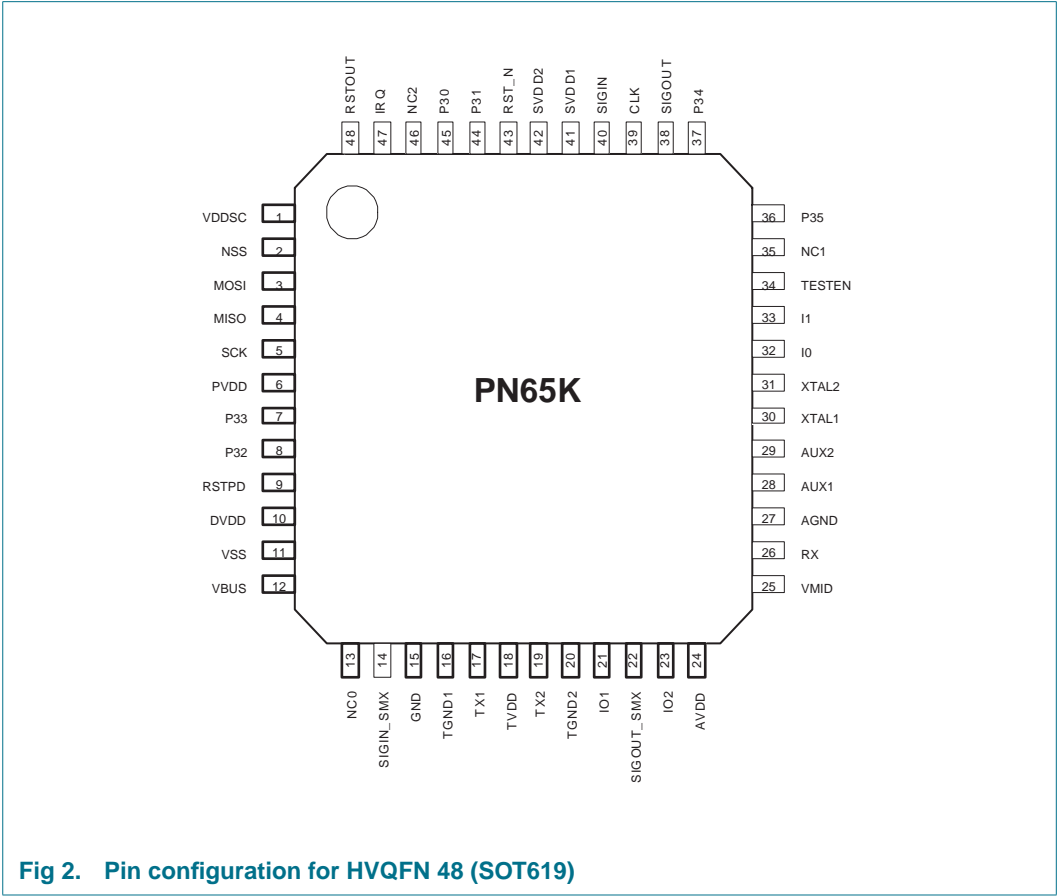**Fig 1. Block diagram of PN65K**

7. Pinning information

7.1 Pinning

Fig 2. **Pin configuration for HVQFN 48 (SOT619)**

7.2 Pin description

Table 3: **Pin description**

Symbol	Pin	Type	Pad Ref Voltage	Description
VDDSC	1	PWR		Smart*MX* supply; to be connected to pins SVDD1 and SVDD2
NSS	2	IO	PVDD	Not Slave Select. In test mode this signal is used as input and output test signal.
MOSI	3	IO	PVDD	Master Out Slave In. In test mode this signal is used as input and output test signal
MISO	4	IO	PVDD	Master In Slave Out. In test mode this signal is used as input and output test signal
SCK	5	IO	PVDD	Serial interface clock. In test mode this signal is used as input and output test signal
PVDD	6	PWR		Pad power supply

Table 3:   **Pin description** *…continued*

Symbol	Pin	Type	Pad Ref Voltage	Description
P33	7	IO	PVDD	General purpose IO signal. Can be used to generate an HZ state on the output of the selected interface for the Host communication and to enter PN531 into Power-down mode without resetting the internal state of PN531. In test mode this signal is used as input and output test signal.
P32	8	IO	PVDD	General purpose IO signal. Can also be used as an interrupt source In test mode this signal is used as input and output test signal.
RSTPD	9	I	PVDD	Reset and Power Down: When High, internal current sources are switched off, the oscillator is inhibited, and the input pads are disconnected from the outside world. With a positive edge on this pin the internal reset phase starts.
DVDD	10	PWR		Digital Power Supply
VSS	11	PWR		Ground for Smart*MX*
VBUS	12	PWR	DVDD	Supply voltage
NC0	13			Do not connect
SIGIN_SMX	14	IO	VDDSC	S^2C signal to PN531
GND	15	PWR		Ground
TGND1	16	PWR		Transmitter ground
TX1	17	O	TVDD	Transmitter 1: delivers the modulated 13.56 MHZ energy carrier
TVDD	18	PWR		Transmitter supply voltage; supply the output stage of TX1 TX2
TX2	19	O	TVDD	Transmitter 2: delivers the modulated 13.56 MHZ energy carrier
TGND2	20	PWR		Transmitter ground
IO1	21	IO	VDDSC	Smart*MX*: Input/Output 1 for serial data
SIGOUT_SMX	22	I	VDDSC	S^2C signal from the PN531
IO2	23	IO	VDDSC	Smart*MX*: Input/Output 2for serial data
AVDD	24	PWR		Analog power supply
VMID	25	PWR	AVDD	Internal Reference Voltage: This pin delivers the internal reference voltage.
RX	26	I	AVDD	Receiver Input: Input pin for the reception signal, which is the load modulated 13.56 MHZ energy carrier from the antenna circuit.
AGND	27	PWR		Analog Ground
AUX1	28	O	DVDD	Auxiliary Output: This pin delivers analog and digital test signals.
AUX2	29	O	DVDD	Auxiliary Output: This pin delivers analog and digital test signals.
XTAL1	30	I	AVDD	Crystal Oscillator Input: input to the inverting amplifier of the oscillator.This pin is also the input for an externally generated clock (f_{osc} = 27.12 MHZ).
XTAL2	31	O	AVDD	Crystal Oscillator output: Output of the inverting amplifier of the oscillator.
I0	32	I	DVDD	Interface mode lines: selects the used host interface. In test mode I0 is used as test signals.
I1	33	I	DVDD	Interface mode lines: selects the used host interface. In test mode I0 is used as test signals.
TESTEN	34	I	DVDD	Test enable pin: When set to 1 enable the test mode. When set to 0 reset the TCB and disable the access to the test mode.
NC1	35			Do not connect
P35	36	IO	DVDD	General purpose IO signal.

Table 3:   **Pin description** *…continued*

Symbol	Pin	Type	Pad Ref Voltage	Description
P34	37	IO	SVDD	General purpose IO signal.
SIGOUT	38	O	SVDD	Contactless communication interface output: delivers a serial data stream according to NFCIP-1 and output signal for the SAM. In test mode this signal is used as test signal output.
CLK	39	I	VDDSC	SMX Clock input
SIGIN	40	I	SVDD	Contactless communication interface input: accepts a digital, serial data stream according to NFCIP-1 and input signal from the SAM. In test mode this signal is used as test signal input.
SVDD1	41	PWR		Output power for Smart*MX* power supply. Switched on by Firmware with an overload detection. Used as a reference voltage for SAM communication.
SVDD2	42	PWR		Output power for Smart*MX* power supply. Switched on by Firmware with an overload detection. Used as a reference voltage for SAM communication.
RSTN	43	I	VDDSC	Smart*MX* reset input; active low
P31	44	IO	PVDD	General purpose IO signal.Can be configured to act either as TX line of the second serial interface or general purpose IO. In test mode this signal is used as input and output test signal.
P30	45	IO	PVDD	General purpose IO signal.Can be configured to act either as TX line of the second serial interface or general purpose IO. In test mode this signal is used as input and output test signal.
NC2	46			Do not connect
IRQ	47	O	PVDD	Interrupt request: Output to signal an interrupt event to the host (Port 7 bit 0)
RSTOUT	48	IO	PVDD	Output reset signal. When Low it indicates that the circuit is in reset state.

8. Limiting values

Table 4: **Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VSS (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
PV_{DD}, SV_{DD}, TV_{DD}, AV_{DD}, DV_{DD}, V_{BUS}	Supply voltage		-0.5	+4.0	V
V_{DDSC}	Supply voltage		-0.5	+6.0	V
P_{tot}	Total power dissipation per package (V_{BUS} and DV_{DD} in short cut mode)		-	<tbd>	W
I_{TX1}	Maximum current in transmitter TX1		-100	100	mA
I_{TX2}	Maximum current in transmitter TX2		-100	100	mA
T_{stg}	Storage temperature range		-55	150	°C
T_J	Junction temperature range			100	°C
V_{ESD}	Electrostatic discharge voltage on all pins			± 2.0	kV
ESDH	ESD Susceptibility (Human Body model)	1500 Ωm, 100pF; JESD22-A114-B		2	KV
ESDM	ESD Susceptibility (Machine model)	0.75 mH, 200 pF; JESD22-A114-A		200	V

9. Recommended operating conditions

Table 5: **Operating conditions**

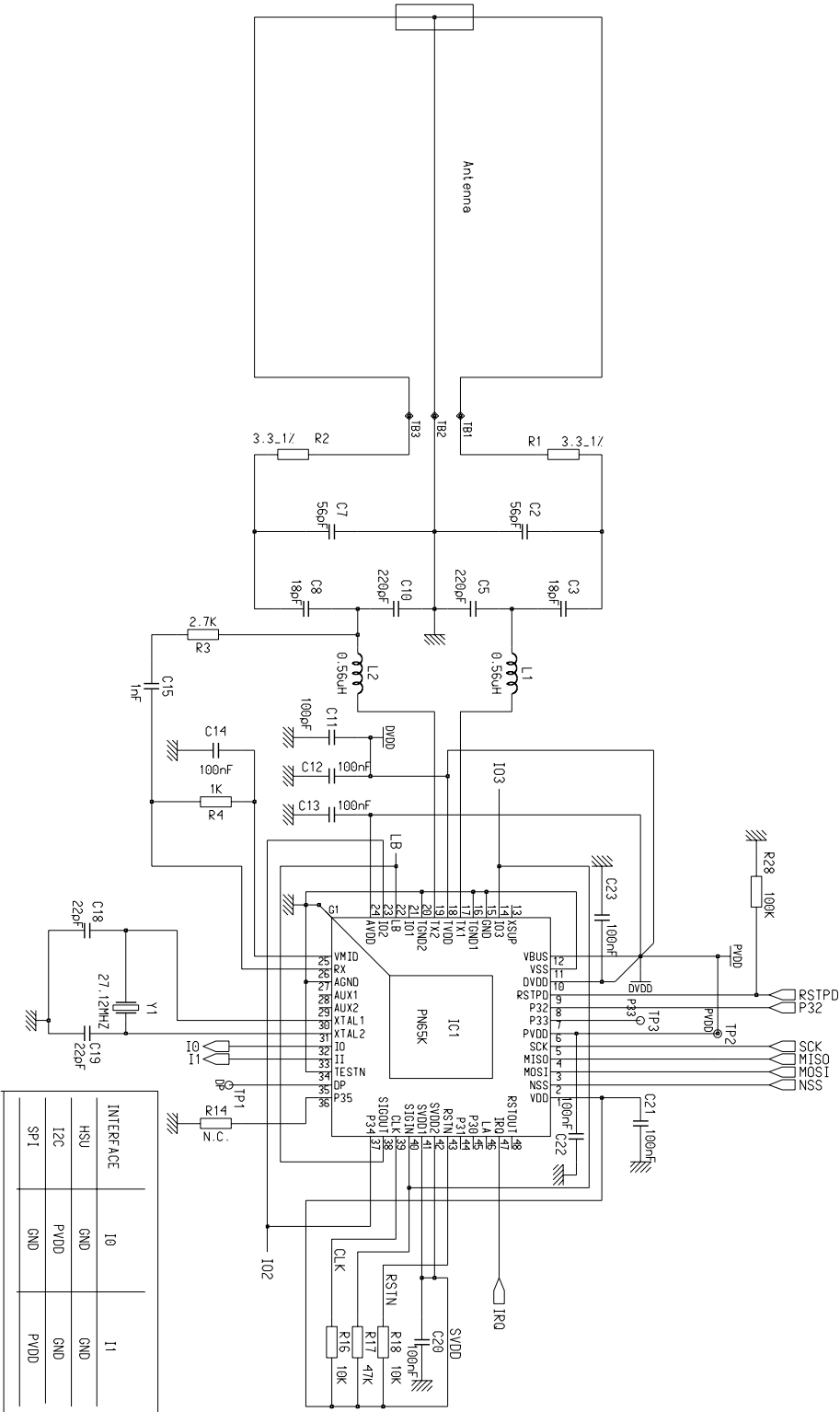| Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TV_{DD}, AV_{DD}, DV_{DD}, V_{BUS}	Supply voltage	$TV_{DD} = AV_{DD} = DV_{DD}$ $V_{SS} = 0$ V	2.5	3.3	3.6	V
PV_{DD}	Supply voltage for host interface	$V_{SS} = 0$ V	1.6	1.8 to 3.3	3.6	V
SV_{DD}, V_{DDSC}	Supply voltage for Smart card device	$V_{SS} = 0$ V Sam_switch_en set to 1	2.4	3.3	3.6	V
T_{amb}	Operating ambient temperature (ISO 7816 or ISO 14443 operation)		-15	+25	+85	°C

10. Application information

Fig 3.   Application diagram of PN65K

11. Package outline

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads;
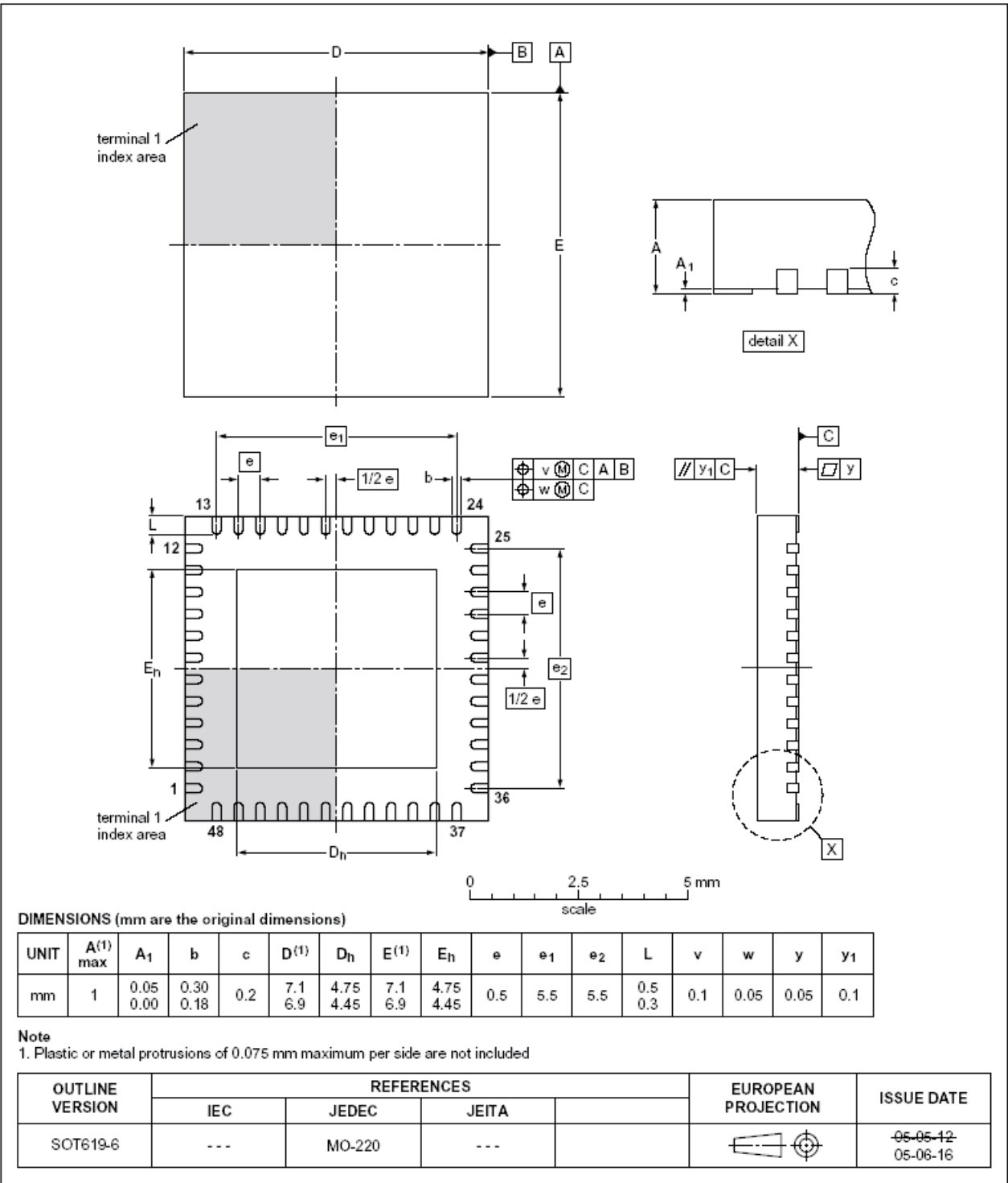48 terminals; body 7 x 7 x 0.85 mm

SOT619-6

terminal 1
index area

detail X

terminal 1
index area

0   2.5   5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	4.75 4.45	7.1 6.9	4.75 4.45	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-6	- - -	MO-220	- - -			05-05-12 05-06-16

Fig 4.   Package outline SOT619-6 (HVQFN48)

12. References

For technical information see separate documents:

- "Data Sheet P5CN072, Secure Dual Interface PKI Smart Card Controller,

- "Data Sheet PN531_C2, Near Field Communication Controller,

13. Revision history

Table 6.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
111113	20 October 2006	Objective short data sheet		Revision 1.2
Modifications:	<td colspan="4">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 4 "Quick reference data" on page 4: added new Section • Section 11 "Package outline" on page 11: update of package drawing</td>

14. Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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