Mosway Technologies Ltd.

PN7103

Half-Bridge Driver

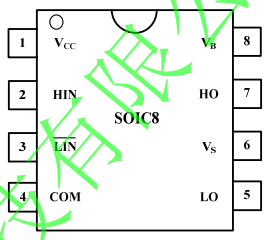
General Description

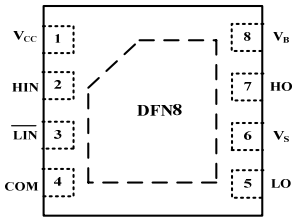
The PN7103 is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT in a half-bridge configuration which operates up to 600 V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

Features

- Fully operational to +600 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for low side channel
- Output Source / Sink Current Capability 300 mA / 600mA
- -5V negative Vs ability
- Matched propagation delay for both channels

Packages/Order information



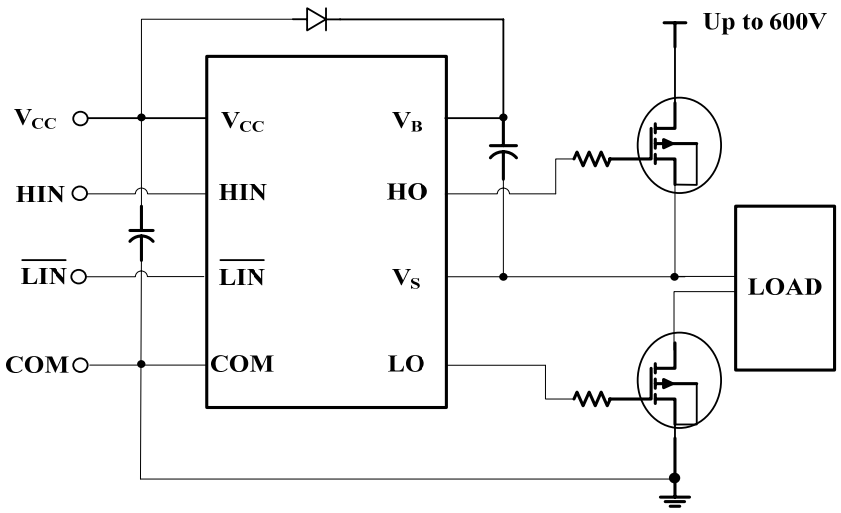


Part number	Order Code	Package
PN7103	**PN7103SEC-R1**	**SOIC8**
PN7103	**PN7103DEC-R1**	**DFN8**

Applications

- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Half-Bridge Power Converters
- Full-Bridge Power Converters

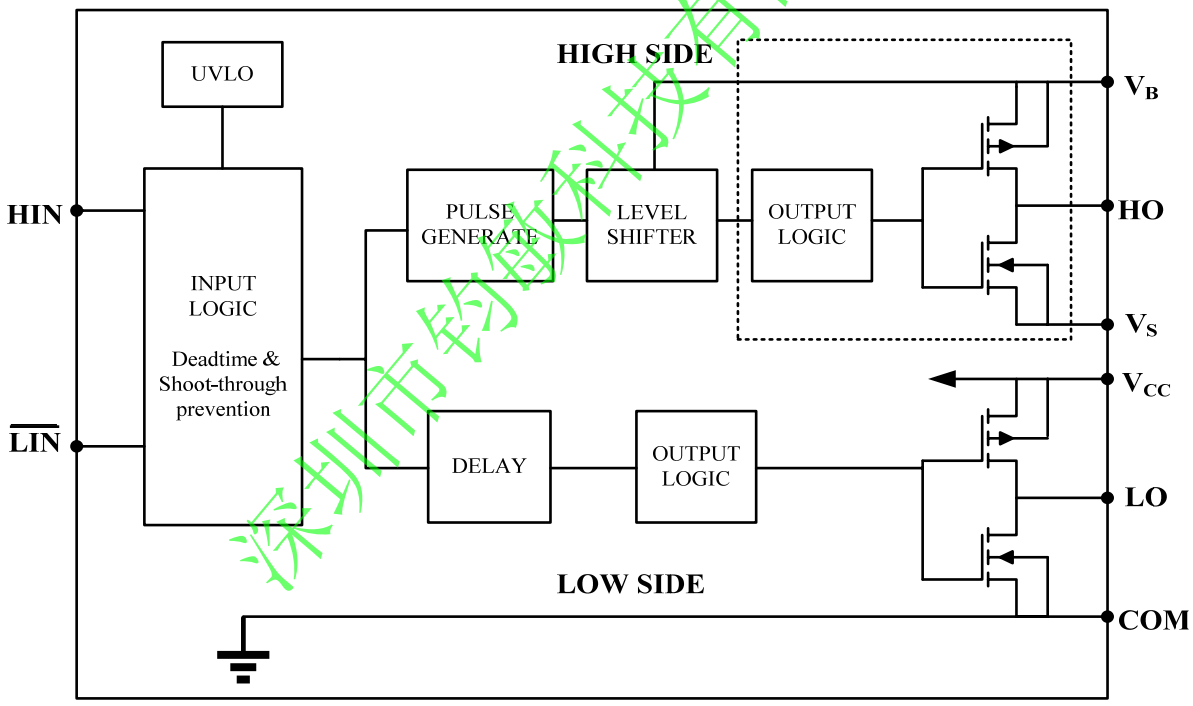
Typical Application Circuit



Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	V_{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	$\overline{LIN}$	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output, out of phase with $\overline{LIN}$
6	V_S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V_B	High side floating supply

Functional Block Diagram



Absolute Maximum Ratings [Note1]

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	622	V
V_S	High side floating supply return		V_B - 22	V_B + 0.3	
V_{HO}	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	22	
V_{LO}	Low side gate drive output		-0.3	VCC + 0.3	
V_{IN}	Logic input of HIN & $\overline{LIN}$		-0.3	VCC + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		--	50	V/ns
ESD	HBM Model		2.5		kV
	Machine Model		200		V
P_D	Package Power Dissipation @ TA ≤25°C	8 Lead SOIC	--	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	8 Lead SOIC	--	200	°C /W
T_J	Junction Temperature		--	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		--	300	

Note 1: Exceeding these ratings may damage the device.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	-	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	VCC	
V_{IN}	Logic input voltage(HIN & $\overline{LIN}$)	0	VCC	
T_A	Ambient temperature	-40	125	℃

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

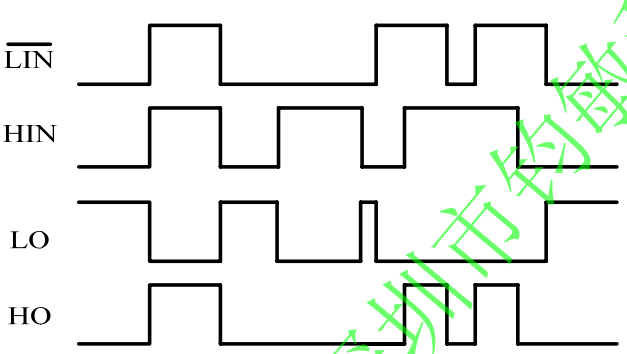
Symbol	Definition	TYP.	MAX.	Units
t_{onH}	High side turn-on propagation delay	630	820	ns
t_{offH}	High side turn-off propagation delay	140	220	
t_{onL}	Low side turn-on propagation delay	630	820	
t_{offL}	Low side turn-off propagation delay	140	220	
MT	Delay matching	-	50	
DT	Dead time	500	650	
t_r	Turn-on rise time	85	120	
t_f	Turn-off fall time	35	90	

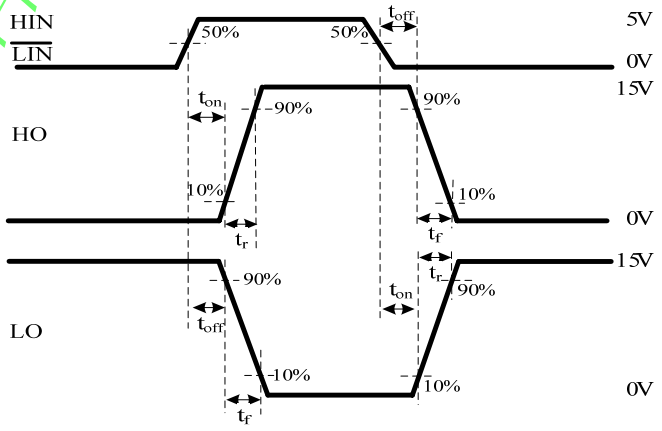
Static Electrical Characteristics

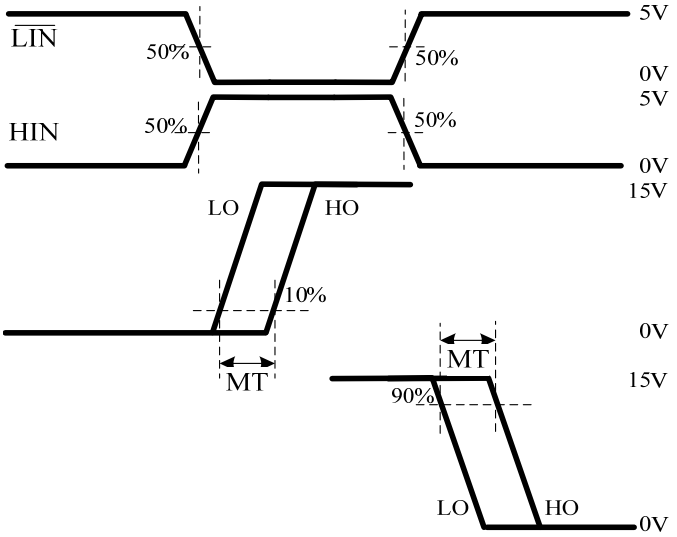
V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

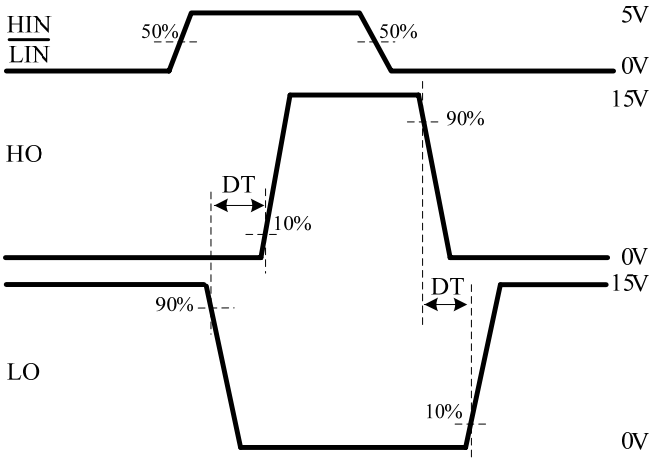
Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic "1"(HIN) & Logic "0"($\overline{LIN}$) input voltage	2.5	-	-	V
V_{IL}	Logic "0" (HIN)& Logic "1"($\overline{LIN}$) input voltage	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	-	-	0.1	
V_{OL}	Low level output voltage, V_O	-	-	0.1	
I_{QCC}	Quiescent V_{CC} supply current	-	150	270	µA
I_{QBS}	Quiescent V_B supply current	-	30	55	
I_{LK}	Leakage current from V_S(600V) to GND		-	10	
I_{IN+}	Logic "1" input bias current (HIN "1" & $\overline{LIN}$ "0")	-	6	20	
I_{IN-}	Logic "0" input bias current (HIN "0" & $\overline{LIN}$ "1")	-		15	
V_{CCU+}	V_{CC} supply UVLO threshold	-	8.7	-	V
V_{CCU-}		-	8	-	
I_{O+}	Output high short circuit pulsed current	--	300	--	mA
I_{O-}	Output low short circuit pulsed current	--	600	--	

Logic Function & Timing Spec









Characterization Curves

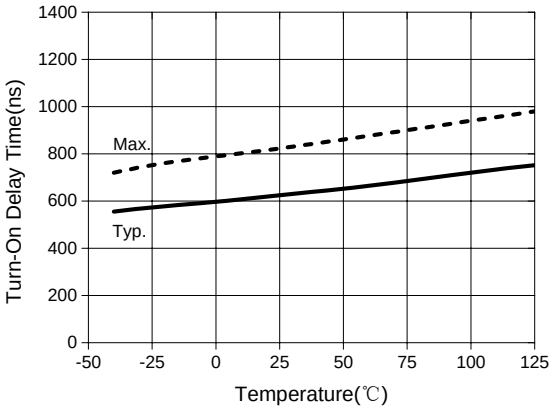


Fig.1 Turn-On Delay vs. Temperature

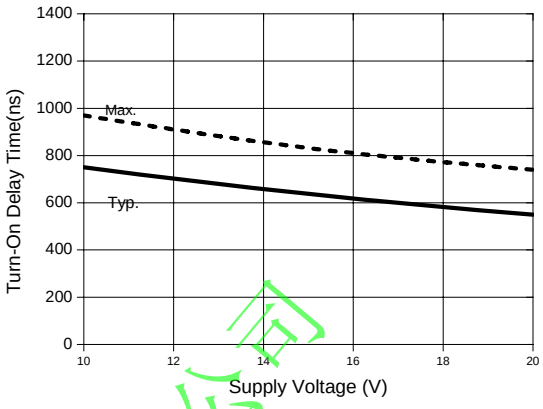


Fig.2 Turn-On Delay vs. Supply Voltage

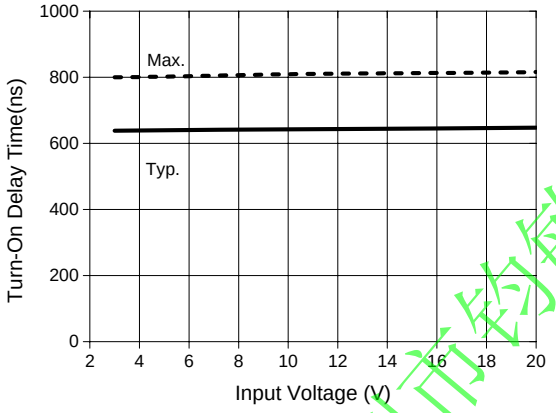


Fig.3 Turn-On Delay Time vs. Input Voltage

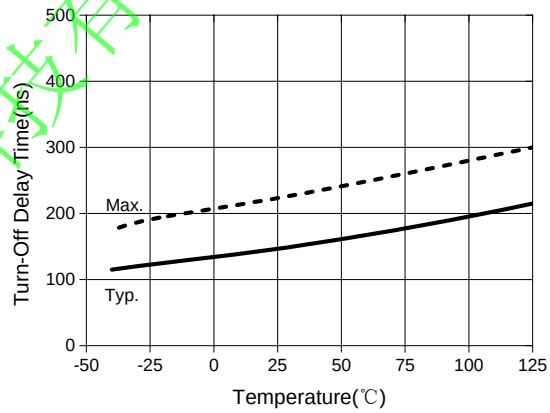


Fig.4 Turn-Off Delay Time vs. Temperature

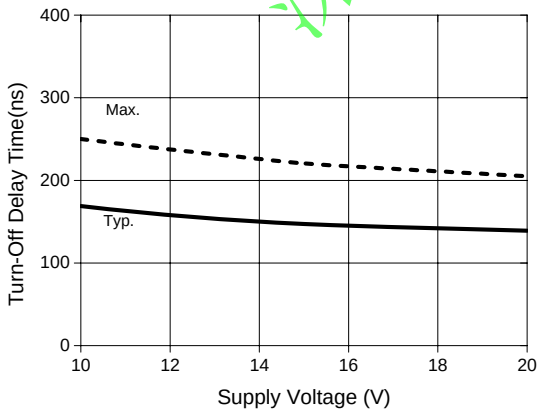


Fig.5 Turn-Off Delay Time vs. Supply Voltage

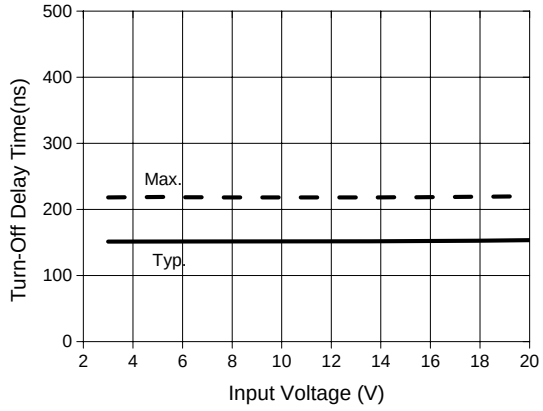


Fig.6 Turn-Off Delay Time vs. Input Voltage

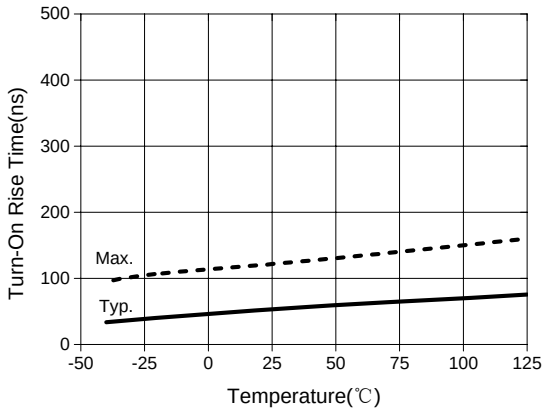


Fig.7 Turn-On Rise Time vs. Temperature

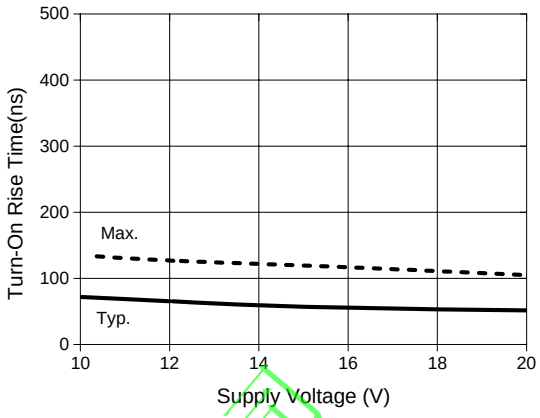


Fig.8 Turn-On Rise Time vs. Supply Voltage

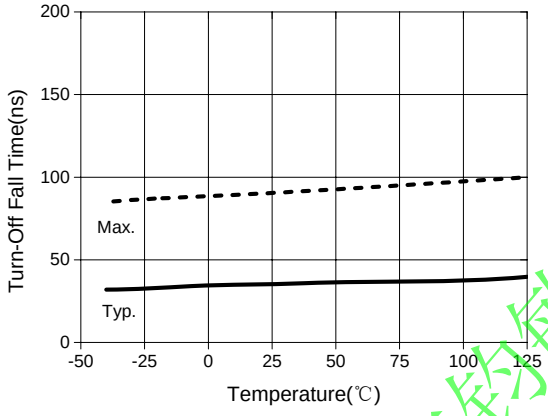


Fig.9 Turn-Off Fall Time vs. Temperature

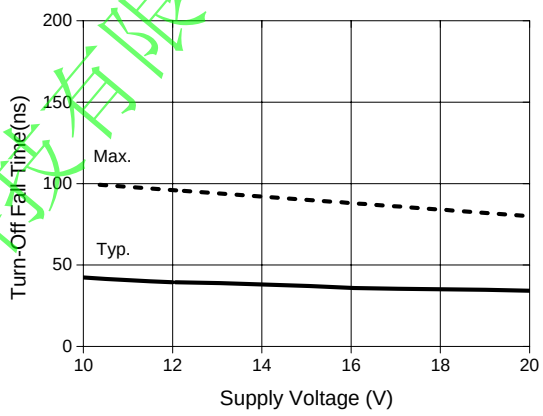


Fig.10 Turn-Off Fall Time vs. Supply Voltage

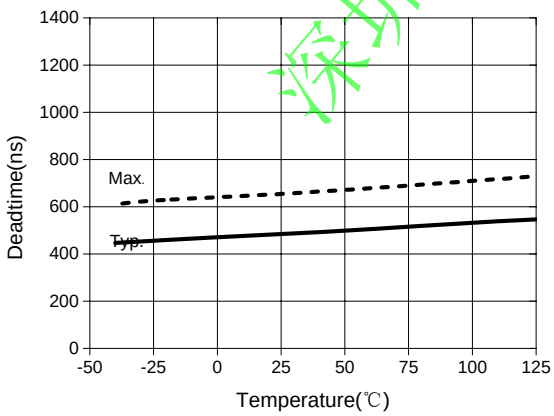


Fig.11 Dead time vs. Temperature

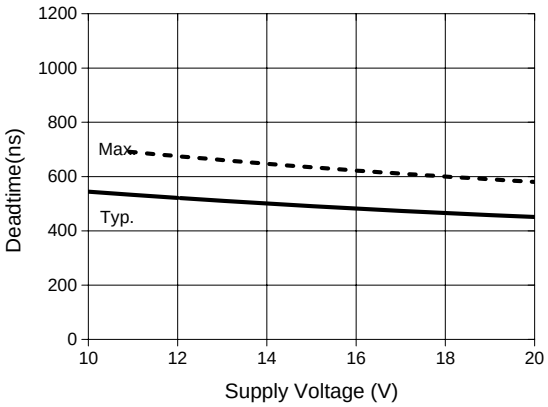


Fig.12 Dead time vs. Supply Voltage

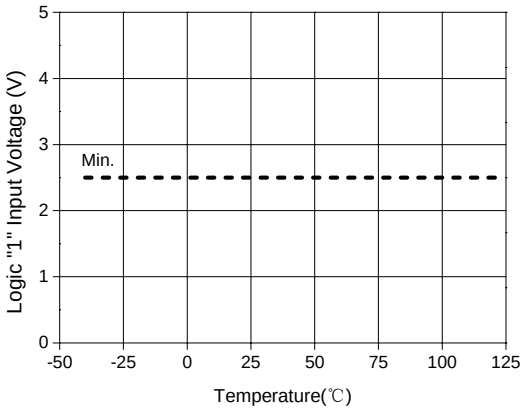


Fig.13 Logic "1" Input Voltage vs. Temperature

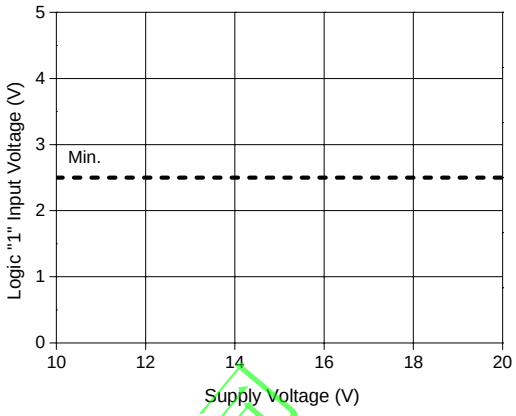


Fig.14 Logic "1" Input Voltage vs. Supply Voltage

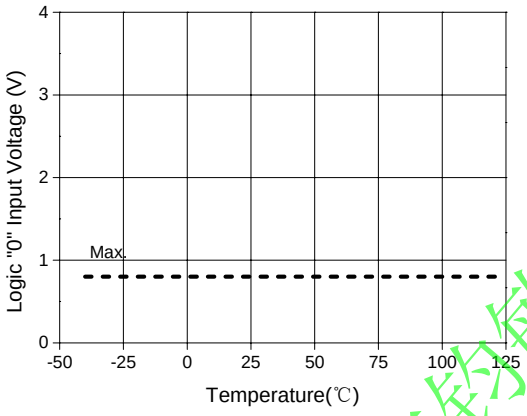


Fig.15 Logic "0" Input Voltage vs. Temperature

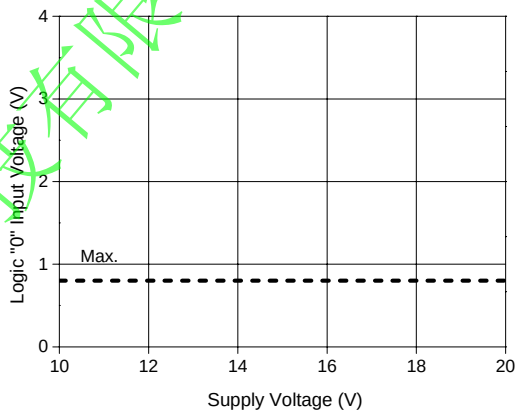


Fig.16 Logic "0" Input Voltage vs. Supply Voltage

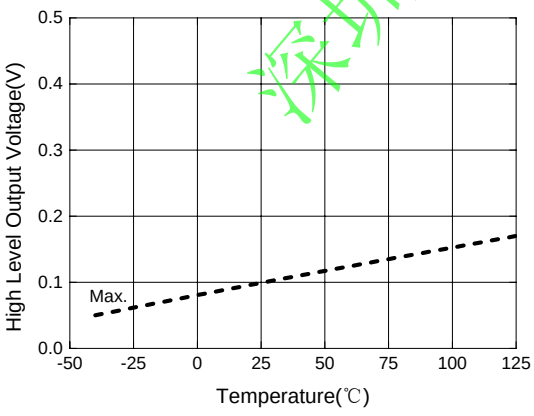


Fig.17 High Level Output vs. Temperature

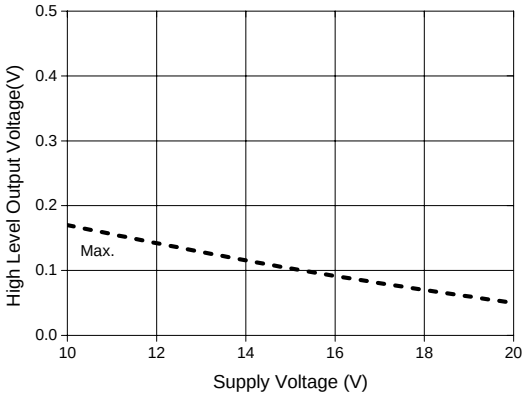


Fig.18 High Level Output vs. Supply Voltage

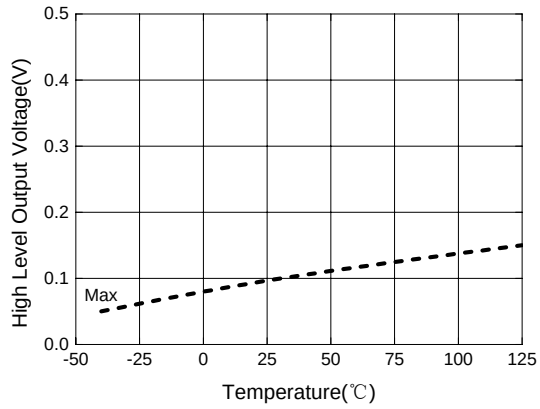


Fig.19 Low Level Output vs. Temperature

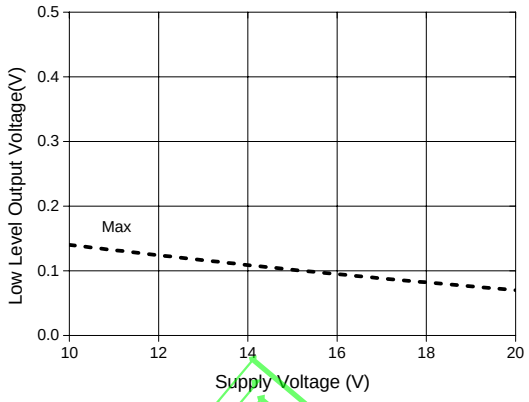


Fig.20 Low Level Output vs. Supply Voltage

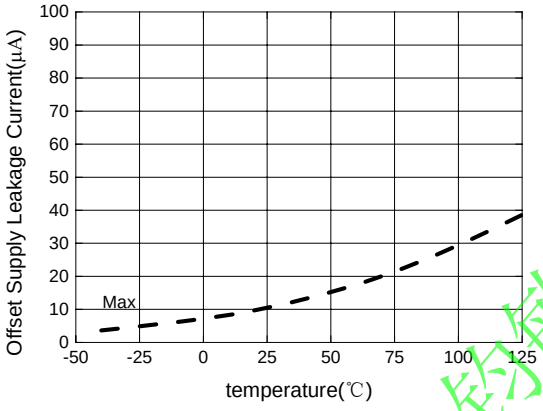


Fig.21 Offset Supply Current vs. Temperature

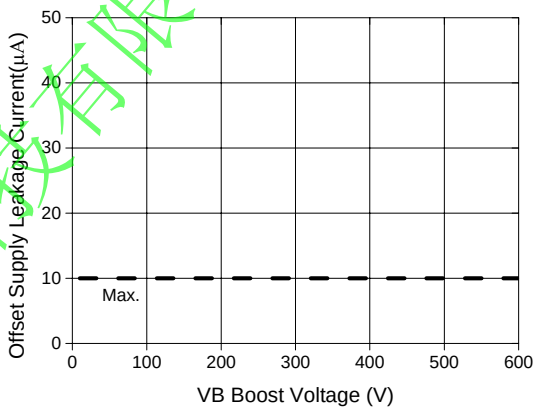


Fig.22 Offset Supply Current vs. Boost Voltage

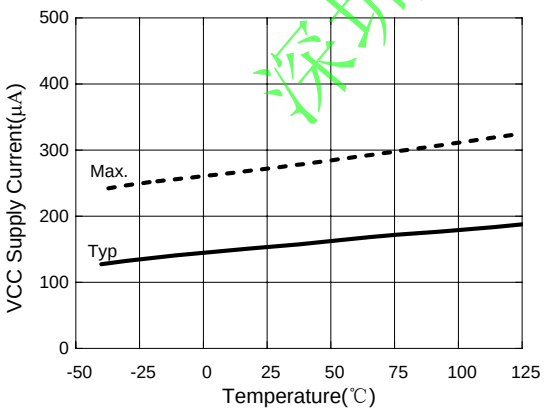


Fig.23 VCC Supply Current vs. Temperature

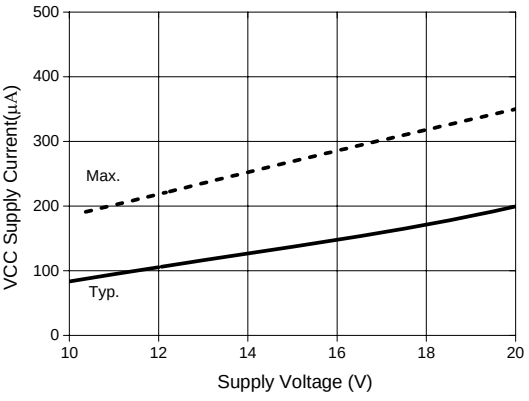


Fig.24 VCC Supply Current vs. Supply Voltage

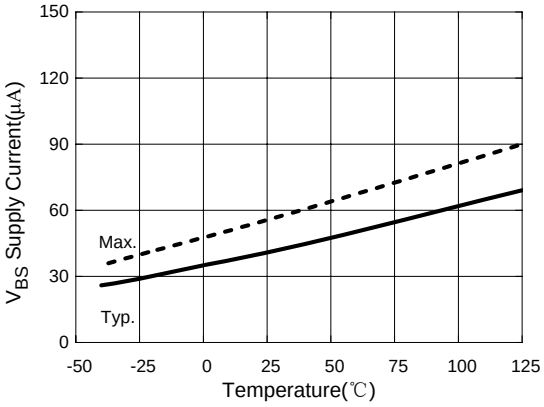


Fig.25 VBS Supply Current vs. Temperature

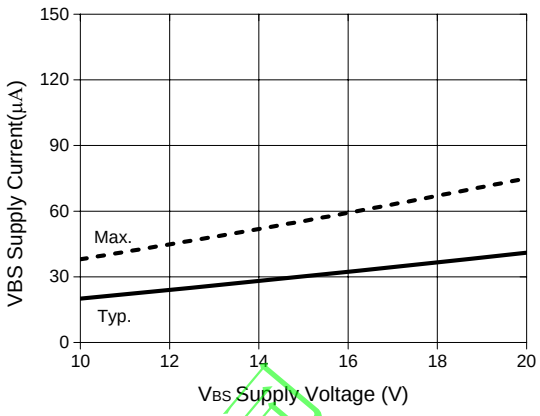


Fig.26 VBS Supply Current vs. Supply Voltage

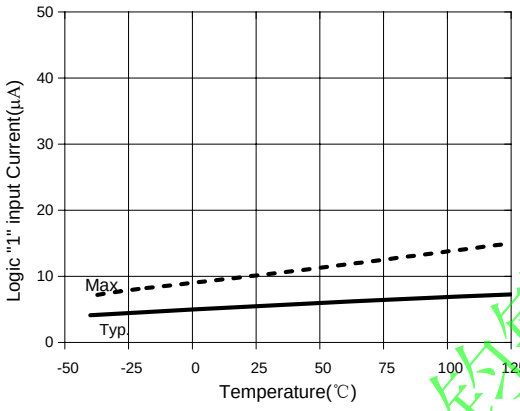


Fig.27 Logic "1" Input Current vs. Temperature

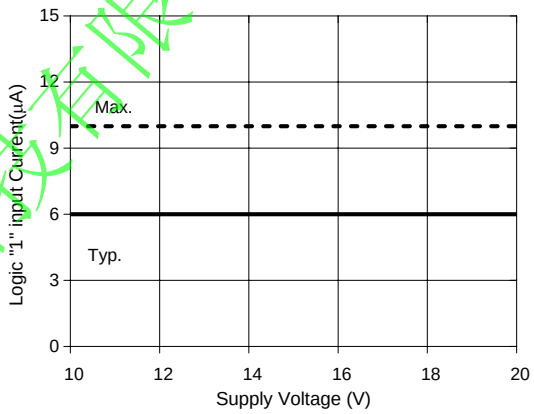


Fig.28 Logic "1" Input Current vs. Supply Voltage

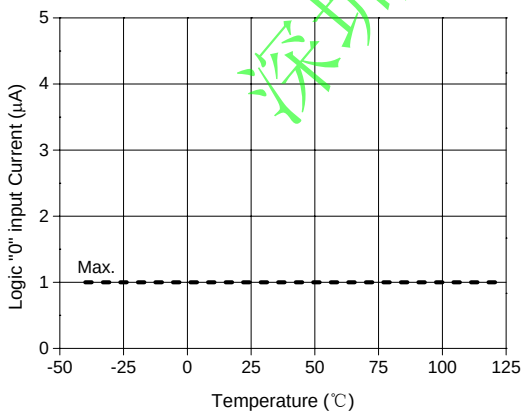


Fig.29 Logic "0" Input Current vs. Temperature

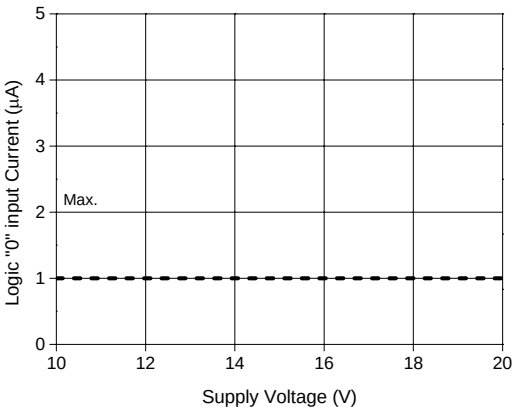


Fig.30 Logic "0" Input Current vs. Supply Voltage

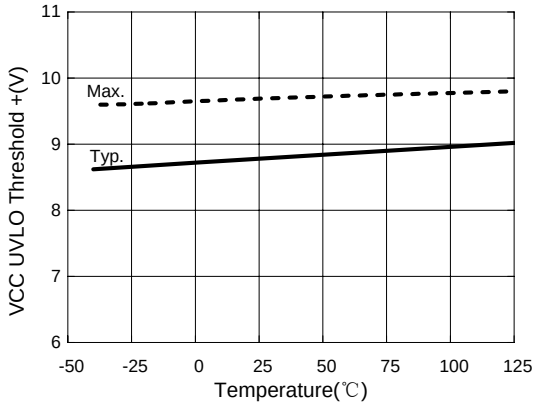


Fig.31 VCC Under voltage Threshold(+) vs. Temperature

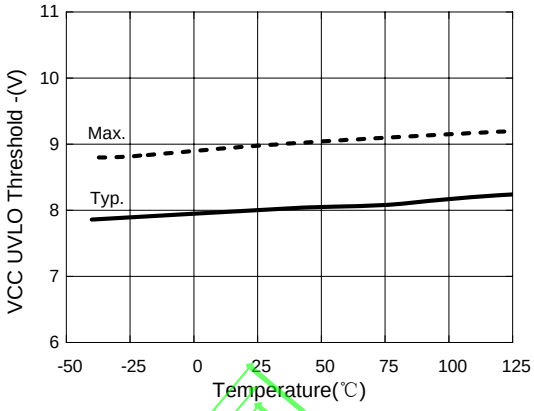


Fig.32 VCC Under voltage Threshold(-) vs. Temperature

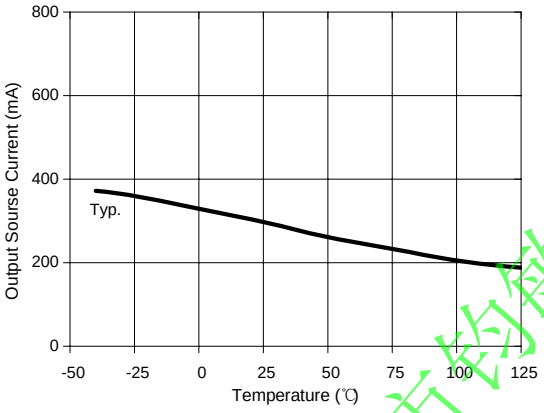


Fig.33 Output Source Current vs. Temperature

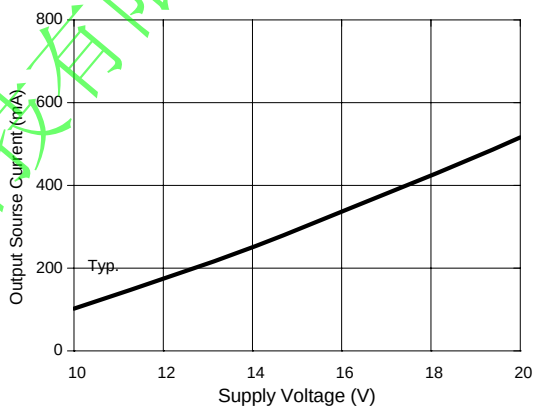


Fig.34 Output Source Current vs. Supply Voltage

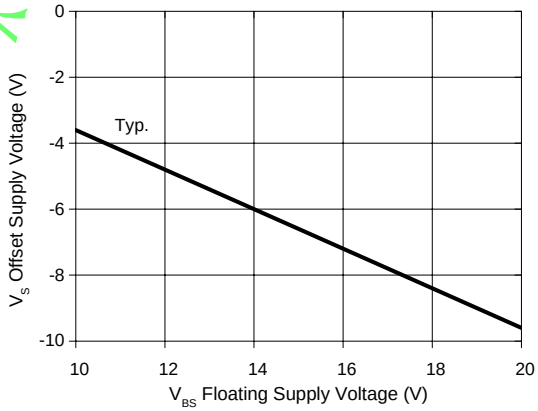


Fig.35 Maximum V_S Negative Offset vs. Supply Voltage

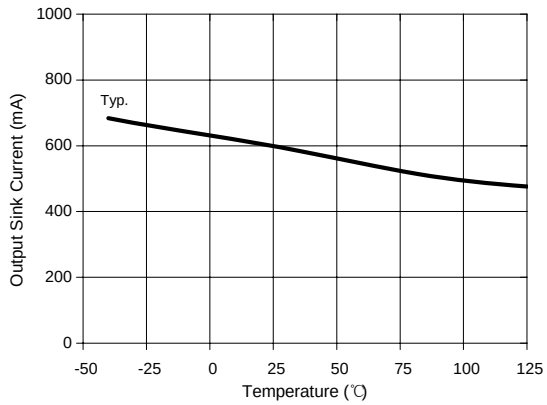


Fig.36 Output Sink Current vs. Temperature

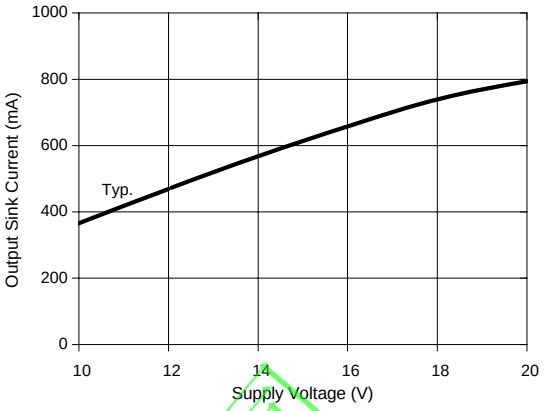


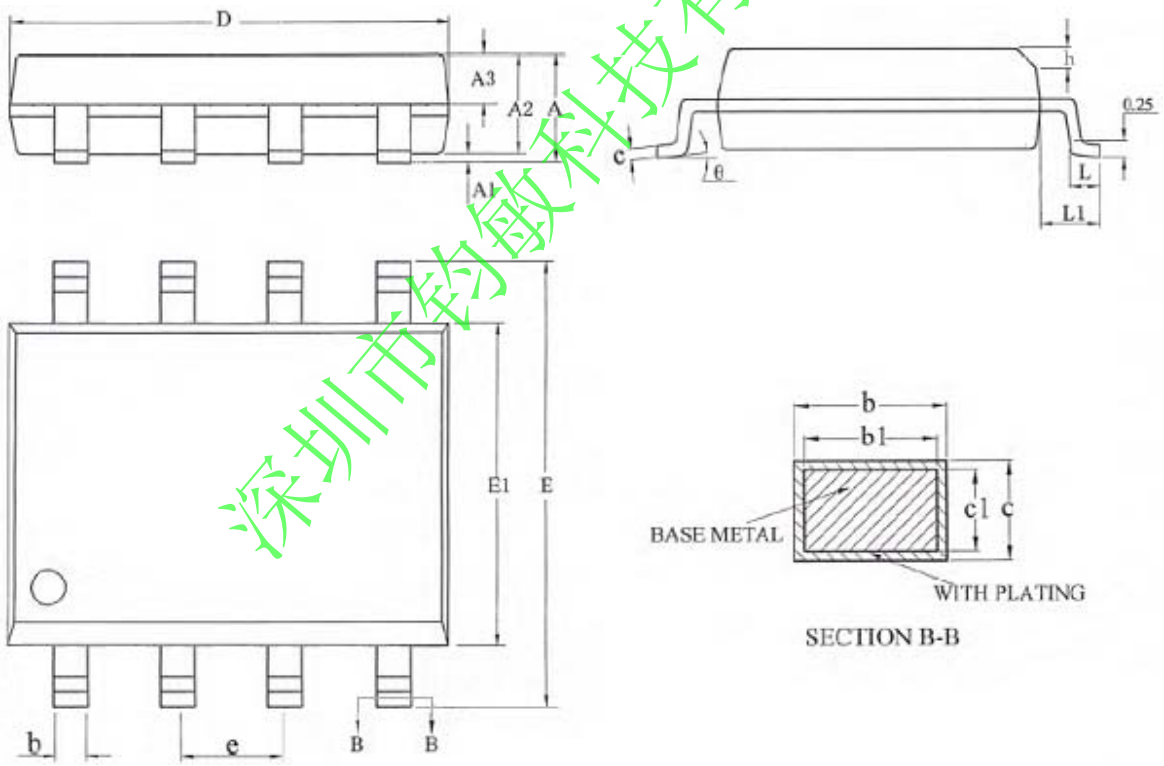
Fig.37 Output Sink Current vs. Supply Voltage

Package Information

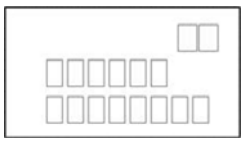
SOIC8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1		1.05BSC	
c1	0.19	0.20	0.21	θ	0	-	8°

Package Outlines



SOIC8 Package Mark Information



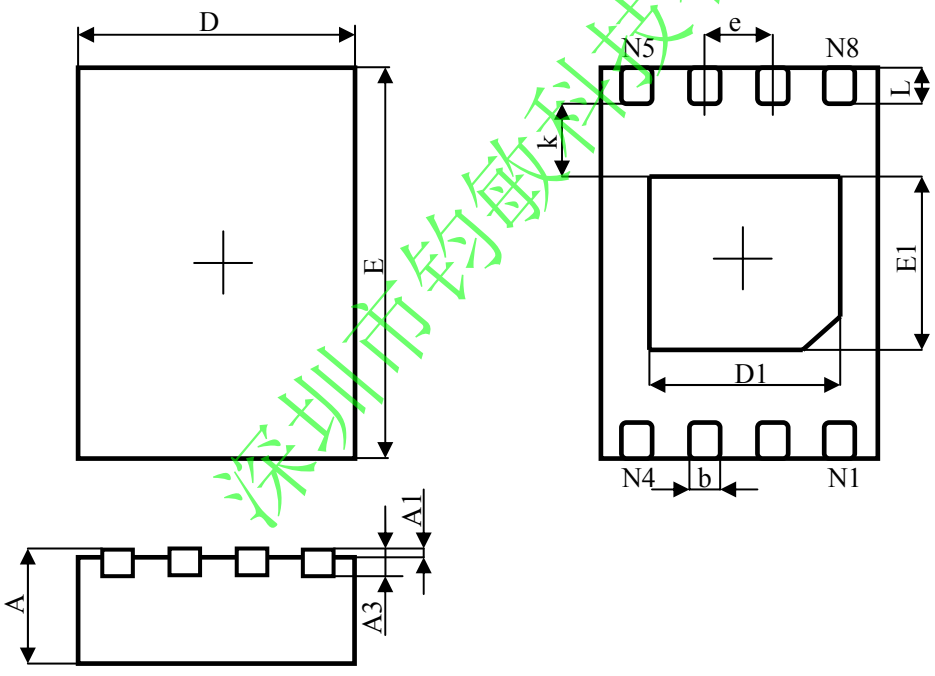
TOP Mark
Logo
PN7103
YWWXXXXX[Note]

Note：Y：Year code，WW：Week codes，XXXXX：Package codes

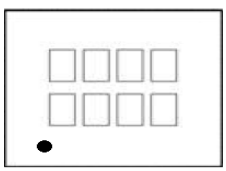
DFN8 Package Dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

Package Outlines



DFN8 Package Mark Information



TOP Mark
7103
AYWX[Note]
Pin 1 indicator point

Note：A：Internal code，Y：Year code，W：Week codes， X：Package codes

Important Notice

Mosway Technologies Ltd. reserves the right to make changes without further notice to any products or specifications herein. Mosway Technologies Ltd. does not assume any responsibility for use of any its products for any particular purpose, nor does Mosway Technologies Ltd assume any liability arising out of the application or use of any its products or circuits. Mosway Technologies Ltd does not convey any license under its patent rights or other rights nor the rights of others.