Mosway Technologies Ltd.

PN7106

High and Low Side Driver

General Description

The PN7106A/B is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT in a half-bridge configuration (version B) or any other high-side& low-side configuration (version A) which operates up to 600V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

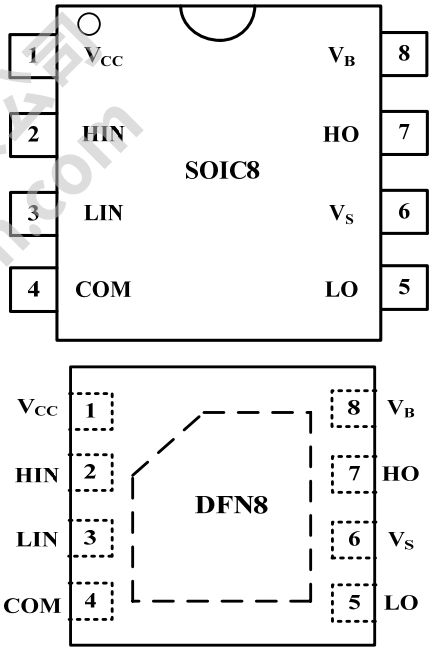
Features

- Fully operational to +600 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/nsec
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for both channels
- Output Source / Sink Current Capability 400mA / 800mA
- Independent Logic Inputs to Accommodate All Topologies (Version A)
- Cross Conduction Protection with 180 ns Internal Fixed Dead Time (Version B)
- -5V negative Vs ability
- Matched propagation delay for both channels

Applications

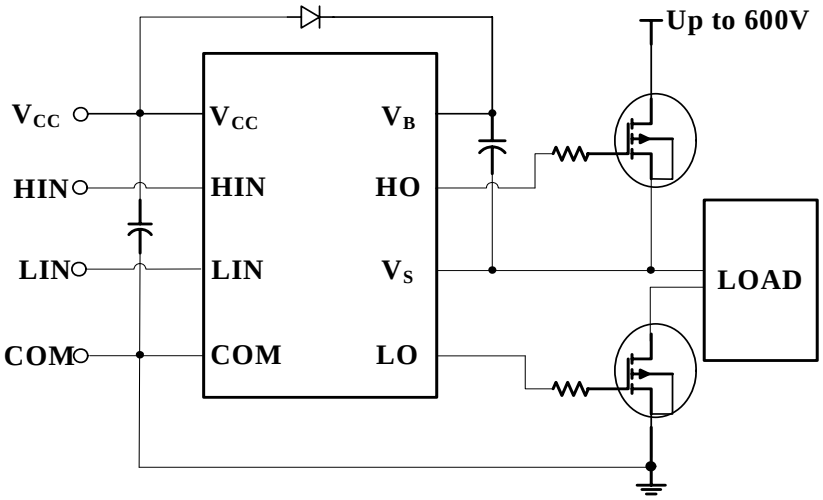
- Small and medium- power motor driver
- Power MOSFET or IGBT driver
- Lighting ballast
- Half−Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Drive Converters (Asymmetrical Half−Bridge, Active Clamp) (A Version Only)

Package/Order information



Part number	Order Code	Package
PN7106A	PN7106ASEC-R1	SOIC8
	PN7106BSEC-R1	SOIC8
PN7106B	PN7106ADEC-R1	DFN8
	PN7106BDEC-R1	DFN8

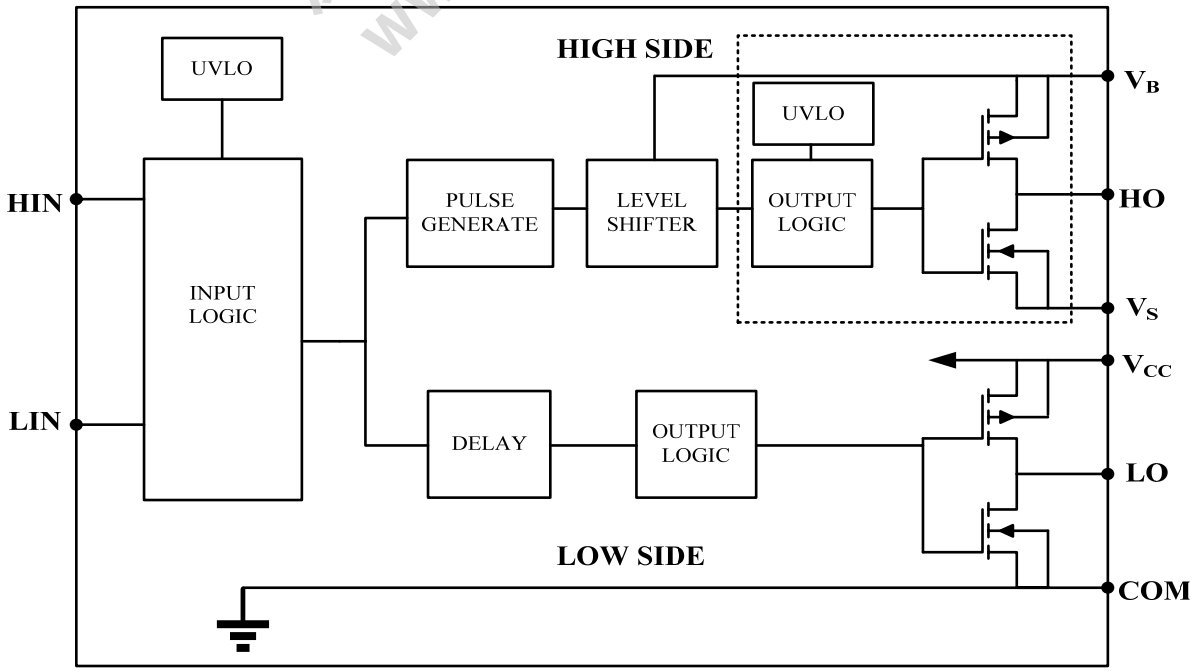
Typical Application Circuit



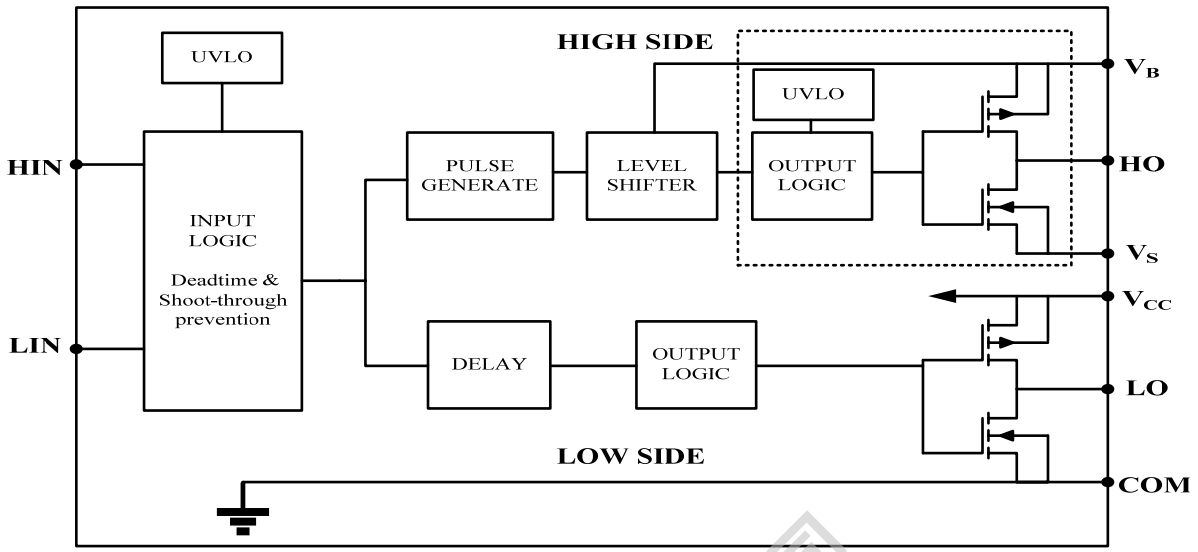
Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	V_{CC}	Low side and main power supply
2	HIN	Logic input for high side gate driver output (HO)
3	LIN	Logic input for low side gate driver output (LO)
4	COM	Ground
5	LO	Low side gate drive output, in phase with LIN
6	V_S	High side floating supply return or bootstrap return
7	HO	High side gate drive output, in phase with HIN
8	V_B	High side floating supply

Functional Block Diagram



Detailed Block Diagram: Version A



Detailed Block Diagram: Version B

Absolute Maximum Ratings [Note1]

Symbol	Definition		MIN.	MAX.	Units
V_B	High side floating supply		-0.3	622	V
V_S	High side floating supply return		V_B - 25	V_B + 0.3	
V_{HO}	High side gate drive output		V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply		-0.3	22	
V_{LO}	Low side gate drive output		-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN and LIN		-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		--	50	V/ns
ESD	HBM Model		2.5		kV
	Machine Model		200		V
P_D	Package Power Dissipation @ TA ≤25°C	8 Lead SOIC	--	0.625	W
Rth_{JA}	Thermal Resistance Junction to Ambient	8 Lead SOIC	--	200	°C /W
T_J	Junction Temperature		--	150	°C
T_S	Storage Temperature		-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		--	300	

Note 1: Exceeding these ratings may damage the device.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S +10	V_S +20	V
V_S	High side floating supply return	-	600	
V_{HO}	High side gate drive output voltage	V_S	V_B	
V_{CC}	Low side supply	10	20	
V_{LO}	Low side gate drive output voltage	0	V_{CC}	
V_{IN}	Logic input voltage(HIN & LIN)	0	V_{CC}	
T_A	Ambient temperature	-40	125	

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

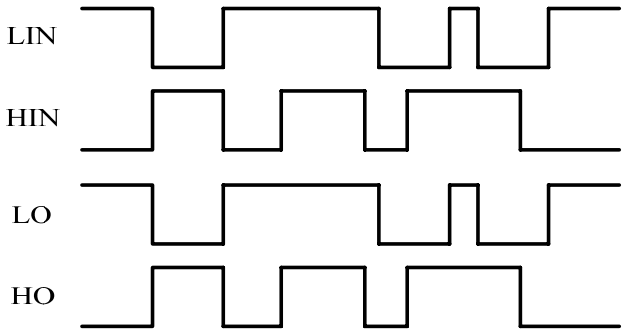
Symbol	Definition	TYP.	MAX.	Units
t_{onH}	High side turn-on propagation delay	160	220	ns
t_{offH}	High side turn-off propagation delay	150	220	
t_{onL}	Low side turn-on propagation delay	160	220	
t_{offL}	Low side turn-off propagation delay	150	220	
MT	Delay matching	20	50	
DT	Dead time (only valid for B version)	180	250	
t_r	Turn-on rise time	60	120	
t_f	Turn-off fall time	50	100	

Static Electrical Characteristics

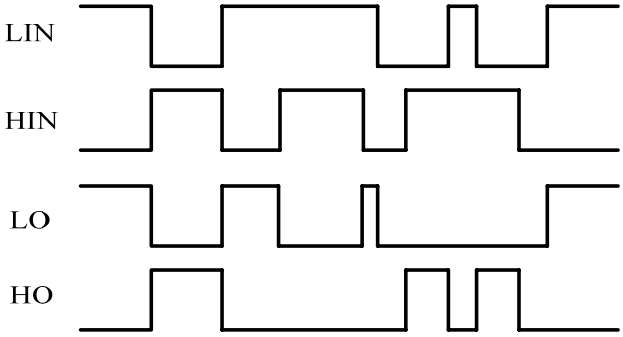
V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic "1"(HIN & LIN) input voltage	2.5	-	-	V
V_{IL}	Logic "0" (HIN & LIN) input voltage	-	-	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	-	-	0.3	
V_{OL}	Low level output voltage, V_O	-	-	0.3	
I_{QCC}	Quiescent V_{CC} supply current	-	200	300	µA
I_{QBS}	Quiescent V_B supply current	-	50	100	
I_{LK}	Leakage current from V_S(600V) to GND		-	10	
I_{IN+}	Logic "1" input bias current	-	6	10	
I_{IN-}	Logic "0" input bias current	-	-	1	
V_{BSU+}	V_{BS} supply UVLO threshold	-	8.7	-	V
V_{BSU-}		-	8	-	
V_{CCU+}	V_{CC} supply UVLO threshold	-	8.7	-	
V_{CCU-}		-	8	-	
I_{O+}	Output high short circuit pulsed current		400		mA
I_{O-}	Output low short circuit pulsed current		800		

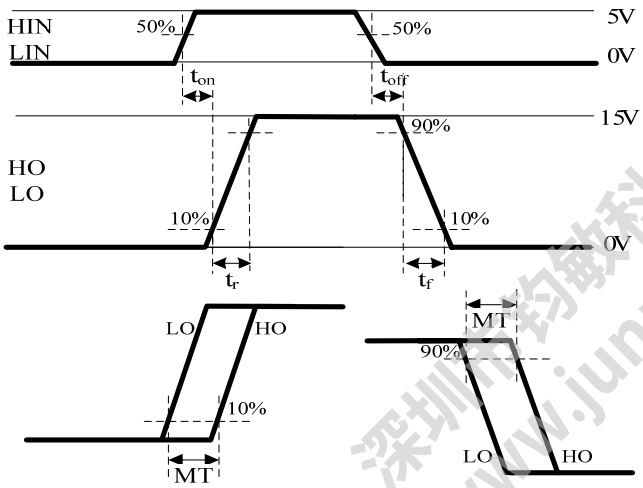
Logic Function & Timing Spec

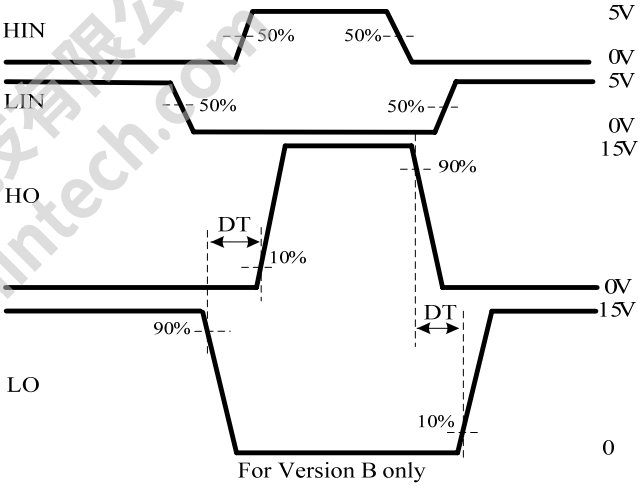


Version A



Version B





For Version B only

Characterization Curves

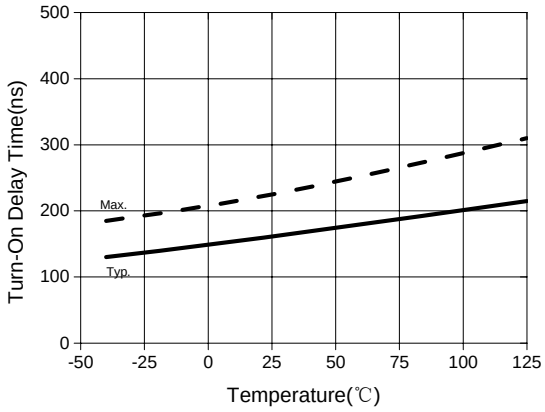


Fig1 Turn-On Delay vs. Temperature

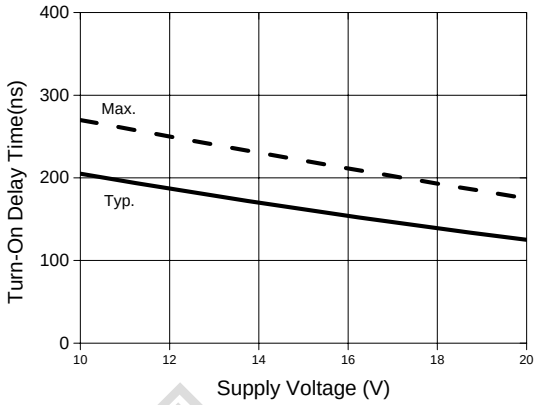


Fig2 Turn-On Delay vs. Voltage

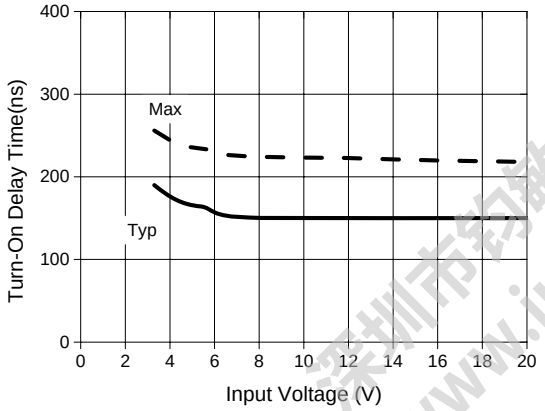


Fig3 Turn-On Delay Time vs. Input Voltage

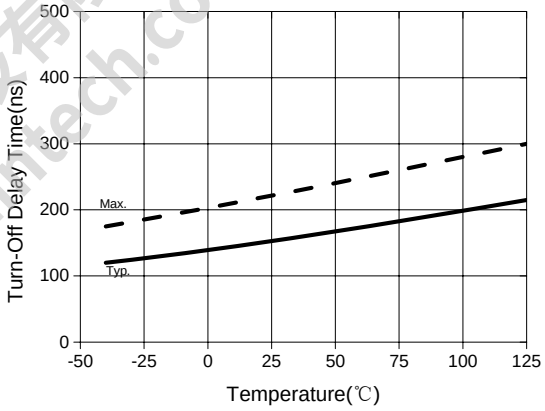


Fig4 Turn-Off Delay Time vs. Temperature

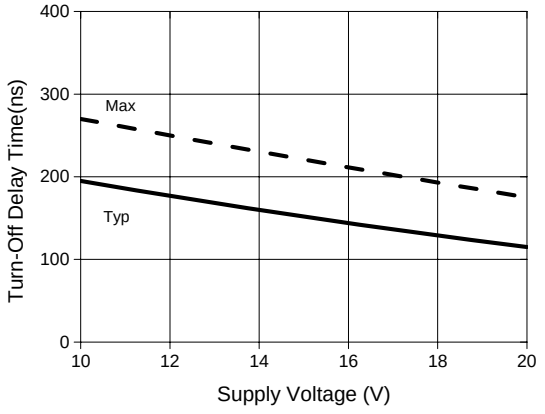


Fig5 Turn-Off Delay Time vs. Supply Voltage

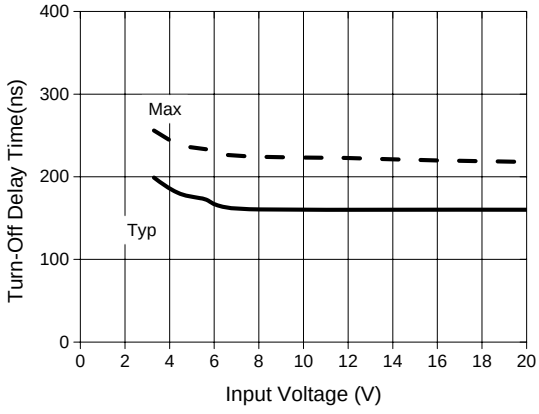


Fig6 Turn-Off Delay Time vs. Input Voltage

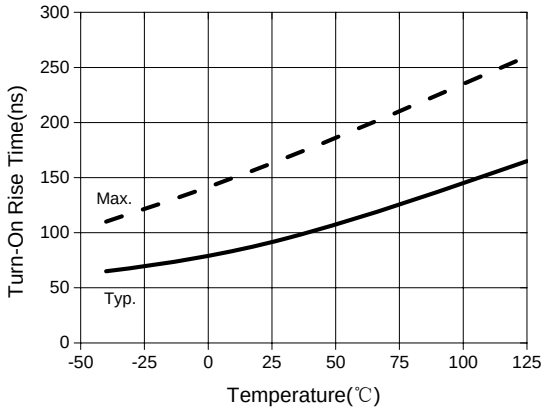


Fig7 Turn-On Rise Time vs. Temperature

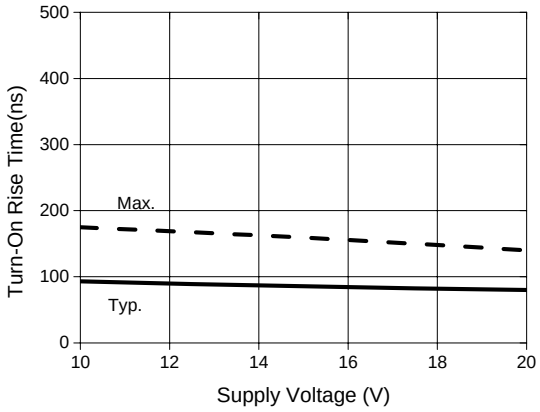


Fig8 Turn-On Rise Time vs. Voltage

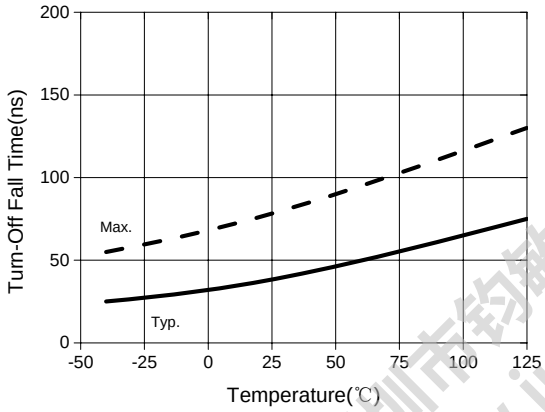


Fig9 Turn-Off Fall Time vs. Temperature

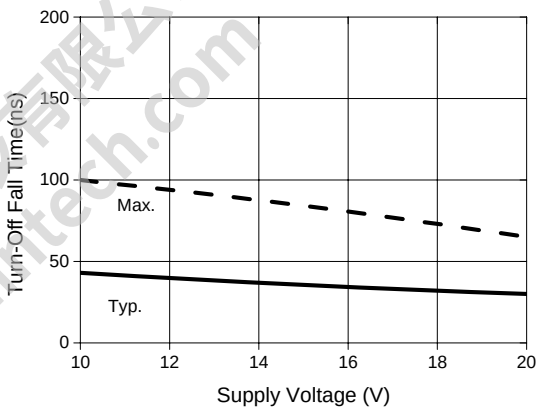


Fig10 Turn-Off Fall Time vs. Voltage

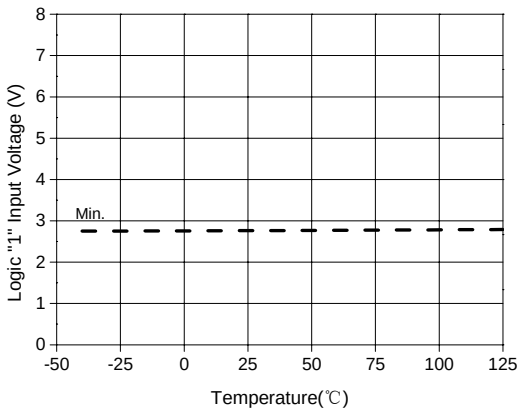


Fig.11 Logic "1" Input Voltage vs. Temperature

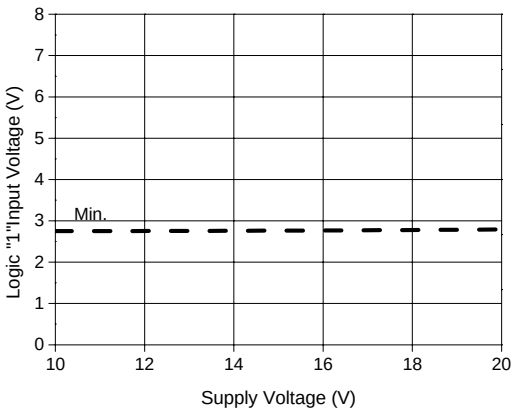


Fig.12 Logic "1" Input Voltage vs. Voltage

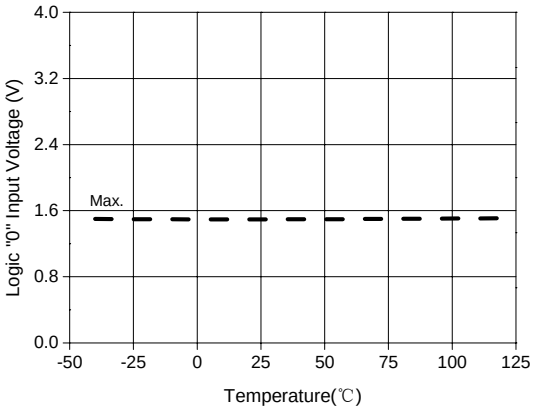


Fig.13 Logic "0" Input Voltage vs. Temperature

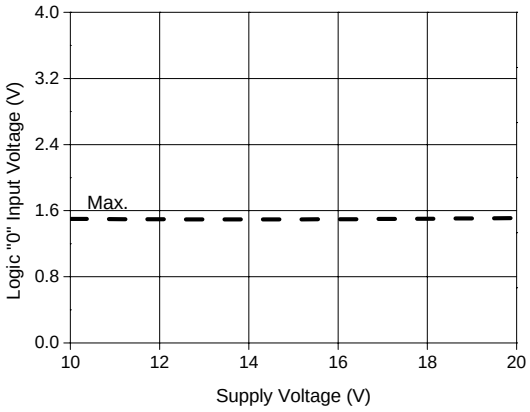


Fig.14 Logic "0" Input Voltage vs. Voltage

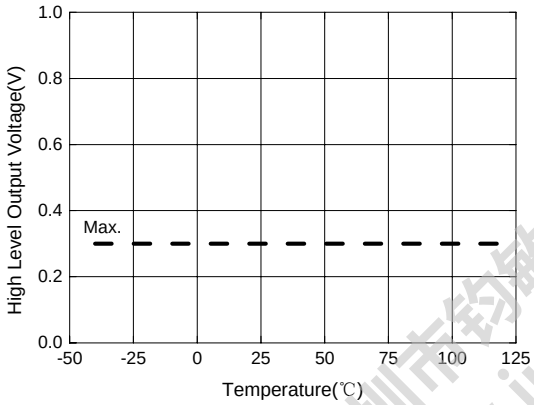


Fig15 High Level Output vs. Temperature

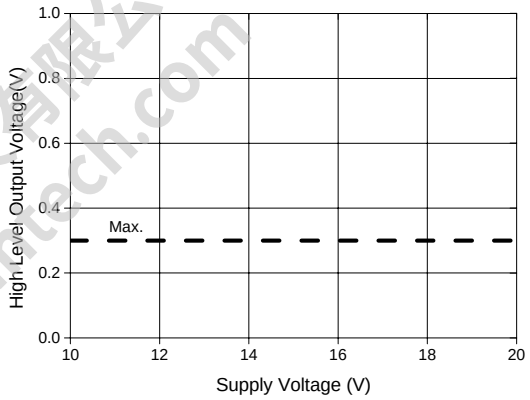


Fig16 High Level Output vs. Voltage

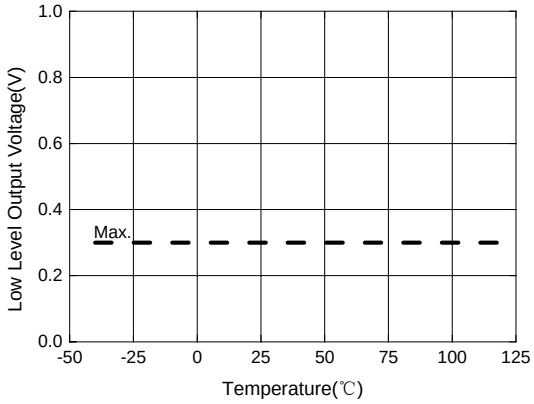


Fig17 Low Level Output vs. Temperature

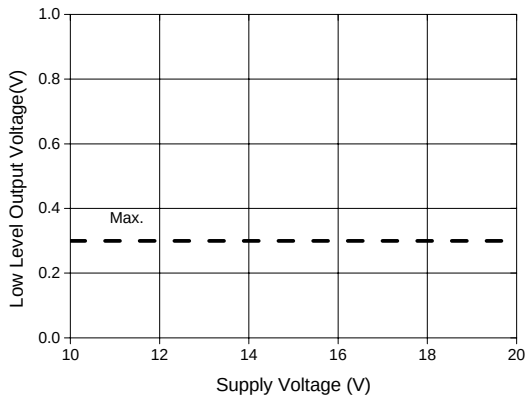


Fig18 Low Level Output vs. Voltage

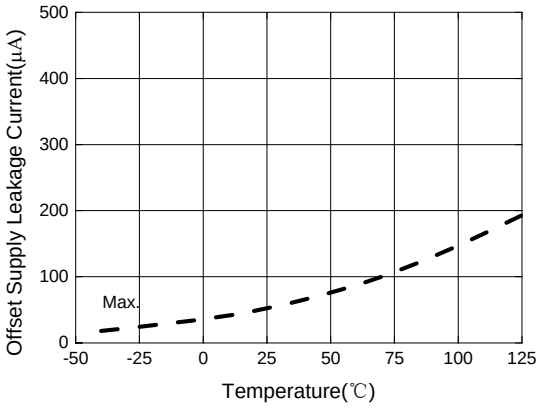


Fig19 Offset Supply Current vs. Temperature

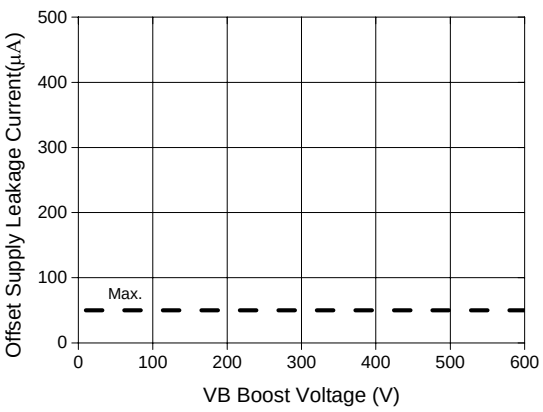


Fig20 Offset Supply Current vs. Voltage

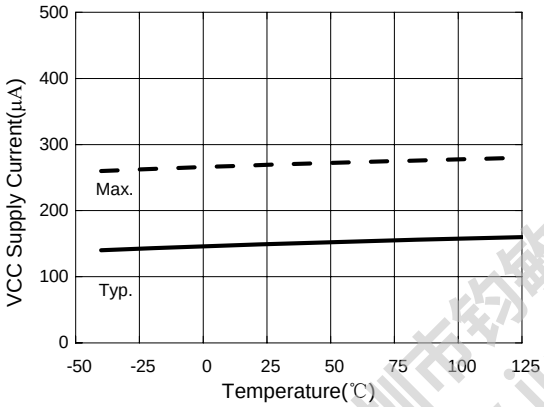


Fig21 VCC Supply Current vs. Temperature

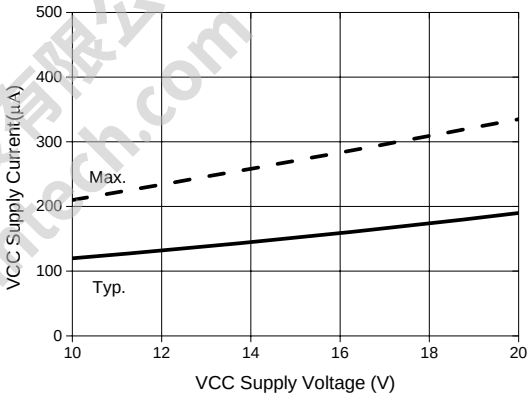


Fig22 VCC Supply Current vs. Voltage

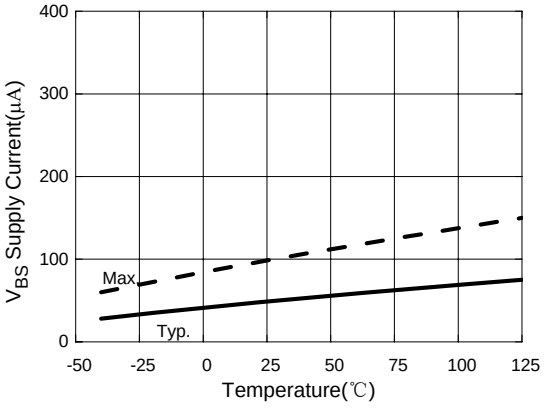


Fig23 VBS Supply Current vs. Temperature

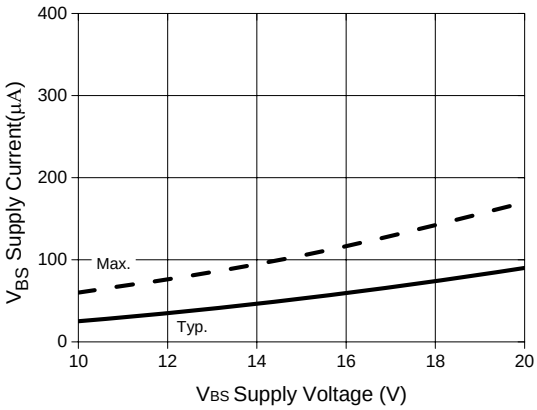


Fig24 VBS Supply Current vs. Voltage

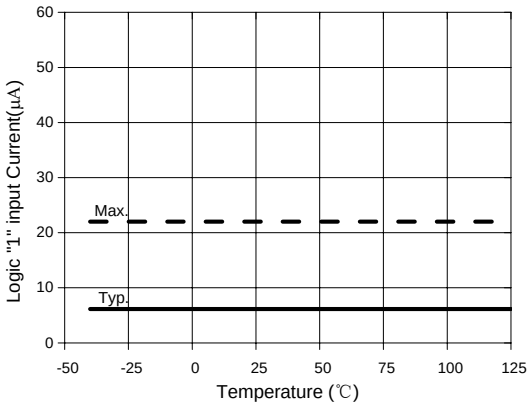


Fig25 Logic "1" Input Current vs. Temperature

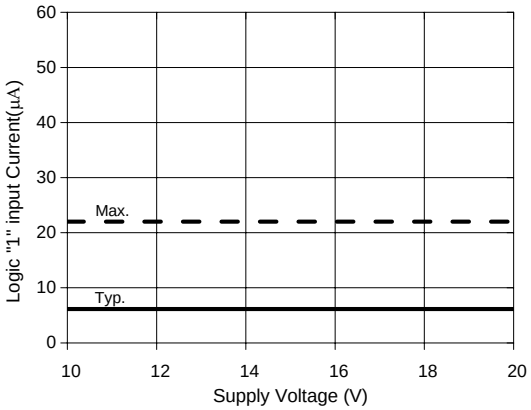


Fig26 Logic "1" Input Current vs. Voltage

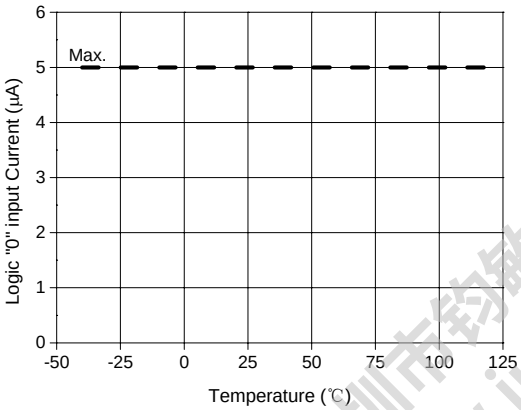


Fig27 Logic "0" Input Current vs. Temperature

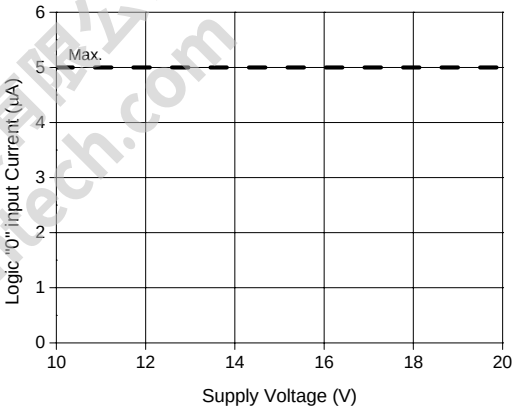


Fig28 Logic "0" Input Current vs. Voltage

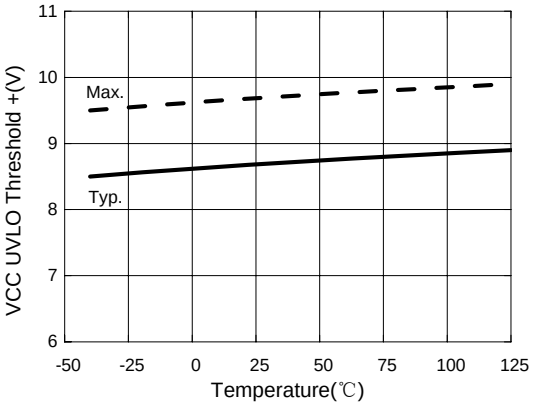


Fig29 VCC Under voltage Threshold(+) Vs. Temperature

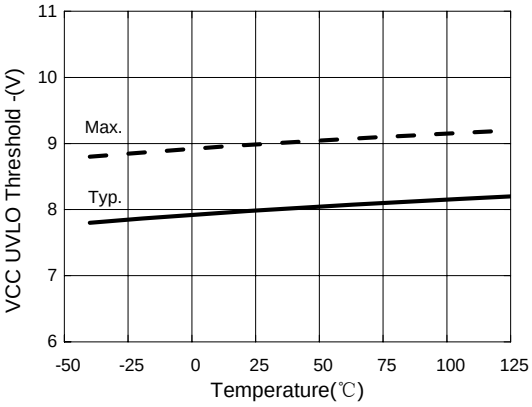


Fig30 VCC Under voltage Threshold(-) vs. Temperature

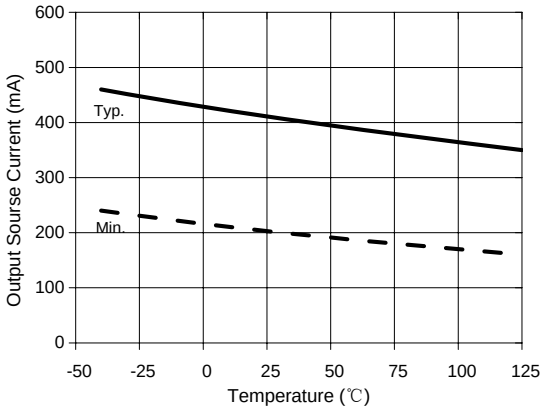


Fig31 Output Source Current vs. Temperature

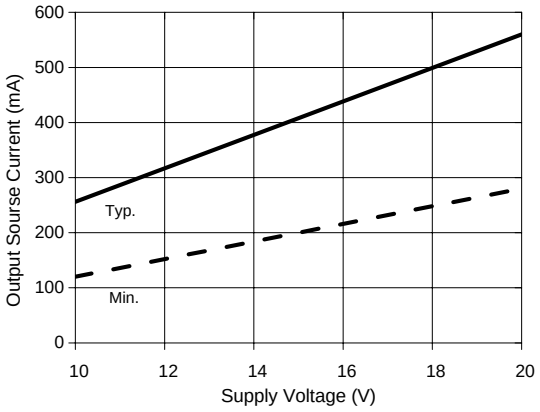


Fig32 Output Source Current vs. Voltage

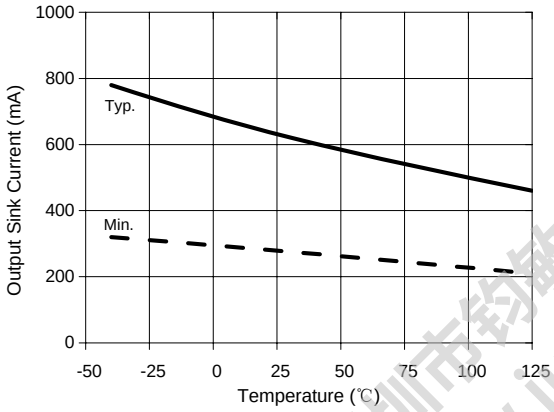


Fig33 Output Sink Current vs. Temperature

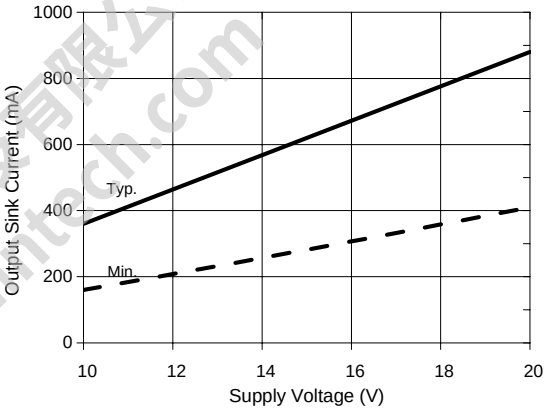


Fig34 Output Sink Current vs. Voltage

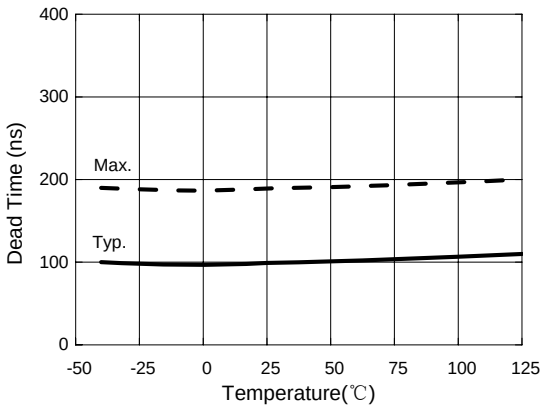


Fig35 PN7106B，Dead Time vs. Temperature

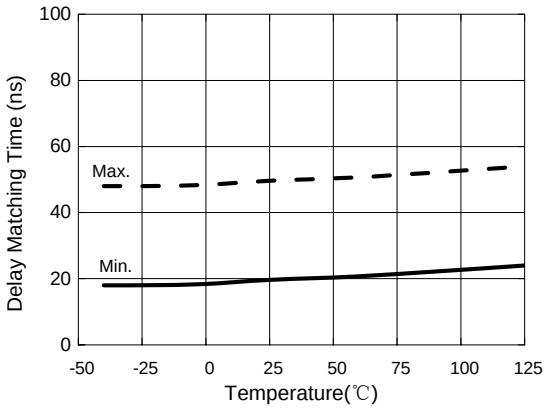


Fig36 High Side & Low Side Delay Matching Time vs. Temperature

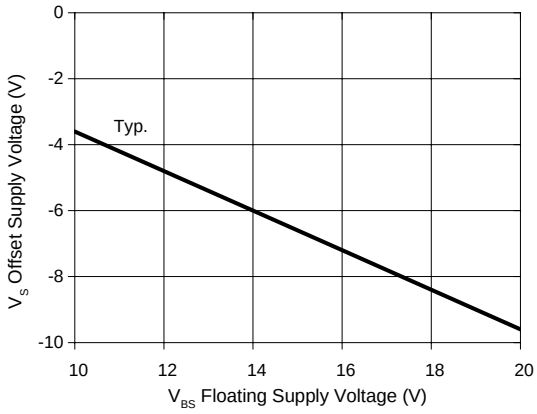


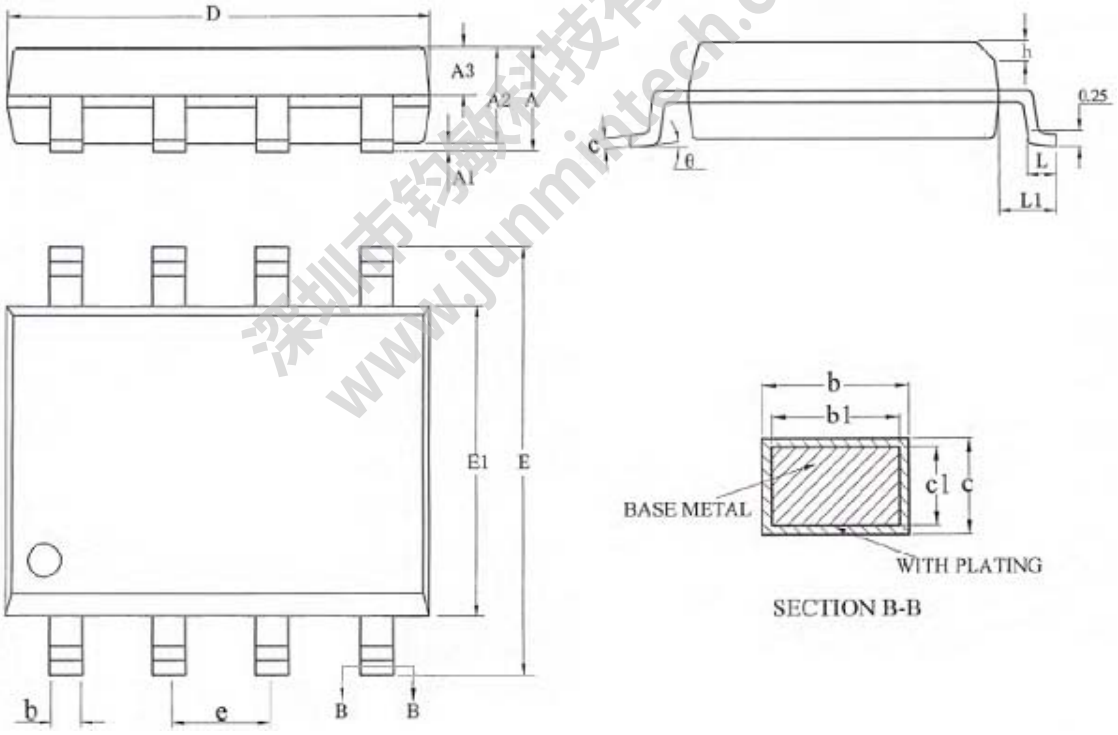
Fig37 Maximum VS Negative Offset vs. Supply Voltage

Package Information

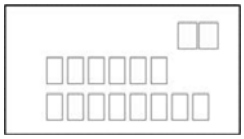
SOIC8 Package Dimensions

Size / Sample	Min(mm)	Typ(mm)	Max(mm)	Size / Sample	Min(mm)	Typ(mm)	Max(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

Package outline



SOIC8 Package Mark Information



TOP Mark
Logo
PN7106M[Note1]
YWWXXXXX[Note2]

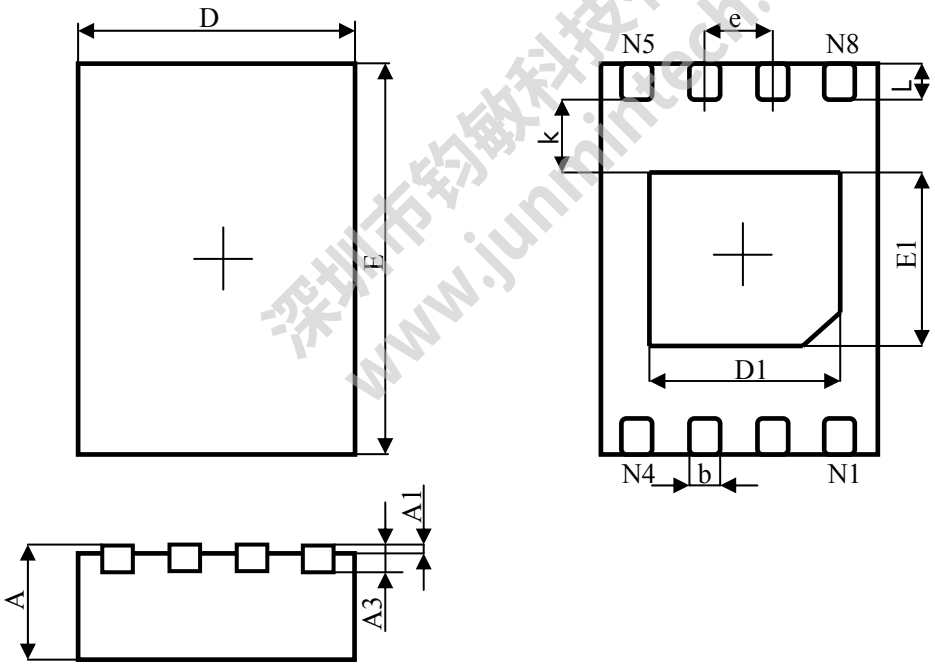
Note1：M：A or B;

Note2：Y：Year code，WW：Week codes，XXXXX：Package codes

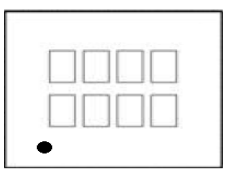
DFN8 Package Dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	2.924	3.076	0.115	0.121
D1	1.400	1.600	0.055	0.063
E1	1.400	1.600	0.055	0.063
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.224	0.376	0.009	0.015

Package Outlines



DFN8 Package Mark Information



TOP Mark
7106M[Note1]
AYWX[Note2]
Pin 1 indicator point

Note1：M：A or B;

Note2：Y：Year code，WW：Week codes，XXXXX：Package codes

Important Notice

Mosway Technologies Ltd. reserves the right to make changes without further notice to any products or specifications herein. Chipown Microelectronics Co. Ltd. does not assume any responsibility for use of any its products for any particular purpose, nor does Chipown Microelectronics Co. Ltd assume any liability arising out of the application or use of any its products or circuits. Chipown Microelectronics Co. Ltd does not convey any license under its patent rights or other rights nor the rights of others.