High and Low Side Driver

General Description

The PN7106A/B is a high voltage, high speed power MOSFET and IGBT driver based on P_SUB P_EPI process. The floating channel driver can be used to drive two N-channel power MOSFET or IGBT in a half-bridge configuration (version B) or any other high-side + low-side configuration (version A) which operates up to 600V. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications.

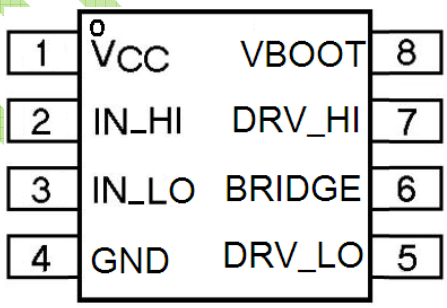
Applications

- Small and medium-power motor driver
- Power MOSFET or IGBT driver
- Lighting ballast
- Half-Bridge Power Converters
- Full-Bridge Power Converters
- Any Complementary Drive Converters (Asymmetrical Half-Bridge, Active Clamp) (A Version Only)

Features

- Fully operational to +600 V
- 3.3 V logic compatible
- dV/dt Immunity ±50 V/ns
- Floating channel designed for bootstrap operation
- Gate drive supply range from 10 V to 20 V
- UVLO for both channels
- Output Source / Sink Current Capability 450mA / 950mA
- Independent Logic Inputs to Accommodate All Topologies (Version A)
- Cross Conduction Protection with 100 ns Internal Fixed Dead Time (Version B)
- -5V negative Vs ability
- Pin-to-Pin Compatible with Industry Standards
- Matched propagation delay for both channels
- 8-Lead PDIP or 8-Lead SOIC package

Package



Typical Application Circuit

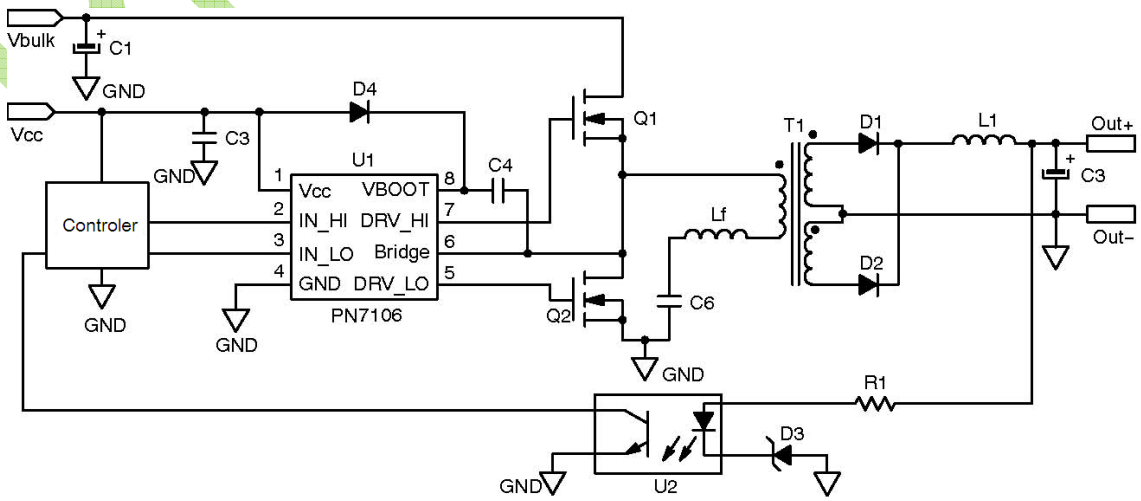


Figure1. Typical Application Resonant Converter (LLC type)

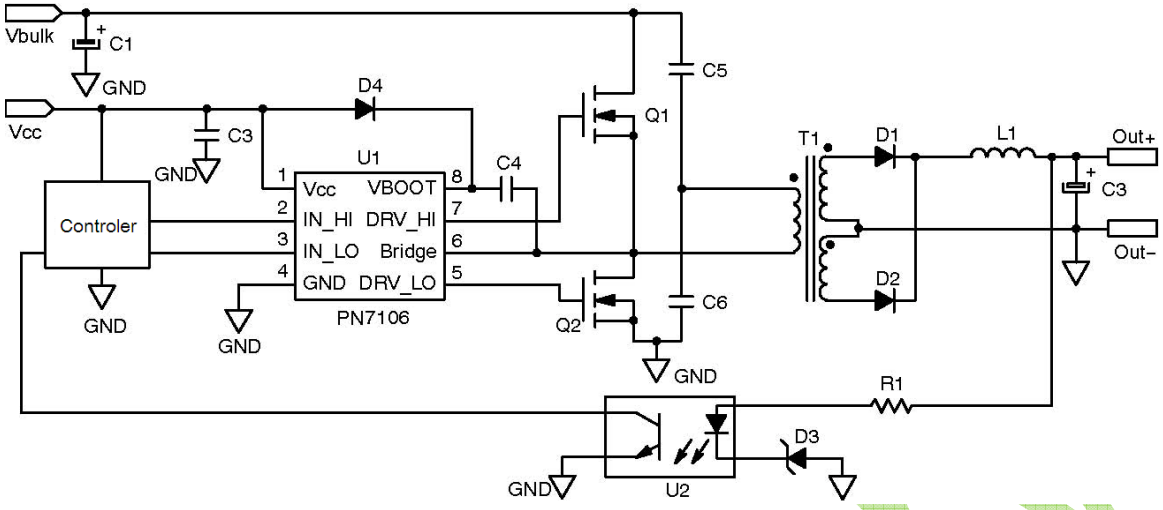


Figure2. Typical Application Half Bridge Converter

Pin Description

PIN NO.	PIN NAME	PIN FUNCTION
1	VCC	Low side and main power supply
2	IN_HI	Logic input for high side gate driver output (HO), in phase
3	IN_LO	Logic input for low side gate driver output (LO), in phase
4	GND	Ground
5	DRV_LO	Low side gate drive output, in phase with IN_LO
6	BRIDGE	High side floating supply return or bootstrap return
7	DRV_HI	High side gate drive output, in phase with IN_HI
8	VBOOT	High side floating supply

Functional Block Diagram

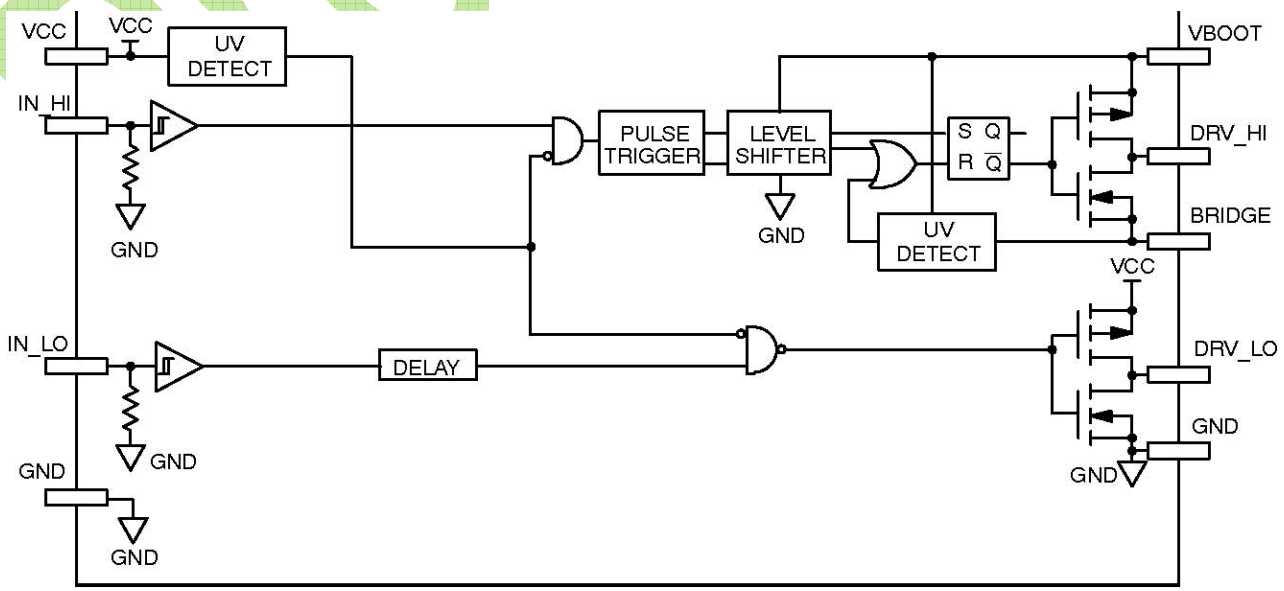


Figure3. Detailed Block Diagram: Version A

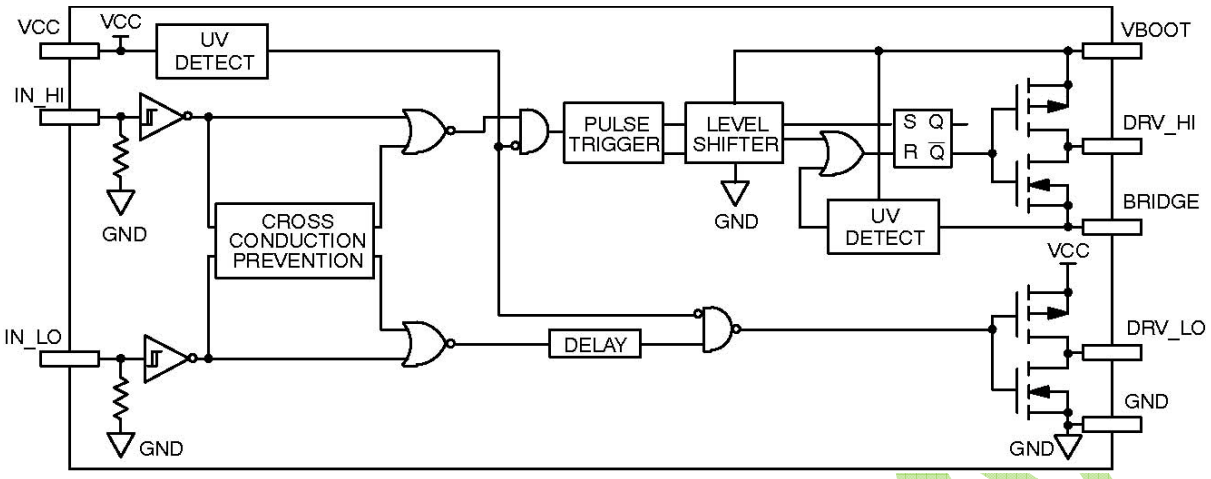


Figure4. Detailed Block Diagram: Version B

Absolute Maximum Ratings [Note1]

Symbol	Definition		MIN.	MAX.	Units
V_VBOOT	High side floating supply		-0.3	600	V
V_Bridge	High side floating supply return		V_VBOOT - 25	V_VBOOT + 0.3	
V_DRV_HI	High side gate drive output		V_Bridge -0.3	V_VBOOT + 0.3	
VCC	Low side and main power supply		-0.3	25	
V_DRV_LO	Low side gate drive output		-0.3	VCC + 0.3	
VIN_XX	Logic input of IN_HI and IN_LO		-0.3	VCC + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient		--	50	V/ns
ESD	HMB Model		2.5		kV
	Machine Model		200		V
P_D	Package Power Dissipation @ TA ≤25°C	8 Lead DIP	--	1.0	W
		8 Lead SOIC	--	0.625	
R_qJA	Thermal Resistance Junction to Ambient	8 Lead DIP	--	125	°C /W
		8 Lead SOIC	--	200	
TJ	Junction Temperature		--	150	°C
TS	Storage Temperature		-55	150	
TL	Lead Temperature (Soldering, 10 seconds)		--	300	

Note 1: Exceeding these ratings may damage the device.

Recommended Operating Conditions

Symbol	Definition	MIN.	MAX.	Units
V_VBOOT	High side floating supply	V_Bridge +10	V_Bridge +20	V
V_Bridge	High side floating supply return	-	600	
V_DRV_HI	High side gate drive output	V_Bridge	V_VBOOT	
VCC	Low side supply	10	20	
V_DRV_LO	Low side gate drive output	0	VCC	
VIN_HI	Logic input for high side	0	VCC	
VIN_LO	Logic input for low side	0	VCC	

Dynamic Electrical Characteristics

VBIAS (VCC, VBoot) = 15V, CL = 1000 pF and TA = 25°C unless otherwise specified.

Symbol	Definition	TYP.	MAX.	Units
ton_H	High side turn-on propagation delay	175	180	ns
$toff_H$	High side turn-off propagation delay	170	175	
ton_L	Low side turn-on propagation delay	175	180	
$toff_L$	Low side turn-off propagation delay	170	175	
MT	Delay matching	5.5	8.0	
DT	Dead time	98	102	
Tr	Turn-on rise time	50	55	
Tf	Turn-off fall time	25	27	

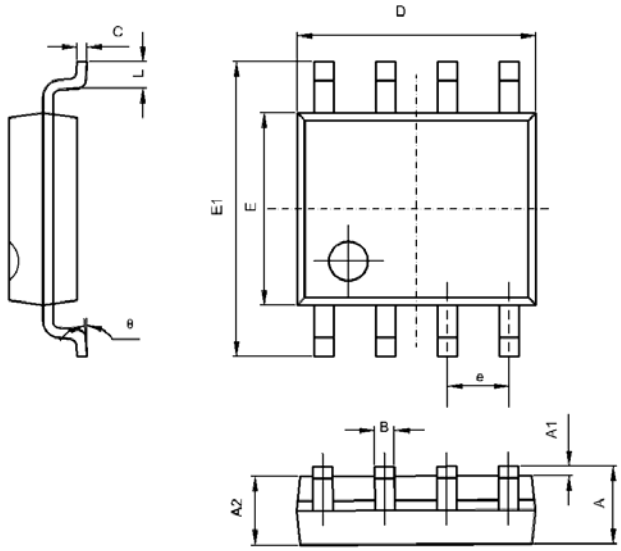
Static Electrical Characteristics

VBIAS (VCC, VBoot) = 15V, CL = 1000 pF and TA = 25°C unless otherwise specified.

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{INH}	Logic “1” input voltage	2.4	-	-	V
V_{INL}	Logic “0” input voltage	-	-	1.0	
V_{DRV-H}	High level output voltage, V_{BIAS} - V_{DRV-H}	-	-	1.3	
V_{DRV_L}	Low level output voltage, V_{DRV-H}	-	-	0.3	
I_{QCC}	Quiescent VCC supply current	-	220	240	uA
I_{QBS}	Quiescent VBOOT supply current	-	75	80	
I_{LK}	Leakage current from VBRIDGE(600V) to GND		0.15	0.2	
I_{IN+}	Logic “1” input bias current	-	6	10	
I_{IN-}	Logic “0” input bias current	-	0.00	0.1	
VBSU+	VBS supply UVLO threshold	-	8.7	-	V
VBSU-		-	8.1	-	
VCCU+	VCC supply UVLO threshold	-	8.7	-	
VCCU-		-	8.1	-	
$I_{DRVSOURCE}$	Output high short circuit pulsed current [Note2]		450		mA
$I_{DRVSINK}$	Output low short circuit pulsed current [Note2]		950		

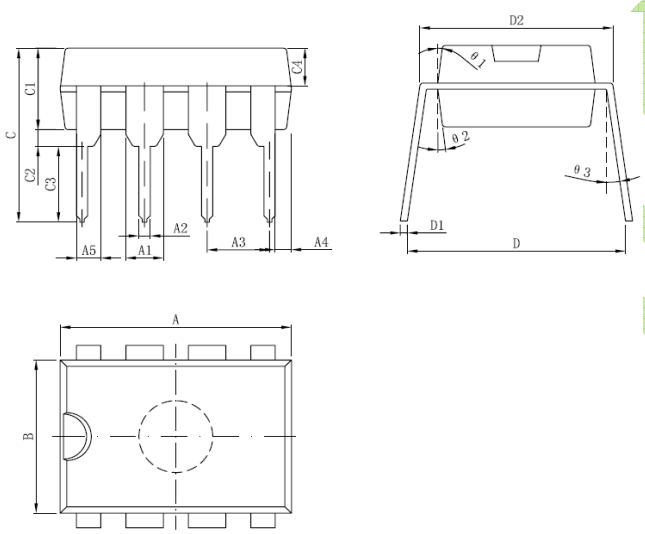
Package Information

SOP-8 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A	0.100	0.250		0.010
A	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.0	0.188	0.197
E	3.800	4.000	0.150	0.157
E	5.800	6.300	0.228	0.248
e	1.270 TYP		0.050 TYP	
L	0.400	1.270	0.016	0.050
θ	0	8	0	8

DIP8 PACKAGE OUTLINE AND DIMENSIONS



Size / symbol	Min(mm)	Max(min)	Size / symbol	Min(mm)	Max(min)
A	9.30	9.50	C2	0.50	
A1	1.524		C3	3.3	
A2	0.39	0.53	C4	1.57TYP	
A3	2.54		D	8.2	8.8
A4	0.66TYP		D1	0.2	0.35
A5	0.99TYP		D2	7.62	7.87
B	6.3	6.5	Θ1	8°TYP	
C	7.2		Θ2	8°TYP	
C1	3.3	3.5	Θ3	5°TYP	

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