Low Standby-Power Off-line PWM converters

General Description

The PN8122 consists of an integrated Pulse Width Modulator (PWM) controller and power MOSFET, specifically designed for a high performance off-line converter with minimal external components. PN8122 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over voltage protection (OVP), over temperature protection (OTP) and soft-start. Burst mode operation and device very low consumption helps to meet the standby energy saving regulations. Excellent EMI performance is achieved with frequency modulation. The device consists of the high voltage start-up circuit. The device provides an advanced platform well suited for low standby-power and cost-effective flyback converters.

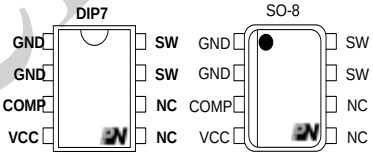
Features

- 85v to 265v wide range AC voltage input
- Operating Frequency(60kHz)
- Frequency modulation for low EMI
- Burst-mode Operation
- Built-in Soft Start
- Internal HV Start-up Circuit
- Excellent Protection :
  - ✧ Over Current Protection (OCP)
  - ✧ Over Temperature Protection (OTP)
  - ✧ Over Voltage Protection (OVP)

Applications

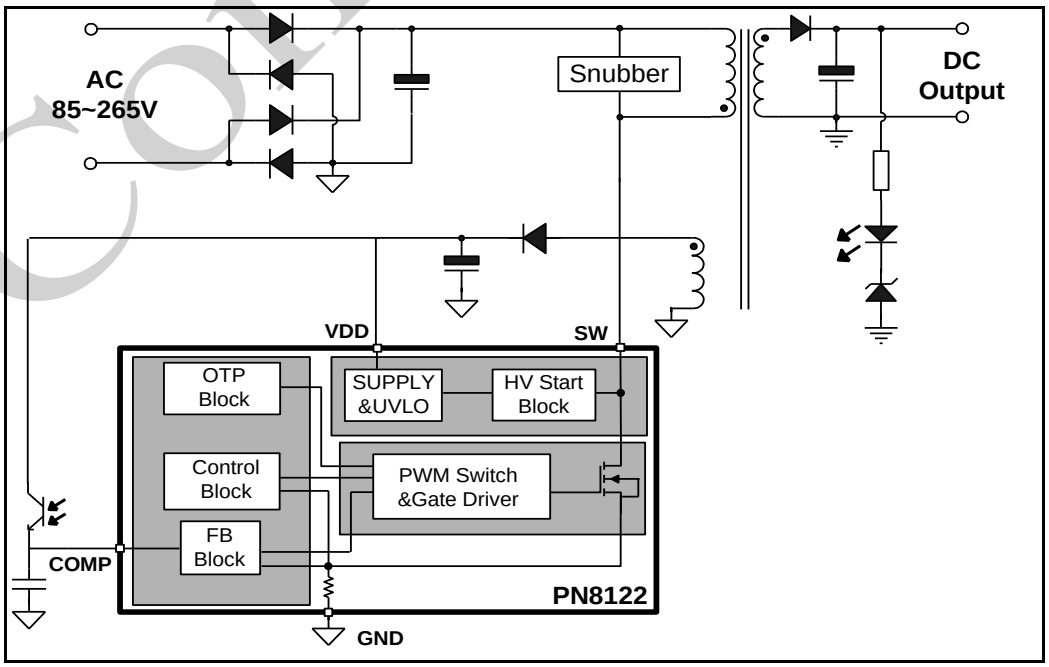
- Electromagnetic Oven power supplies
- Small household application power supplies (Coffee machine, Electric kettle, etc.)
- LED Driver

Package/Order Information



Order codes	Package
PN8122-NSC-T1	DIP7
PN8122-SEC-R1	SOP8

Typical Application



Pin Definitions

Table 1. Pin Definitions

Pin Number	Pin Name	Pin Function Description
1,2	GND	Ground
3	COMP	Voltage feedback. By connecting a opto-coupler to close the control loop and achieve the regulation.
4	VCC	Positive Supply voltage Input.
5,6	NC	No connection
7,8	SW	The SW pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 600V.

Note: NC Pin can not be connected

Typical power

Table 2. Typical power

Part number	85~265 V_{AC}		230 V_{AC} ±15%	
	SO8	DIP7	SO8	DIP7
PN8122	7W	12W	12W	20W

Note:

Maximum practical continuous power in an open frame design at 50 ℃ ambient, with adequate heat sinking.

Absolute Maximum Ratings

Supply voltage Pin VCC……-0.3~20V

High-Voltage Pin, SW……600V

Start-up Voltage ,SW to GND Voltage……-0.3~400V

Pin COMP Feedback Current……3mA

Continuous VDMOS Drain Current……Internally limited

ESD voltage Protection……2.5kV

Junction Operating Temperature……Internally limited

Case Operating Temperature……-40~150℃

Storage Temperature Range……-55~150℃

Lead Temperature (Soldering, 10secs) ……260℃

Electrical Characteristics

(T_J =25℃, V_{CC} = 15 V; unless otherwise specified)

Table 3. Power section

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	VDMOS Breakdown Voltage	I_D=250uA;V_{COMP}=2V	600	650		V
R_{DSON}	Static Drain-Source on Resistance	V_{GS}=10V;I_D=0.4 A;		15		Ω

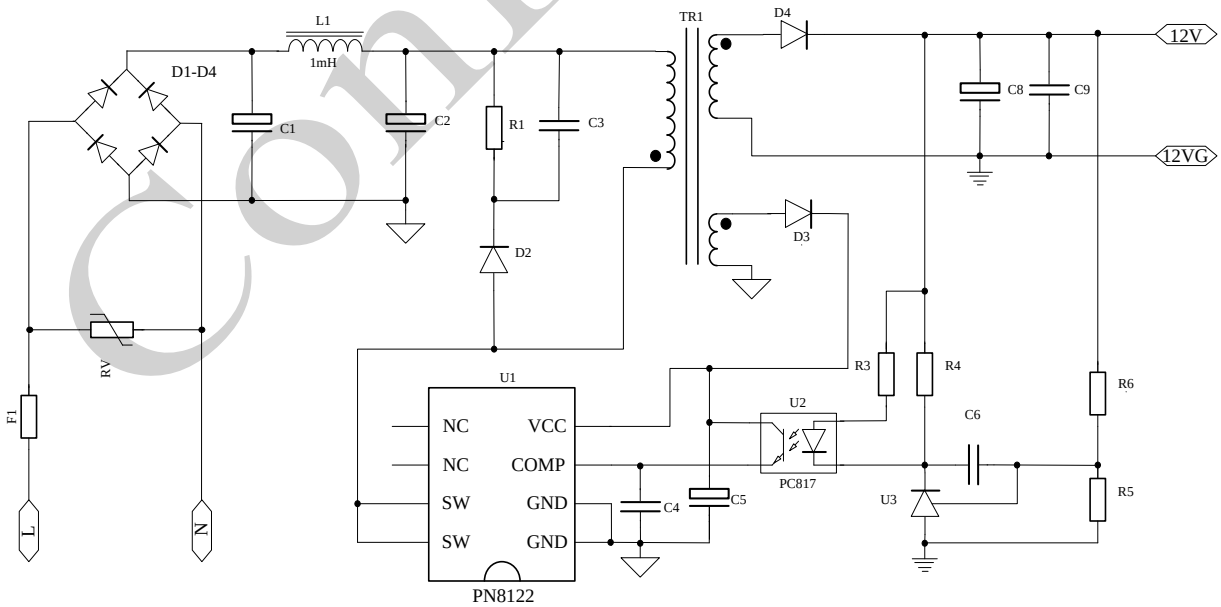
Table 4. Control section

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
UVLO SECTION						
V_{START}	VCC Start Threshold Voltage	V_{COMP}=0V	12	13	14	V
V_{STOP}	VCC Stop Threshold Voltage	V_{COMP}=0V	8	9	10	V
V_{HYS}	VCC Threshold Hysteresis			4		V
OSCILLATOR SECTION						
F_{OSC}	Initial Accuracy	0≤T_j≤ 100℃	54	60	66	kHz
FD	Frequency Variation			±4		kHz
FM	Modulation frequency			250		Hz
DMAX	Maximum duty cycle		70		80	%
FEEDBACK SECTION						
I_{COMP}	Feedback Shutdown Current			0.9		mA
R_{COMP}	COMP Pin Input Impedance			1.2		kΩ
CURRENT LIMIT(SELF-PROTECTION)SECTION						
I_{LIM}	Peak Current Limit	T_j = 25 ℃	0.61	0.72	0.82	A
TLEB	Minimum Turn On Time	LEB time		300		ns
tSS	Soft-start time			8		ms
ID_BM	Peak drain current during burst mode	VCOMP= 0.6 V	95	135	176	mA
PROTECTION SECTION						
T_{SD}	Thermal Shutdown Temperature		120	160	-	℃
T_{HYST}	Thermal Shutdown Hysteresis			40		℃
SUPPLY CURRENT SECTION						

V_{DRAIN_START}	Drain-source start voltage		60	80	100	V
I_{CH}	Startup Charging Current (SW pin)	V_{DRAIN} = 120 V, V_{COMP} = GND,VDD = 4 V		-1		mA
		VDRAIN = 120 V , V_{COMP} = GND,VDD = 4 V after fault.	-0.4	-0.6	-0.8	mA
I_{DD}	Operating supply current, switching	VDRAIN = 120 V			1.2	mA
VDD	Operating voltage range	After turn-on	9.5		19	V
VDDclamp	VDD clamp voltage	IDD = 20 mA	20.5			V
VDDovp	VDD ovp Voltage		22			V
IDD_FAULT	Operating supply current, with protection tripping	V_{COMP} = 0V			400	uA
IDD_OFF	Operating supply current with VDD < VDD_OFF	VDD = 7 V			270	uA

Typical circuit

Figure 1. Flyback application (basic)



Functional Description

1. Startup

This device includes a high voltage start up current source connected on the SW of the device. As soon as a voltage is applied on the input of the converter, this start up current source is activated and to charge the VCC capacitor as long as VCC is lower than VSTART. When reaching VSTART, the start up current source is cut off by UVLO&TSD and the device begins to operate by turning on and off its main power MOSFET. As the COMP pin does not receive any current from the opto-coupler, the device operates at full current capacity and the output voltage rises until reaching the regulation point where the secondary loop begins to send a current in the opto-coupler. At this point, the converter enters a regulated operation where the COMP pin receives the amount of current needed to deliver the right power on secondary side.

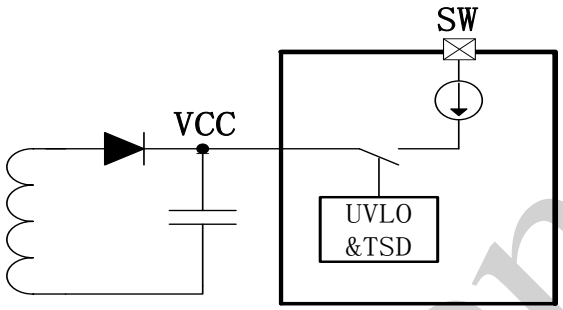


Fig 1 Startup circuit

2. Soft-start up

In the process of start up, the current of drain increases to maximum limitation step by step. As a result, it can reduce the stress of secondary diode greatly and is propity to prevent the transformer turning into the saturation states. Typically, the duration of soft-start is 8ms.

3. Gate driver

The internal power MOSFET in PN8122 is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate drive results in worse EMI.

A good tradeoff is achieved through the built-in totem pole gate design with proper output strength and dead time. The good EMI system design and low idle loss is easier to achieve with this dedicated control scheme.

4. Oscillator

The switching frequency of PN8122 is internally fixed at 60 kHz. No external frequency setting components are required for PCB design.

The frequency modulation is implemented in PN8122. So that, it minimizes the conduction band EMI and therefore eases the system design because the tone energy could be spread out.

5. Feed-back

A feedback pin controls the operation of the device. Unlike conventional PWM control circuits which use a voltage input, the COMP pin is sensitive to current. Figure 2 presents the internal current mode structure. The Power MOSFET delivers a sense current which is proportional to the main current. R2 receives this current and the current coming from the COMP pin. The voltage across R2(VR2) is then compared to a fixed reference voltage. The

MOSFET is switched off when VR2 equals the reference voltage.

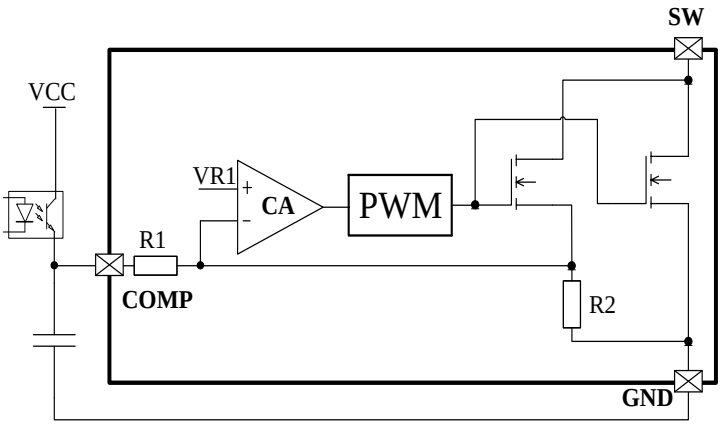


Fig 2 Feedback circuit

6. Leading Edge Blanking (LEB)

At the instant the internal Sense FET is turned on, there usually exists a high current spike through the Sense FET, caused by the primary side capacitance and secondary side rectifier diode reverse recovery. Excessive voltage across the sense resistor would lead to false feedback operation in the current mode PWM control. To counter this effect, the device employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (typically 300ns) after the Sense FET is turned on.

7. Under Voltage Lock Out

Once fault condition occurs, switching is terminated and the Sense FET remains off. This causes VCC to fall. When VCC reaches the UVLO stop voltage, 9V, the protection is reset and the internal high voltage current source charges the VCC capacitor. When VCC reaches the UVLO start voltage, 13V, the device resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power Sense FET until the fault condition is eliminated.

8. Thermal Shutdown (TSD)

The Sense FET and the control IC are integrated in the same chip, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 160℃, thermal shutdown is activated, the device turn off the Sense FET and the high voltage current source to charge VCC. The device will go back to work when the lower threshold temperature about 120℃ is reached.

Package Dimensions（DIP7）

Table 5. DIP7 mechanical data

Size / symbol	Min(mm)	Max(mm)	Size / symbol	Min(mm)	Max(mm)
A	9.30	9.50	C2	0.50	
A1	1.524		C3	3.3	
A2	0.39	0.53	C4	1.57TYP	
A3	2.54		D	8.2	8.8
A4	0.66TYP		D1	0.2	0.35
A5	0.99TYP		D2	7.62	7.87
B	6.3	6.5	Θ1	8 ℃TYP	
C	7.2		Θ2	8 ℃TYP	
C1	3.3	3.5	Θ3	5 ℃TYP	

Figure 3. Package dimensions

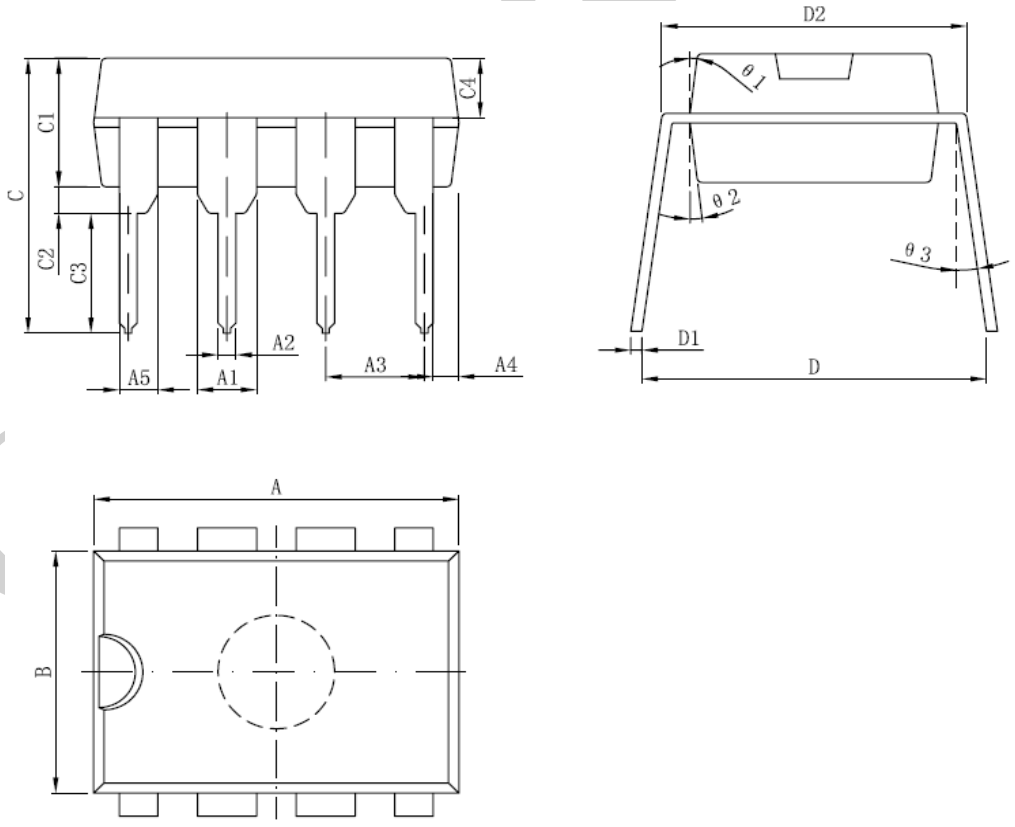
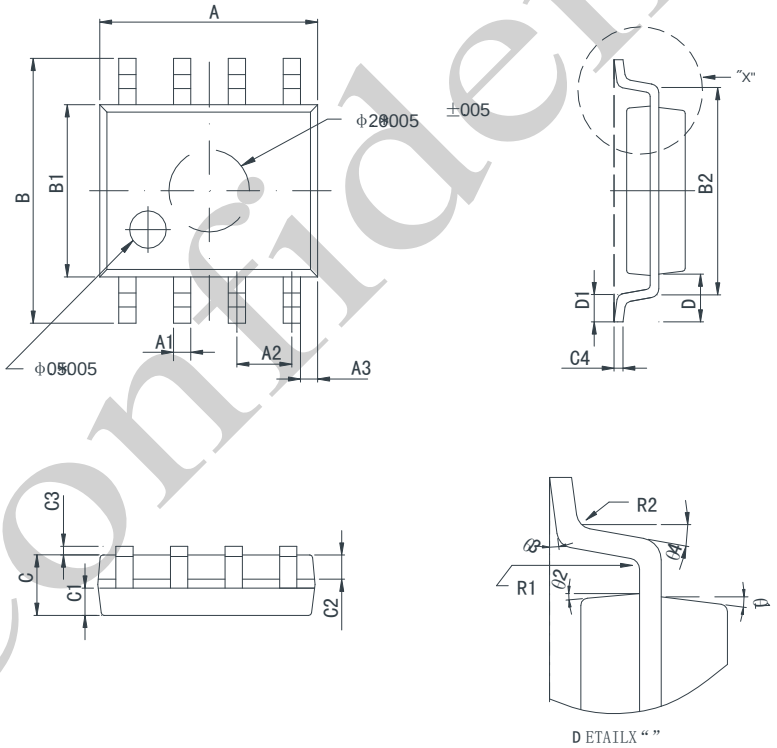


Table 6. SOP-8 mechanical data

Size symbol	Min(mm)	Nom(mm)	Max(mm)	Size symbol	Min(mm)	Nom(mm)	Max(mm)
A	4.95	—	5.15	C3	0.05	—	0.20
A1	0.37	0.42	0.47	C4	0.20TYP		
A2	1.2TYP			D	1.05TYP		
A3	0.41TYP			D1	0.40	0.50	0.60
B	5.80	6.00	6.20	R1	0.07TYP		
B1	3.80	3.90	4.00	R2	0.07TYP		
B2	5.0TYP			θ1		17	
C	1.30	1.40	1.50	θ2	11 °	13 °	15 °
C1	0.55	0.60	0.65	Θ3	0 °	—	8 °
C2	0.55	0.60	0.65	Θ4	12 °TYP		

Figure 4. Package dimensions



TOP MARK	Package
PN8122	DIP7
YWWXXXXX	SOP8

Note: Y: Year Code; W: Week Code; XXXXX: Internal Code