Low Standby-Power Quasi-Resonant Primary-Side Converter

General Description

The PN8386 consists of a Low Standby-Power Quasi-Resonant (QR) Primary-Side controller and a 650V avalanche-rugged smart power VDMOSFET, specifically designed for a high performance AC/DC charger or adaptor with minimal external components. PN8386 operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. Because of internal HV Start-up circuit, the system with PN8386 can achieve less than 50mW standby power consumption (264VAC). In CV mode, multi-mode and quasi resonant technique is utilized to achieve high efficiency, avoid audible noise and make the system meeting Energy star class VI. Good load regulation is achieved by the built-in cable drop compensation. In CC mode, the current and output power setting can be adjusted externally by the sense resistor at CS pin. PN8386 offers complete protections including Cycle-by-Cycle current limiting protection (OCP), over voltage protection (OVP), over temperature protection (OTP) and CS open or short protection (CSO/SP) etc.

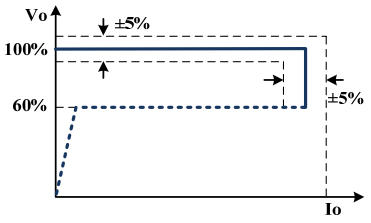
Applications

- Switch AC/DC Adaptor
- Battery Charger

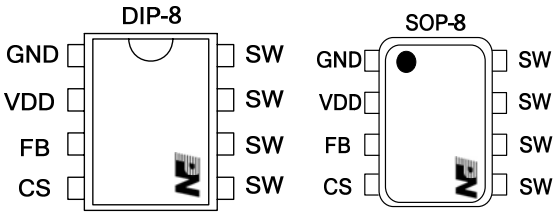
Features

- Internal 650 V avalanche-rugged smart power VDMOSFET
- Internal HV Start-up Circuit, Standby power consumption < 50mW at 264VAC
- Multi-mode and Quasi-Resonant technique
- ±5% CC Regulation at Universal AC input
- Primary-side Sensing and Regulation without TL431 and Opto-coupler
- Programmable Cable Drop Compensation
- No-need Control Loop Compensation Capacitance
- Excellent Protection Coverage:
  - ✧ Over Temperature Protection (OTP)
  - ✧ VDD Under/Over Voltage Protection(UVLO&OVP)
  - ✧ Cycle-by-Cycle Current Limiting (OCP)
  - ✧ Cs Short/Open Protection (CS O/SP)

Output Features

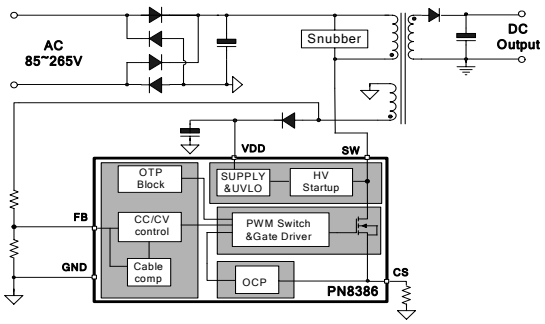


Package/Order Information



Order codes	Package	Typical power
		85~265 V_{AC}
PN8386NEC-T1	DIP-8	18W
PN8386SEC-R1	SOP-8	15W

Typical Circuit



Pin Definitions

Pin Name	Pin Number	Pin Function Description
GND	1	Ground
VDD	2	Power supply
FB	3	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
CS	4	Current Sense Input
SW	5,6,7,8	Avalanche-rugged power MOSFET Drain pin. The Drain pin is connected to the primary lead of the transformer.

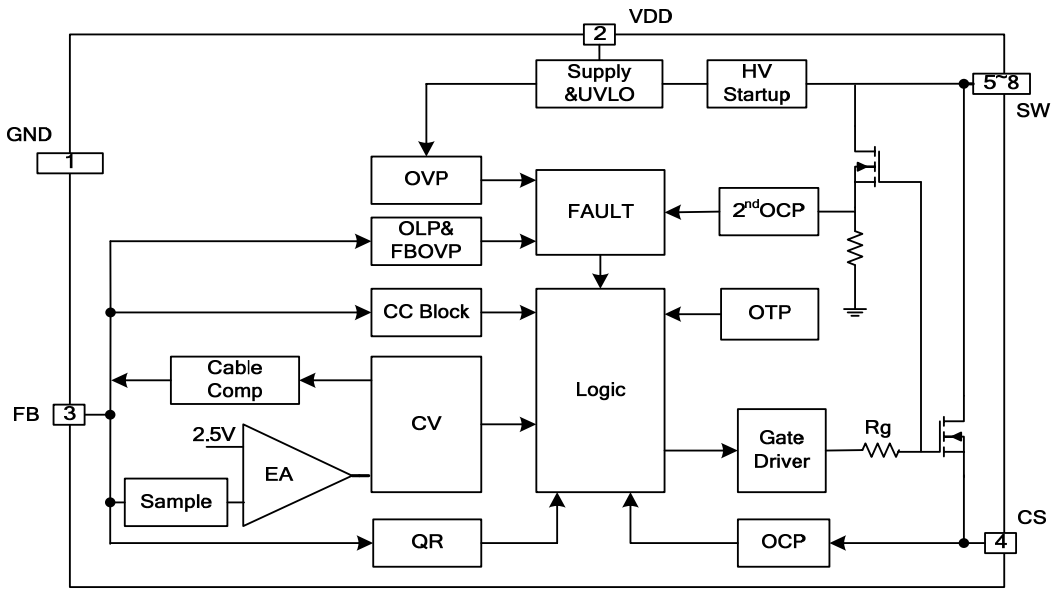
Typical power

Part Number	Package	Adapter(1)
		85-265 V_{AC}
PN8386	DIP-8	18W
	SOP-8	15W

Note:

1. Maximum output power is tested in an adapter at 45°C ambient temperature, with enough cooling conditions.

Block Diagram



Absolute Maximum Ratings

Supply voltage Pin VDD……-0.3~40V

Pin FB, CS……-0.3~5.5V

High-Voltage Pin, SW…… -0.3~650V

Operating Junction Temperature……-40~150℃

Storage Temperature Range…… ….-55~150℃

Note：1.Test standard: ESDA/JEDEC JDS-001-2014。

Lead Temperature (Soldering, 10Secs)……...260℃

Package Thermal Resistance $R\theta_{JC}$（DIP-8）..…….40℃/W

Package Thermal Resistance $R\theta_{JC}$（SOP-8）...…….80℃/W

HBM ESD Protection [(1)] ……..…..…±4kV

Pulse Drain Current（T_{pulse}=100us）……..…..…..…5A

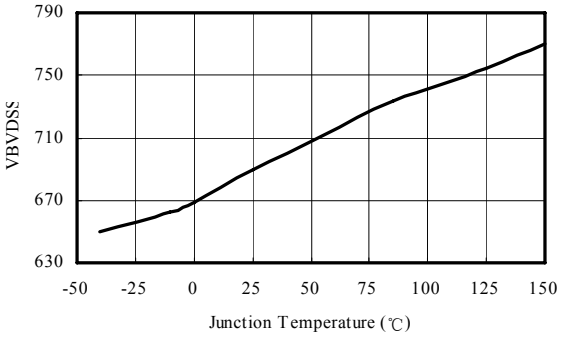
Electrical Characteristics

(T_A = 25°C, V_{DD} = 21 V, unless otherwise specified)

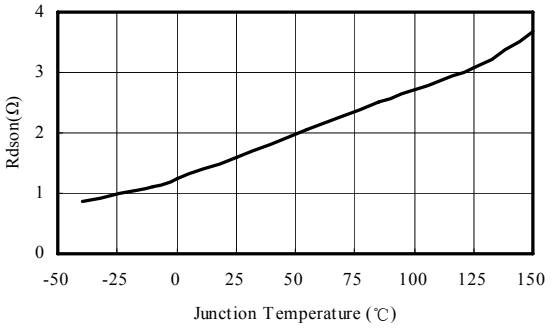
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power Section						
Break-down voltage	BVDSS	I_{SW} =250uA	650	700		V
Off-state drain current	I_{OFF}	V_{sw} =500V			100	μA
Drain-source on state resistance	$R_{DS(on)}$	I_{SW} = 1A, T_J = 25℃		1.6		Ω
Start up threshold	V_{SW_START}	V_{DD}=V_{DDon} - 1V		30		V
Supply Voltage Section						
Operating voltage range	V_{DD}		10		30	V
VDD start up threshold	V_{DDon}		14.5	16.5	18.5	V
VDD under voltage shutdown threshold	V_{DDoff}		7.5	8.5	9.5	V
VDD over voltage protect	V_{DDovp}		30	34	38	V
Supply Current Section						
VDD charge current	I_{DD_CH}	V_{DD}=V_{DDon} - 1V, Vsw=100V		0.85		mA
Operating current, switching	I_{DD}	V_{DD} = 19.5V	0.3	0.5	0.7	mA
Operating current after fault	I_{DD_FAULT}	V_{DD}＝15V after fault		0.5		mA
Current Sense Section						
Current sense threshold	V_{TH_OC}		485	500	515	mV
Maximum Current sense threshold	$V_{TH\_OC\_MAX}$			560		mV
Minimum CS threshold	Vcs_min			170		mV
Leading Edge Blanking time	T_{LEB}			300		ns
Maximum Ton	T_{onmax}			50		us
OCP propagation delay	T_{D_OC}			100		ns

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
FB Section						
Reference voltage for feedback threshold	V_{REF_CV}		2.475	2.5	2.525	V
Output over voltage protection threshold	V_{FBOVP}		2.85	3	3.15	V
Output under voltage threshold	V_{UVP}			1.55		V
Maximum cable compensation current	Icable	V_{FB}=0V	44	48	52	uA
Minimum Toff	T_{offmin}			5		us
Maximum Toff	T_{offmax}			2.2		ms
Output under voltage protection Blanking time	T_{UVP}	F_{SW}= 50kHz	20		32	ms
Thermal Section						
Thermal shutdown temperature threshold	T_{SD}		135	150		°C
Thermal shutdown hysteresis	T_{HYST}			30		°C

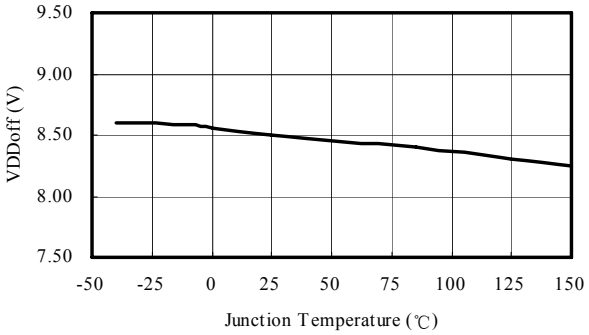
Typical Characteristics Plots



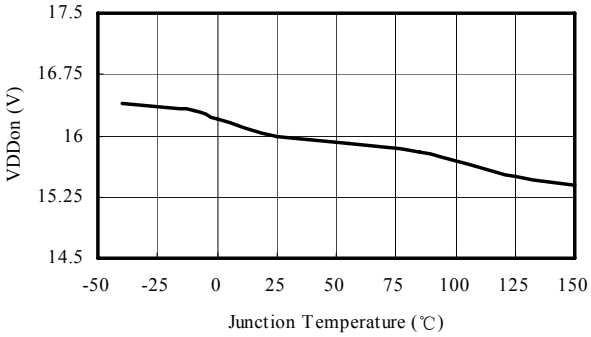
(a) BV vs Tj



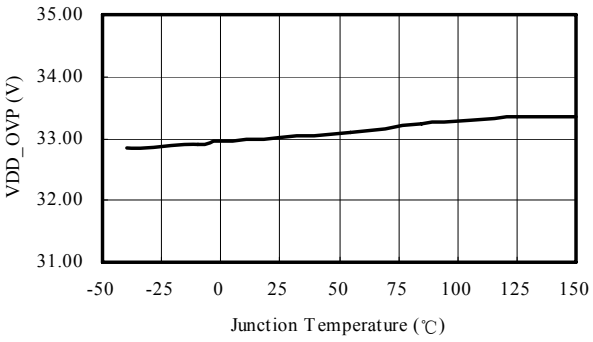
(b) Rdson vs Tj



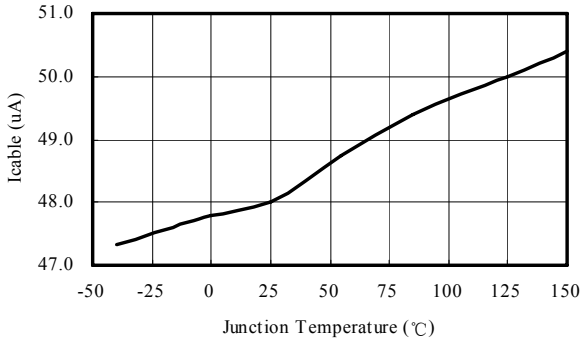
(c) V_{DDoff} vs Tj



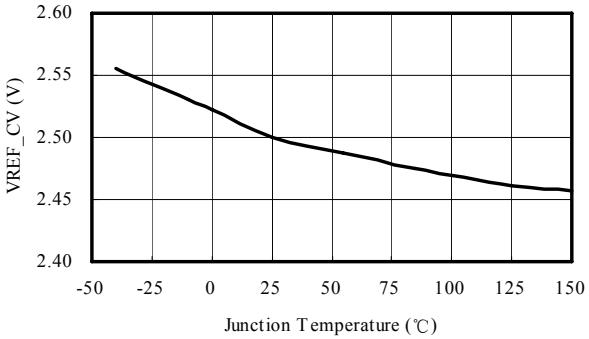
(d) V_{DDon} vs Tj



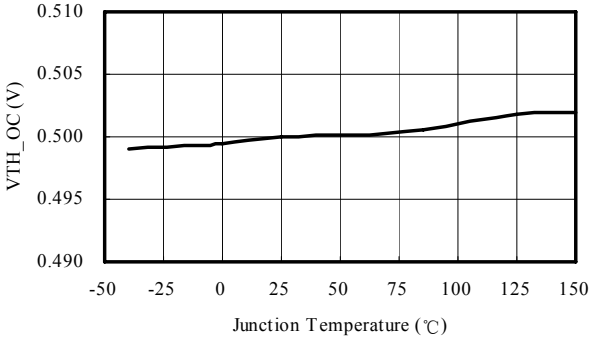
(e) VDD_OVP vs Tj



(f) Icable vs Tj



(g) V_{REF_CV} vs Tj



(h) V_{TH_OC} vs Tj

Functional Description

The PN8386 is a high performance CC/CV primary-side controller. PN8386 operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve high precision CC/CV control meeting most charger and adaptor application requirements. Internal HV Start-up circuit and the chip's low consumption help the system to meet strict standby power standard.

1. HV Start up Control

At start up, the internal high-voltage start-up circuit provides the internal bias and charges the external VDD capacitor, so that PN8386 starts up quickly. When VDD reaches V_{DDon}, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device keeps in normal operation provided as long as VDD keeps above V_{DDoff}. After startup, the bias is supplied from the auxiliary transformer winding, the current of HV start-up circuit is designed to be very low so that the power consumption is very low.

2. CC Operation Mode

In CC operation mode, the PN8386 captures the auxiliary flyback signal at FB pin through a resistor dividing-network. The pulse width of the auxiliary flyback signal determines the PN8386 oscillator frequency. The higher the output voltage is, the shorter the pulse width is, and the higher the chip oscillator frequency is, thus the constant output current can be achieved.

The current waveform of DCM mode is shown in Figure 1. During MOSFET turn-on time, the current in the primary winding (Ipri) ramps up. When MOSFET turns off, the energy stored in the primary winding is transferred to the secondary side, so the peak current in the secondary winding is

$$I_{sec\_pk} = I_{pri\_pk} \times N_{ps} \quad (1)$$

The output current is

$$I_O = \frac{I_{sec\_pk}}{2} \times \frac{T_{demag}}{T_P} = \frac{1}{2} N_{PS} \frac{V_{CS}}{R_{sense}} \frac{T_{demag}}{T_P} \quad (2)$$

Because Vipk is constant and Tp is equal to tow times Tdemag, the output current Io is constant.

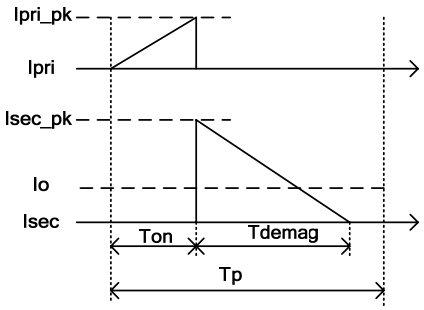


Figure 1. The current waveform of DCM mode

3. CV Operation Mode

In CV mode，PN8386 uses a pulse to sample V_{FB} and it is hold until the next sampling. The sampled voltage is compared with V_{REF_CV} and the error is amplified. The error amplified output reflects the load condition and controls the switching off time to regulate the output voltage, thus constant output voltage can be achieved.

The relationship between the output voltage and V_{REF_CV} is

$$Vo = (V_{REF\_CV} \times \frac{R1 + R2}{R2}) \times \frac{N_S}{N_{AUX}} \quad (3)$$

N_S means Secondary winding, N_{AUX} means Auxiliary winding

The PN8386 operates in PFM_QR mode during full load mode, since the peak current (Ipeak) of MOSFET is constant, the chip frequency decreases while the output current decreases. When the switching frequency approaches to 25kHz, the PN8386 enters PWM_QR mode, the chip frequency decreases slowly while the output current decreases, the Ipeak decreases while the output current decreases. Therefore the PN8386 can avoid audible noise, while achieving high efficiency at 25% load conditions. When Vcs decreases to 170mV, the PN8386 enters Standby mode. In this mode, Ipeak

keeps around constant, the chip oscillator frequency decreases while the output current decreases. Figure 2 illustrates the relations of the switching frequency, Ipeak and Loading for PN8386.

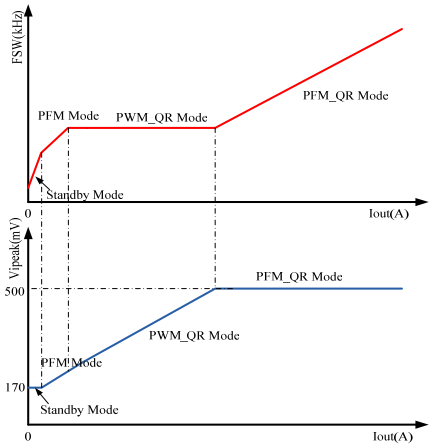


Figure 2. The Switching Frequency, Vipeak VS. LOAD

4. Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in PN8386. The switch current is detected by a sense resistor at CS pin. The CC set-point and maximum output power can be externally adjusted by external current sense resistor at CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power MOSFET on-state so that the external RC filtering on sense input is no longer needed.

5. Programmable Cable Drop Compensation

In PN8386, an offset voltage is generated at FB pin by an internal current flowing into the divider resister, as shown in Figure 3. The Cable Drop Compensation block compensates the voltage drop across the cable. As the load current decreases from full load to no load, the voltage drop across the cable decreases. It can be programmed by adjusting the external resistor R2 or R1 at FB pin. The maximum compensation is

$$\frac{V_{cable}}{V_O} = \frac{I_{cable} \times (R2 // R1)}{2.5V} \qquad (4)$$

Because of the influence of the chip's sampling position and devices of the system, the actual maximum compensation is less than theoretical value.

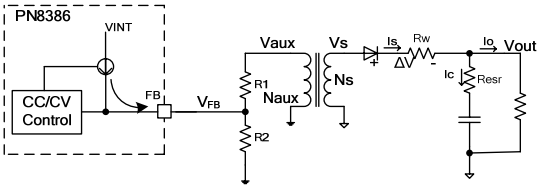


Figure 3. Icable

6. Reference Negative Temperature Compensation

As shown in Figure 3, the voltage of FB pin is

$$V_{FB} = K(V_O + \Delta V), K = \frac{R2 \times N_{AUX}}{(R1 + R2) \times N_S} \qquad (5)$$

Where ΔV has a negative temperature coefficient, K is a constant.

In PN8386, the voltage reference uses the negative temperature compensation technology. At room temperature, the voltage reference is 2.5V. The voltage reference (V_{REF_CV}) decreases while the temperature of chip increases. The reference negative temperature compensation block compensates the ΔV, thus the output voltage keeps constant at full range of temperature. The reference negative temperature compensation improves output precision.

7. Quasi-Resonant Switching

The PN8386 incorporates a unique proprietary quasi-resonant switching scheme that achieves valley-mode turn on for every switching cycle in CV mode. This unique feature greatly reduces the switching loss. The actual switching frequency can vary slightly cycle by cycle, providing the additional benefit of reducing EMI.

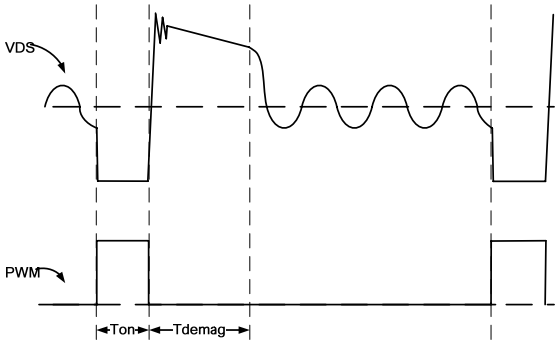
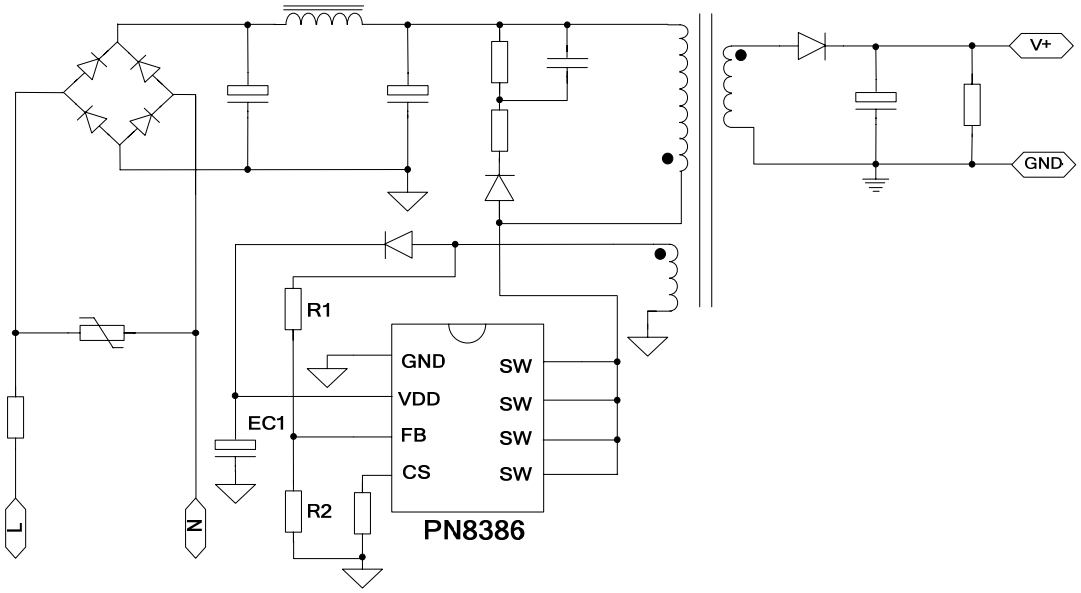


Figure 4. QR Mode

8. Protection Control

The PN8386 has several self-protection functions, such as Cycle-by-Cycle current limiting (OCP), Over-Voltage Protection, Over-Temperature Protection, Feedback Loop open Protection, Output short circuit Protection, CS resistor open/short circuit Protection and Under Voltage Lockout on VDD. All protections are self-recovered.

Typical Application

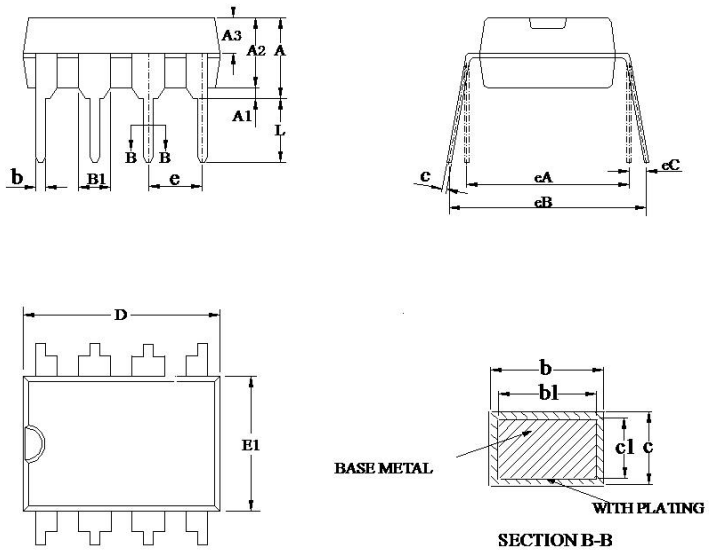


Component Parameter and Layout Considerations:

1. VDD capacitor EC1 should be placed at the nearest place from the VDD pin and the GND pin.

Package Information

DIP-8 Package Information



Size / symbol	Min.(mm)	Max.(mm)	Size / symbol	Min.(mm)	Max.(mm)
A	3.60	4.00	c1	0.23	0.27
A1	0.51	——	D	9.05	9.45
A2	3.00	3.40	E1	6.15	6.55
A3	1.55	1.65	e	2.54BSC	
b	0.44	0.53	e A	7.62BSC	
b1	0.43	0.48	e B	7.62	9.30
B1	1.52BSC		e C	0.00	0.84
c	0.24	0.32	L	3.00	——

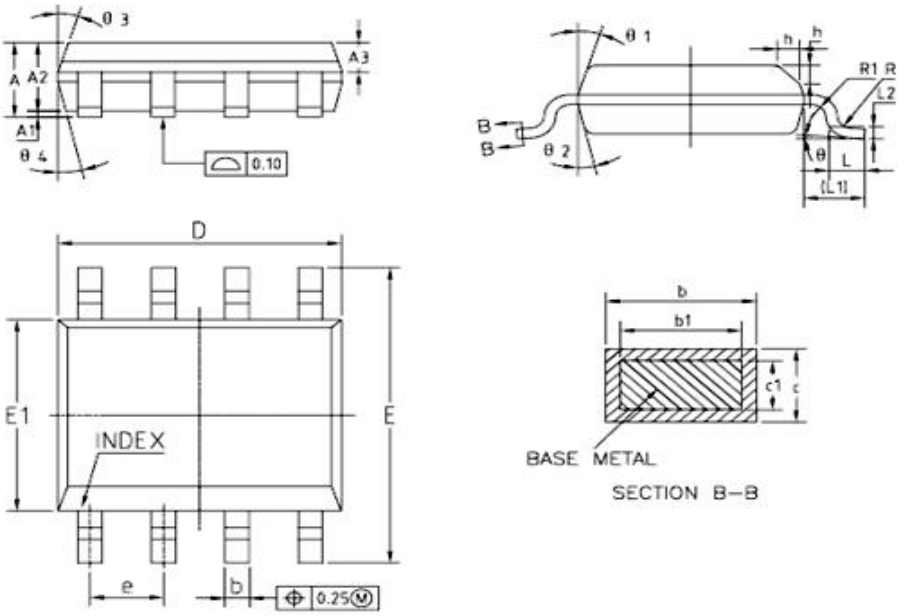
TOP MARK	Package
PN8386 YWWXXXXX	DIP-8

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:

1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

SOP-8 Package Information



Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)	Size / Symbol	Min.(mm)	Typ.(mm)	Max.(mm)
A	1.35	1.55	1.75	L	0.45	0.60	0.80
A1	0.10	0.15	0.25	L1	1.04REF		
A2	1.25	1.40	1.65	L2	0.25BSC		
A3	0.50	0.60	0.70	R	0.07	—	—
b	0.38	—	0.51	R1	0.07	—	—
b1	0.37	0.42	0.47	h	0.30	0.40	0.50
c	0.17	—	0.25	θ	0°	—	8°
c1	0.17	0.20	0.23	θ1	15°	17°	19°
D	4.80	4.90	5.00	θ2	11°	13°	15°
E	5.80	6.00	6.20	θ3	15°	17°	19°
E1	3.80	3.90	4.00	θ4	11°	13°	15°
e	1.270（BSC）						

TOP MARK	Package
PN8386 YWWXXXXX	SOP-8

Note: Y: Year Code; WW: Week Code; XXXXX: Internal Code

Notes:

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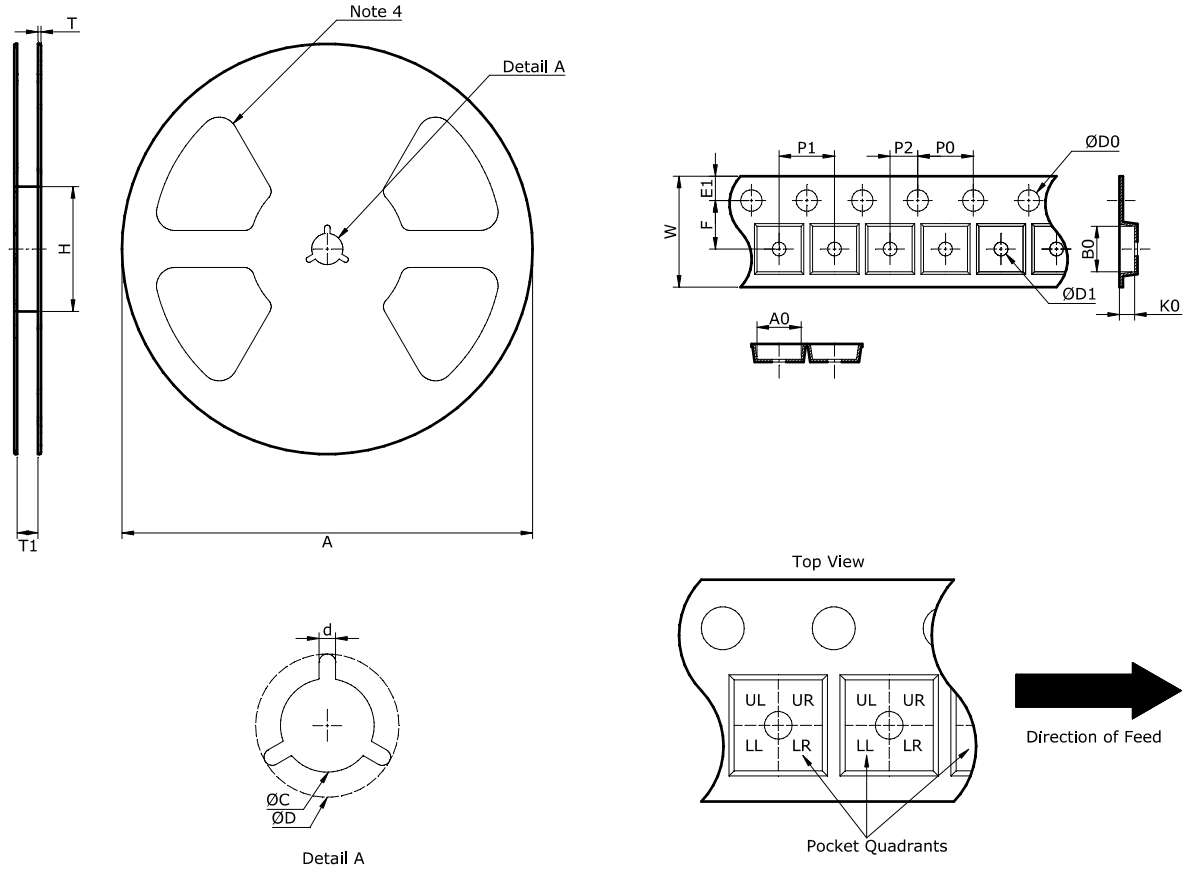
Tape and Reel Information



SOP-8 Package									
A (mm)	**T (mm)**	**T1 (mm)**	**H (mm)**	**ØC (mm)**	**ØD (mm)**	**d (mm)**	**A0 (mm)**	**B0 (mm)**	**K0 (mm)**
330±1.0	3 +1/−0	12.4 +1/−0	100±0.5	12.00 +0.5/−0.2	17.70 ±0.40	2.00 +0.5/−0.2	6.60 ±0.1	5.2±0.1	1.9±0.1
W (mm)	**F (mm)**	**E1 (mm)**	**P0 (mm)**	**P1 (mm)**	**P2 (mm)**	**ØD0 (mm)**	**ØD1 (mm)**	**Pin 1 Quadrant**	
12.00 ±0.1	5.50±0.1	1.75 ±0.10	4.00 ±0.10	8.0 ±0.1	2.0 ±0.1	1.5 +0.1/−0	1.55 ±0.05	UL	

Notes:

1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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