

## Internal BJT Low Standby-Power Primary-side Converter

### General description

The PN8571M consists of a Low Standby-Power Primary-Side controller and BJT, specifically designed for a high performance AC/DC charger or adapter with minimal external components.

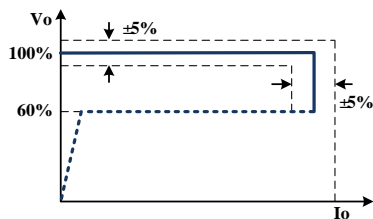
PN8571M operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. In CV mode, multi-mode technique is utilized to achieve high efficiency, avoid audible noise and make the system meeting Energy star level VI. Good load regulation is achieved by the built-in cable drop compensation. In CC mode, the current and output power setting can be adjusted externally by the sense resistor at CS pin.

PN8571M offers complete protections including Cycle-by-Cycle current limiting protection (OCP), over voltage protection (OVP), open loop protection (OLP), over temperature protection (OTP) and CS open or short protection (CS O/SP) etc.

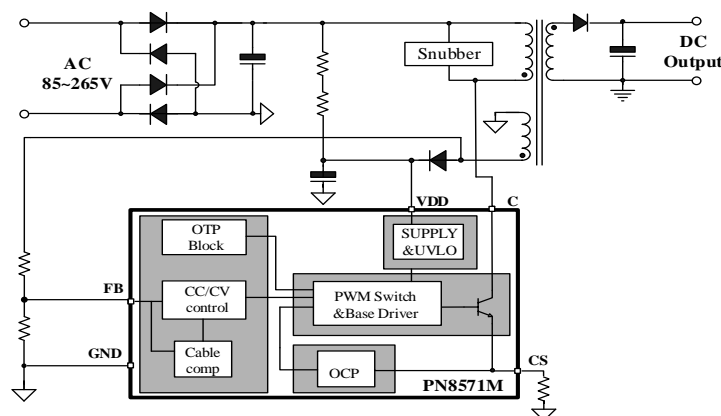
### Application

- Switch AC/DC Adapter
- Battery Charger
- Set-top box power supply

### Output Features



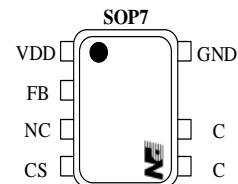
### Typical Circuit



### Features

- Internal BJT switch
- Multi-mode technique
- $\pm 5\%$  CC Regulation at Universal AC input
- Primary-side Sensing and Regulation without TL431 and Opto-coupler
- Programmable Cable Drop Compensation
- No-need Control Loop Compensation Capacitor
- Excellent Protection include:
  - ◇ Over Temperature Protection (OTP)
  - ◇ VDD Under/Over Voltage Protection(UVLO&OVP)
  - ◇ Cycle-by-Cycle Current Limiting (OCP)
  - ◇ CS Short/Open Protection (CS O/SP)
  - ◇ Open Loop Protection(OLP)

### Package/Order Information



Order code	Package	Typical Power
		85~265V <sub>AC</sub>
PN8571MSSC-R1C	SOP7	7.5W

## Pin Definitions

Pin Name	Pin Number	Pin Function Description
VDD	1	Power supply
FB	2	The voltage feedback from auxiliary winding. Connected to resistor divider from auxiliary winding reflecting output voltage.
NC	3	No connection
CS	4	Current Sense Input
C	5,6	HV BJT collector pin
GND	7	Ground

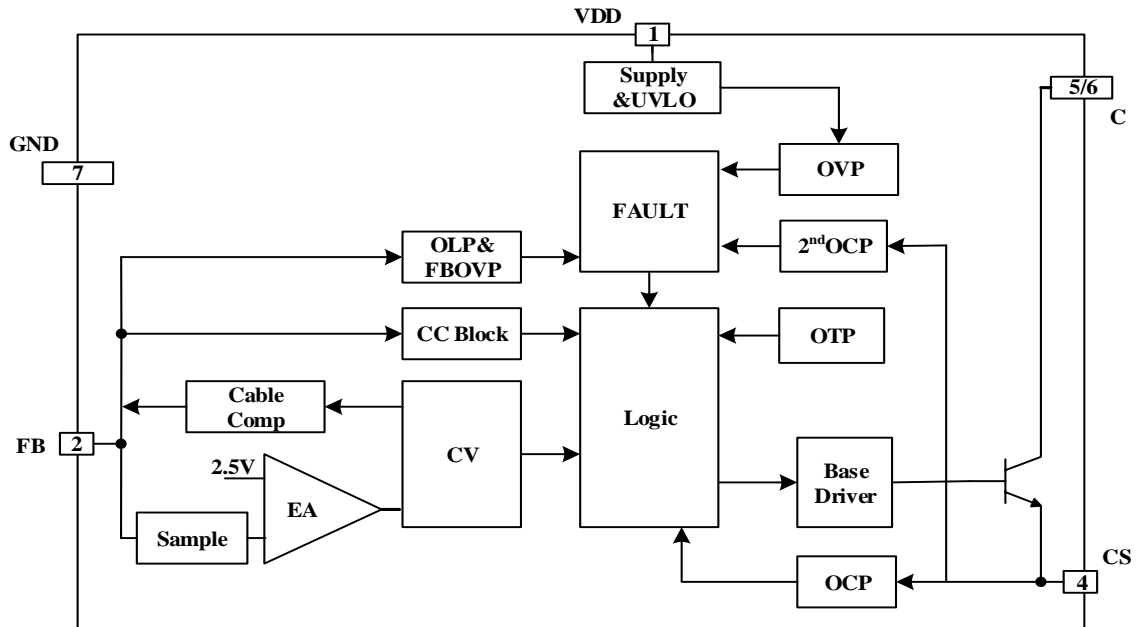
## Typical Power

Part number	Package	Adapter <sup>(1)</sup>
		85~265V <sub>AC</sub>
PN8571M	SOP7	7.5W

Note:

1. Maximum output power is tested in an adapter at 40 °C ambient temperature, with enough cooling conditions.

## Block Diagram



## Absolute Maximum Ratings

Supply voltage Pin VDD.....-0.3~40V  
 Pin CS .....-0.3~5.5V  
 Pin FB(I<sub>FB</sub>≤10mA) .....-1~5.5V  
 CB voltage .....700V  
 Operating Junction Temperature.....-40~150 °C

Storage Temperature Range.....-55~150 °C  
 Lead Temperature (Soldering, 10Secs).....260 °C  
 Package Thermal Resistance θ<sub>JC</sub> (SOP7) .....40 °C /W  
 HBM ESD Protection <sup>(1)</sup> .....±3kV

Note:

1. Test standard: ANSI/ESDA/JEDEC JS-001-2017.

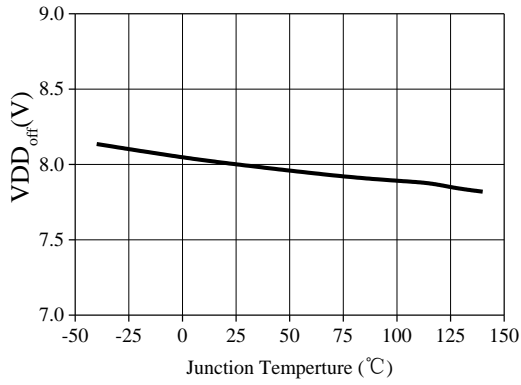
## Electrical Characteristics

(T<sub>A</sub>= 25 °C, VDD=21V, unless otherwise specified)

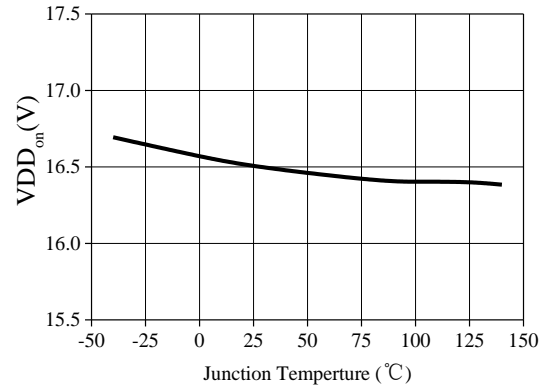
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Power Section</b>						
Collector-base breakdown voltage	V <sub>CBO</sub>	I <sub>C</sub> =10mA	700			V
Collector-emitter breakdown voltage	V <sub>CEO</sub>	I <sub>C</sub> =10mA, I <sub>B</sub> =0		410		V
Collector Peak Current	I <sub>C</sub>				0.6	A
<b>Supply Voltage Section</b>						
Operating voltage range	VDD		9.0		30	V
VDD start up threshold	VDD <sub>on</sub>		14.5	16.5	18.5	V
VDD under voltage shutdown threshold	VDD <sub>off</sub>		7	8	9	V
VDD over voltage protect	VDD <sub>ovp</sub>		30	33	36	V
<b>Supply Current Section</b>						
VDD charge current	I <sub>DD_STARTUP</sub>	VDD=VDD <sub>on</sub> - 1V		3	5	uA
Operating current, switching	I <sub>DD</sub>	VDD = VDD <sub>on</sub> +1V	0.1	0.5	0.8	mA
Operating current after fault	I <sub>DD_FAULT</sub>	VDD= 15V after fault		0.5		mA
<b>Current Sense Section</b>						
Current sense threshold	V <sub>TH_OC</sub>		485	500	515	mV
Maximum Current sense threshold	V <sub>TH_OC_MAX</sub>			560		mV
Minimum CS threshold	V <sub>CS_min</sub>			170		mV
Leading Edge Blanking time	T <sub>LEB</sub>			300		ns
Maximum Ton	T <sub>onmax</sub>		32	40	50	us
OCP propagation delay	T <sub>D_OC</sub>			100		ns
<b>FB Section</b>						
Reference voltage for feedback threshold	V <sub>REF_CV</sub>		2.45	2.475	2.51	V
Output over voltage protection threshold	V <sub>FBOVP</sub>		2.85	3	3.15	V
Output under voltage threshold	V <sub>UVP</sub>			1.55		V
Maximum cable compensation current	I <sub>cable</sub>	V <sub>FB</sub> =0V	33	36	39	uA

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Minimum Toff	$T_{offmin}$			5		us
Maximum Toff	$T_{offmax}$			2.2		ms
Output under voltage protection Blanking time	$T_{UVP}$	$F_S=50kHz$	40		64	ms
<b>Thermal Section</b>						
Thermal shutdown temperature threshold	$T_{SD}$		135	150		°C
Thermal shutdown hysteresis	$T_{HYST}$			30		°C

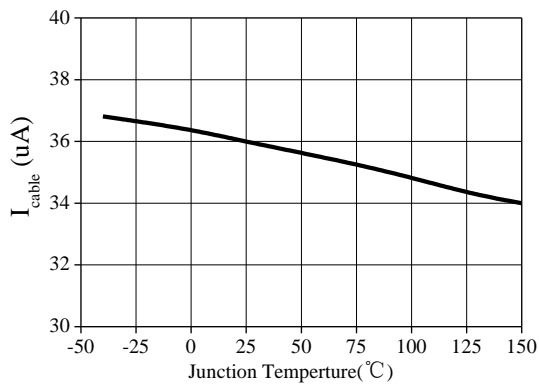
## Typical Characteristics Plots



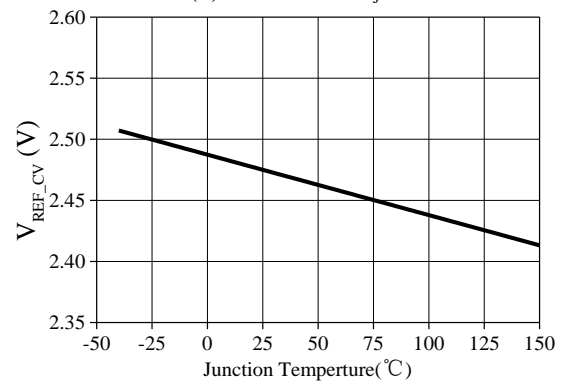
(a) VDD<sub>off</sub> VS T<sub>j</sub>



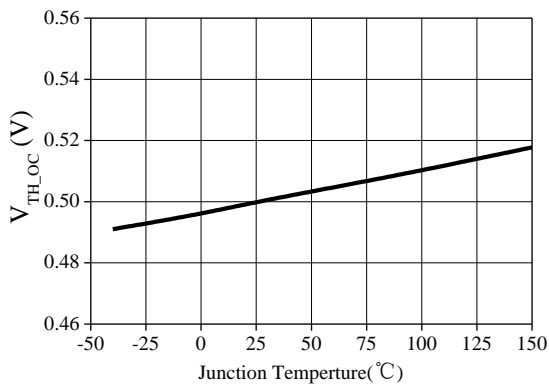
(b) VDD<sub>on</sub> VS T<sub>j</sub>



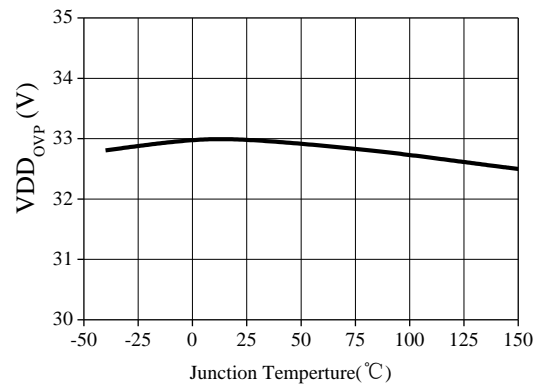
(c) I<sub>cable</sub> VS T<sub>j</sub>



(d) V<sub>REF\_CV</sub> VS T<sub>j</sub>



(e) V<sub>TH\_OC</sub> VS T<sub>j</sub>



(f) VDD<sub>OVP</sub> VS T<sub>j</sub>

## Functional Description

The PN8571M is a high performance CC/CV primary-side controller. PN8571M operates in primary-side sensing and regulation, so opto-coupler and TL431 could be eliminated. Proprietary built-in CV and CC control can achieve high precision CC/CV control meeting most charger and adapter application requirements. Startup current of PN8571M is designed to be very low so a large value startup resistor can be used to minimize the power loss in application.

### 1. Start up Control

At start up, external startup resistor charges the VDD capacitor via VDD pin. When VDD reaches VDD<sub>on</sub>, the device starts switching. The device keeps in normal operation provided as long as VDD keeps above VDD<sub>off</sub>. After startup, the bias is supplied from the auxiliary transformer winding.

### 2. CC Operation Mode

In CC operation mode, the PN8571M captures the auxiliary flyback signal at FB pin through a resistor dividing-network. The pulse width of the auxiliary flyback signal determines the PN8571M oscillator frequency. The higher the output voltage is, the shorter the pulse width is, and the higher the chip oscillator frequency is, thus the constant output current can be achieved.

The current waveform in DCM mode is shown in Fig.1. During BJT turn-on time, the current in the primary winding (I<sub>pri</sub>) ramps up. When BJT turns off, the energy stored in the primary winding is transferred to the secondary side, so the peak current in the secondary winding is

$$I_{sec\_pk} = I_{pri\_pk} \times N_{ps} \quad (1)$$

The output average current is

$$I_O = \frac{I_{sec\_pk}}{2} \times \frac{T_{demag}}{T_p} = \frac{1}{2} N_{PS} \frac{V_{CS}}{R_{sense}} \frac{T_{demag}}{T_p} \quad (2)$$

Where R<sub>sense</sub> means system resistor at CS pin, N<sub>PS</sub> means primary winding and secondary winding turn ratio.

In CC mode, PN8571M fixes  $\frac{T_{demag}}{T_p}$  to be 0.5, and V<sub>CS</sub> to

be V<sub>TH\_OC</sub> (typically 0.5V, actually about 0.58V considering the affection of system and delay time). Meanwhile, assuming the current coupling ratio is K<sub>c</sub>, the output current will be constant as:

$$I_O = \frac{1}{4} N_{PS} \frac{0.58}{R_{sense}} \times K_c \quad (3)$$

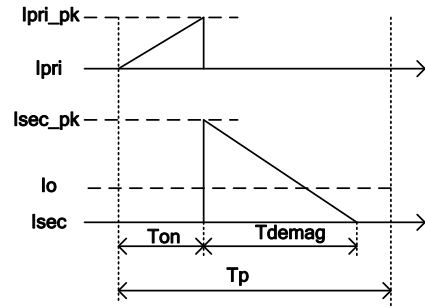


Fig.1 The current waveform in DCM mode

### 3. CV Operation Mode

In CV mode, PN8571M uses a pulse to sample V<sub>FB</sub> and holds hold until the next sampling. The sampled voltage is compared with V<sub>REF\_CV</sub> and the error is amplified. The error amplified output reflects the load condition and controls the switching off time to regulate the output voltage, thus constant output voltage can be achieved.

The relationship between the output voltage and V<sub>REF\_CV</sub> is

$$V_O = (V_{REF\_CV} \times \frac{R1 + R2}{R2}) \times \frac{N_S}{N_{AUX}} \quad (4)$$

N<sub>S</sub> means Secondary winding turns, N<sub>AUX</sub> means Auxiliary winding turns.

The PN8571M operates in PFM mode during full load mode, since the peak current (I<sub>peak</sub>) of BJT is constant, the chip frequency decreases while the output current decreases. When the switching frequency approaches to 25kHz, the PN8571M enters PWM mode, the chip frequency decreases slowly while the output current decreases, the I<sub>peak</sub> decreases while the output current decreases. Therefore the PN8571M can avoid audible noise, while achieving high efficiency at 25% load conditions. When V<sub>cs</sub> decreases to 170mV, the PN8571M enters Standby mode. In this mode, I<sub>peak</sub> keeps around constant, the chip oscillator frequency decreases while the output current decreases. Fig.2 illustrates the relations of the switching frequency, I<sub>peak</sub> and Loading for PN8571M.

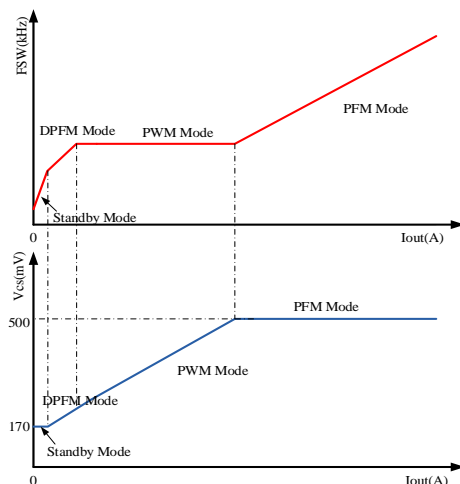


Fig.2 The Switching Frequency, V<sub>CS</sub> VS. LOAD

## 4. Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in PN8571M. The switch current is detected by a sense resistor at CS pin. The CC set-point and maximum output power can be externally adjusted by external current sense resistor at CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial power BJT on-state so that the external RC filtering on sense input is no longer needed.

## 5. Programmable Cable Drop Compensation

In PN8571M, an offset voltage is generated at FB pin by an internal current flowing into the divider resistor, as shown in Fig.3. The Cable Drop Compensation block compensates the voltage drop across the cable. As the load current decreases from full load to no load, the voltage drop across the cable decreases. It can be programmed by adjusting the external resistor R2 or R1 at FB pin. The maximum compensation is

$$\frac{V_{cable}}{V_O} = \frac{I_{cable} \times (R2 // R1)}{2.5V} \quad (5)$$

Because of the influence of the chip's sampling position and parameters of the system, the actual maximum compensation may be less than theoretical value.

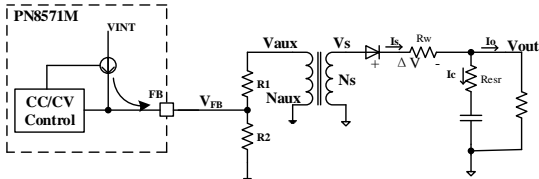


Fig.3 I\_cable

## 6. Reference Negative Temperature Compensation

As shown in Fig.3, the voltage of FB pin is

$$V_{FB} = K_R (V_O + \Delta V), \quad K_R = \frac{R2 \times N_{AUX}}{(R1 + R2) \times N_S} \quad (6)$$

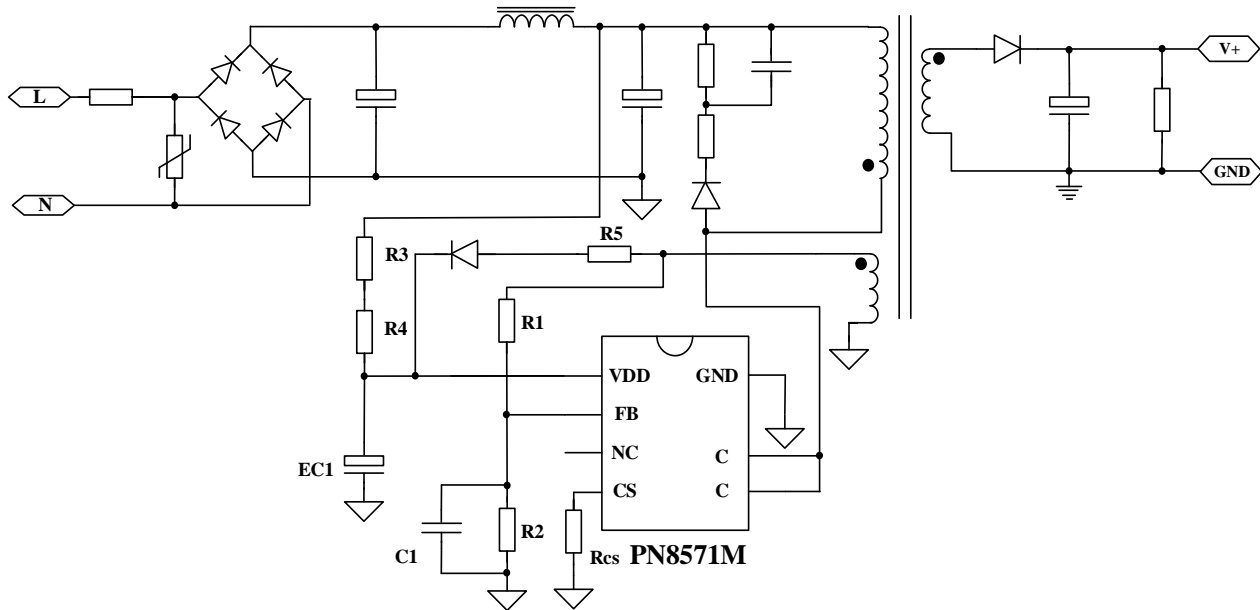
Where  $\Delta V$  has a negative temperature coefficient,  $K_R$  is a constant.

In PN8571M, the voltage reference uses the negative temperature compensation technology. At room temperature, the voltage reference is 2.5V. The voltage reference ( $V_{REF\_CV}$ ) decreases while the temperature of chip increases. The reference negative temperature compensation block compensates the  $\Delta V$  represented rectifier diode VF variation, thus the output voltage keeps constant at full range of temperature. The reference negative temperature compensation improves output precision.

## 7. Protection Control

The PN8571M has several self-protection functions, such as Cycle-by-Cycle current limiting (OCP), Over-Voltage Protection, Over-Temperature Protection, Feedback Loop open Protection, Output short circuit Protection, CS resistor open/short circuit Protection and Under Voltage Lockout on VDD. All protections are self-recovered.

## Typical Application



### Component Parameter and Layout Considerations:

1. VDD capacitor EC1 should be placed at the nearest place between the VDD pin and the GND pin.
2. It is suggested that the power supply diode and the R5 should be connected in series in order to improve the safety capability. The recommend value is 4.7ohm.
3. It is suggested that the FB pin and the C1 should be connected in parallel in order to improve the anti-interference of the sampling network. The recommend value is 47pF.
4. Choose CS resistance reasonably to avoid  $I_C$  exceeding 0.6A.



## Package Information

### Package Information SOP7

Symbol	Size	Min. (mm)	Max. (mm)	Symbol	Size	Min. (mm)	Max. (mm)
A		1.45	1.75	E		5.8	6.2
A1		0.05	0.25	E1		3.85	4.05
A2		1.35	1.55	L		0.4	1.27
b		0.3	0.5	$\theta$		0°	8°
D		4.7	5.1	e		1.270(BSC)	

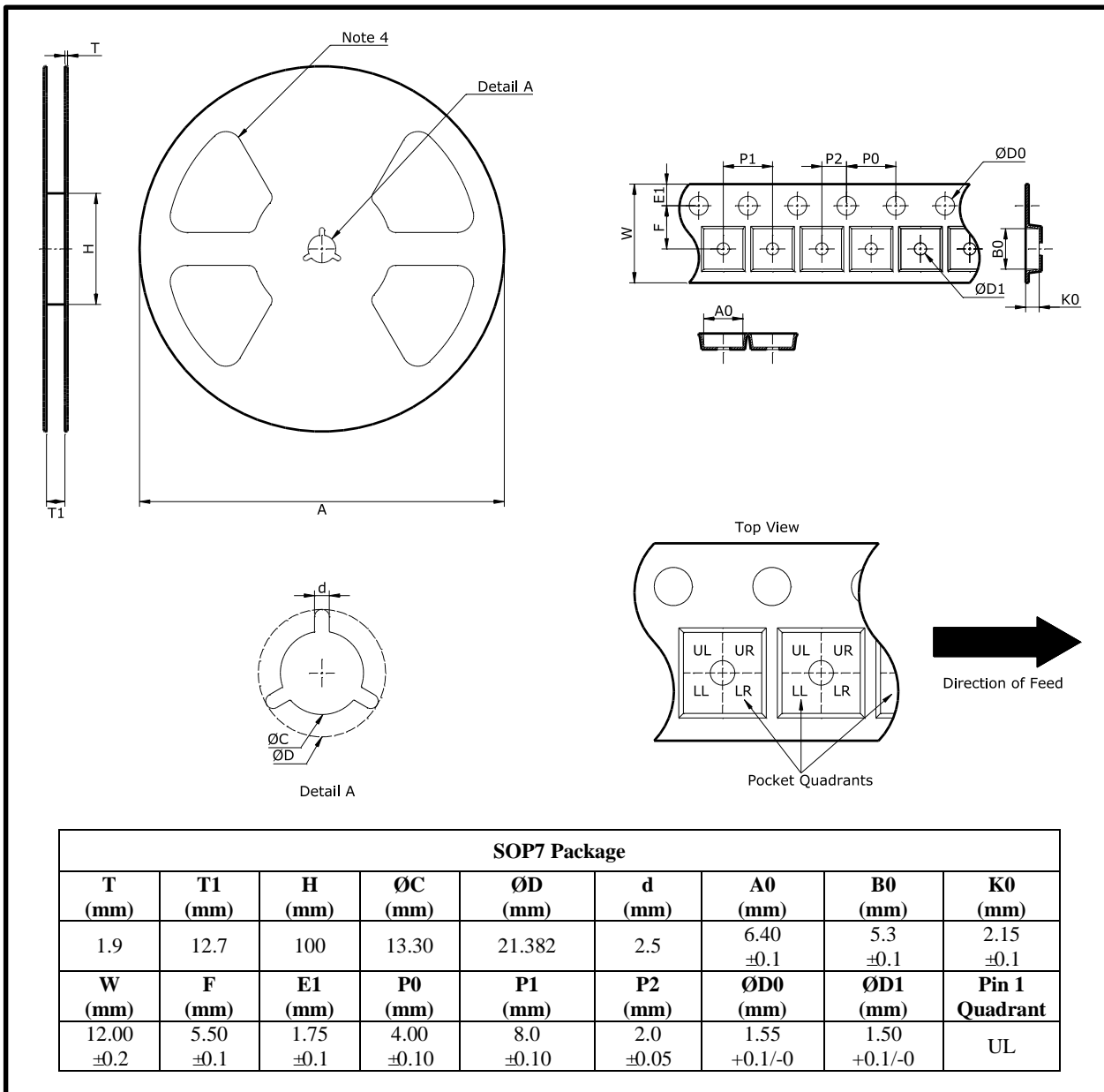
Top mark	Package
PN PN8571M YWWCXXXX	SOP7

Note: Y: Year Code; WW: Week Code; C: Version information; XXXX: Internal Code

Notes:

1. This drawing is subjected to change without notice.
2. Body dimensions do not include mold flash or protrusion.

## Tape and Reel Information



**Notes:**

1. This drawing is subjected to change without notice.
2. All dimensions are nominal and in mm.
3. This drawing is not in scale and for reference only. Customer can contact Chipown sales representative for further details.
4. The number of flange openings depends on the reel size and assembly site. This drawing shows an example only.

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