



PO3030K Data sheet



PO3030K 1/6.2 Inch VGA Single Chip CMOS IMAGE SENSOR

Rev 1.06

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CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

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**CMOS Image Sensor with 640 X 480 Pixel Array
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Table of Contents

Features	4
PIN Descriptions	5
Signal Environment	7
Chip Architecture	7
Frame Structure and Windowing	8
Data Formats	9
Data and Synchronization Timing	10
Video Mode and Still Image Capture Mode	12
Scaling	13
I2C Description	14
I2C Functional Description	15
Register Table	16
Register Descriptions	19
Electrical Characteristics	51
CLCC40Pin Package Specification	56
Application Note	57

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

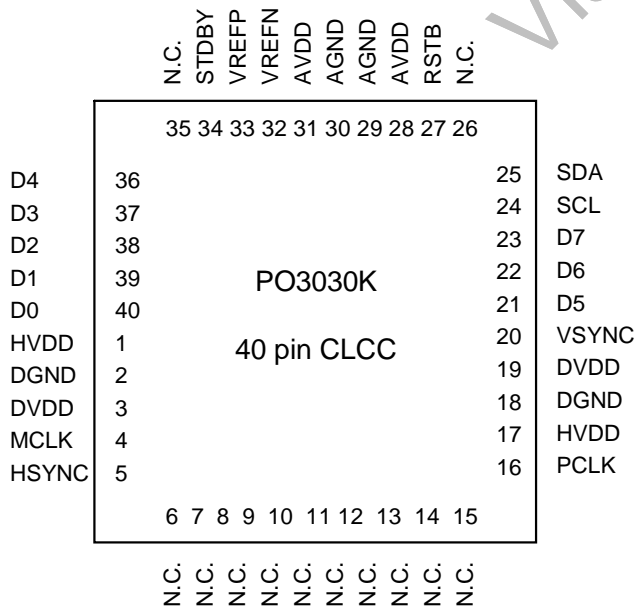
§ This document is an initial draft. It will be revised on without prior notice.
Contact Pixelplus for up-to-date information.

Features

- 1/ 6.2 inch 640 X 480 effective pixel array with color filters and micro-lens.
- Power supply 1.8V for core and 1.8 ~ 3.3V for I/O.
- Power down mode through pin or I2C register setting.
- Output formats : 8bit YCbCr / 8Bit Bayer data / 5:6:5 RGB / 8bit Y, CCIR 656
- 30 frames/sec progressive scan @27 MHz master clock.
- Image processing on chip : lens shading, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto white balance, auto exposure control and back light compensation.
- Still image capture with electrical shutter.
- Frame size, window size and position controllable through a serial interface bus.
- VGA / QVGA / QQVGA Scaling.
- Horizontal / Vertical mirroring.
- 50Hz, 60Hz flicker cancellation.
- Package : 40 pin CLCC, 32 pin CSP

Table 1. Typical Parameters

Total Pixel Array	648 X 488
Pixel Size	3.6um X 3.6um
Image Area	2.30 mm X 1.72 mm
Clock Rate	27MHz (Max.)
Frame rate	Variable up to 30fps
Dark Signal	9.24mV/sec
Sensitivity	1.9 V/Lux.sec @15fps, IR cut filter
Saturation Level	780 mV
Fill Factor	40 %
Supply voltage	1.8~3.3V I/O, 1.8V Core
Power consumption	23 mA @30fps, 2.5V I/O, active 10 uA @ standby
Operation Temp.	-30 ~ 50 °C
Dynamic Range	62 dB
SNR	TBD dB
Package	40 pin CLCC, 32 pin CSP



< Figure. 1> Pin Diagram

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

PIN Descriptions

Pin No.	Name	I/O Type	Functions / Descriptions
1	HVDD	P	Digital vdd for I/O : DC 1.8~3.3V. Voltage range for all output signals is 0V ~ HVDD.
2	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
3	DVDD	P	Digital vdd for core logic : 1.8V DC. 100nF capacitor to DGND.
4	MCLK	I	Master clock input pad.
5	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
6 - 15	N.C.	-	No Connection.
16	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled anyway.
17	HVDD	P	Digital vdd for I/O : DC 1.8~3.3V. Voltage range for all output signals is 0V ~ HVDD.
18	DGND	P	Digital ground. Core and I/O circuits share the ground pads.
19	DVDD	P	Digital vdd for core logic : 1.8V DC. 100nF capacitor to DGND.
20	VSYNC	O	Vertical sync : Indicates the start of a new frame.
21	D5	O	Bit 5 of data output.
22	D6	O	Bit 6 of data output.
23	D7	O	Bit 7 of data output.
24	SCL	I	I2C serial clock input.
25	SDA	I/O	I2C serial data bus.
26	N.C.	-	No Connection.
27	RSTB	I	System reset must remain low for at least 8 master clocks after power is stabilized. When the sensor is reset, all registers are set to their default values.
28	AVDD	P	Analog vdd : 1.8V DC. 100nF capacitor to AGND.
29	AGND	P	Analog ground.
30	AGND	P	Analog ground.
31	AVDD	P	Analog vdd : 1.8V DC. 100nF capacitor to AGND.

Table 2-1. PIN Descriptions

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Pin No.	Name	I/O Type	Functions / Descriptions
32	VREFN	O	ADC reference voltage. 100nF capacitor to AGND. ADC assumes VREFP – VREFN is the minimum input voltage that will be converted to 1FFh.
33	VREFP	O	ADC reference voltage. 100nF capacitor to AGND.
34	STDBY	I	Power standby mode. When STDBY='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<7:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state (Hi-Z). But it is possible to control internal registers through I2C bus interface in STDBY mode. All registers retain their current values.
35	N.C.	-	No Connection.
36	D4	O	Bit 4 of data output.
37	D3	O	Bit 3 of data output.
38	D2	O	Bit 2 of data output.
39	D1	O	Bit 1 of data output.
40	D0	O	Bit 0 of data output.

Table 2-2. PIN Descriptions

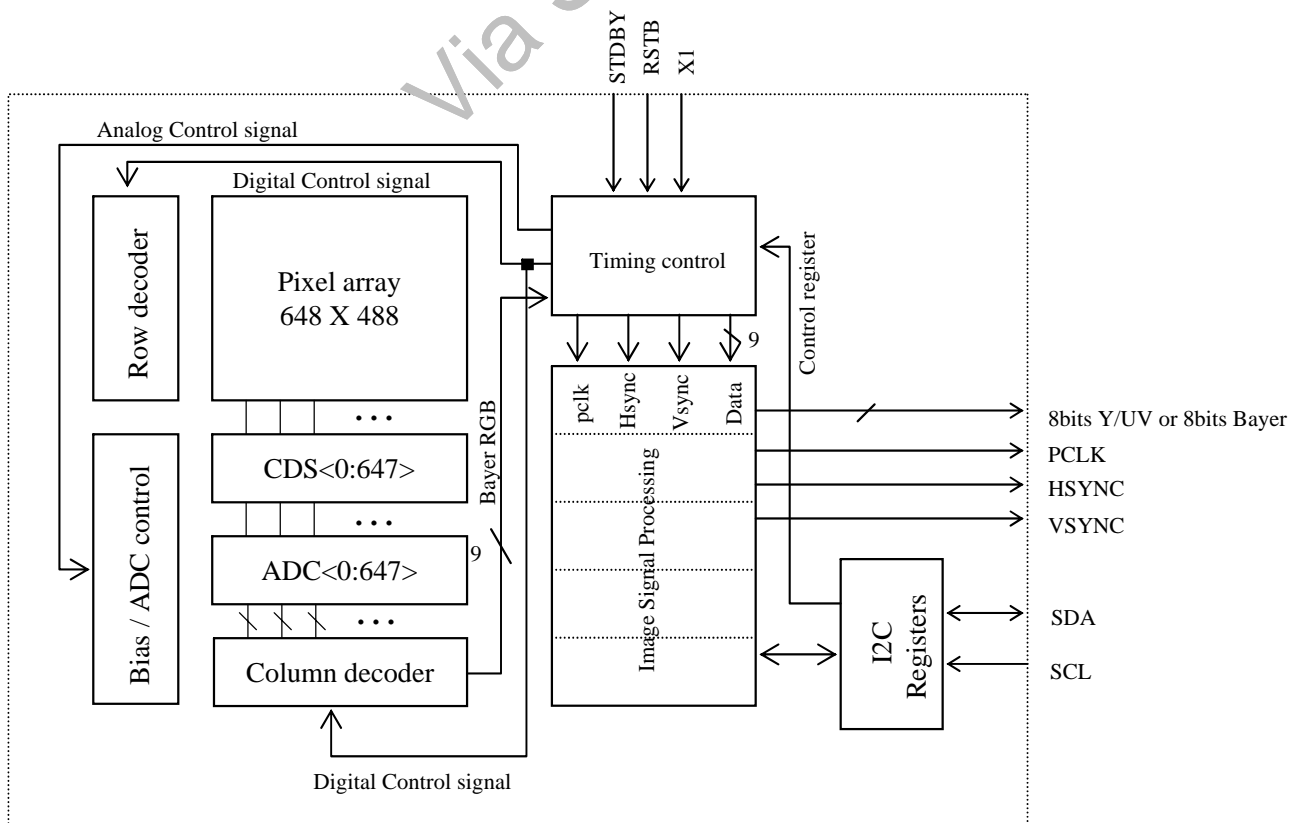
**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Signal Environment

PO3030K has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PO3030K input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

Chip Architecture

PO3030K has 648 x 488 effective pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through I²C serial interface.

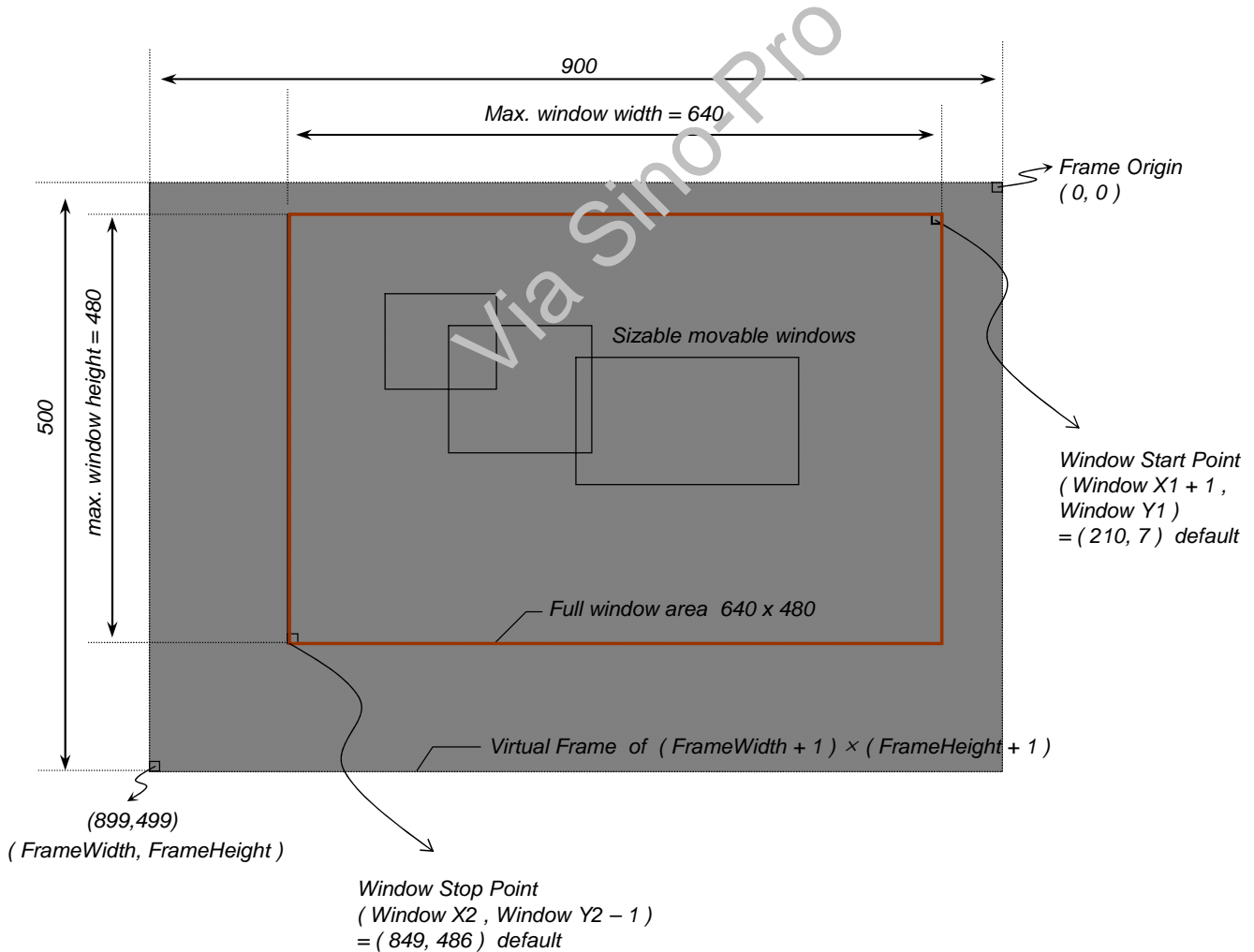


<Figure. 2> Block Diagram

**CMOS Image Sensor with 640 X 480 Pixel Array
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Frame Structure and Windowing

Origin (0, 0) of the frame is at the upper right corner. Size of the frame is determined by two registers : *FrameWidth* and *FrameHeight*. One frame consists of *FrameWidth* + 1 columns and *FrameHeight* + 1 rows. *FrameWidth* and *FrameHeight* can be programmed to be larger than physical array size. Physical array of 640 × 480 pixels is positioned at (210, 7). It is possible to define a specific region of the frame as a window. Pixel scanning begins from (0, 0) and proceeds row by row downward, and for each line scan direction is from right to the left. HSYNC signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *FrameHeight* , and 0 to *FrameWidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. (ref. regA5h ~ AAh) The pixel data rate is fixed and is independent of frame size (frame rate.)



< Fig. 3 > Default structure of frame and window. (Top view)

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Data Formats

Pixel array is covered by Bayer color filters as can be seen in the figure below. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PO3030K provides this Bayer pattern RGB data through an 8bit channel. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as

G1	R	G1	R
B	G2	B	G2
G1	R	G1	R
B	G2	B	G2

< Fig. 4> Bayer filter pattern

an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PO3030K adopts a low pass filter to prevent the interference patterns(called Moire pattern) from degrading the image quality too much.

For low grade display devices, it is not necessary to have 3 RGB data of all 8bit precision. PO3030K provides lower precision RGB data such that, 5bit R data and upper 3 bits of 6bit precision G data are passed first to output pins, and then the remaining 3 bits of G and 5 bit B data are routed outward. It takes two PCLK's to get 5:6:5 RGB data for each pixel.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : $Y = 0.299R + 0.587G + 0.114B$ where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$U = 0.492 (B - Y)$$

$$V = 0.877 (R - Y)$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

U1	Y1	V1	Y2	U3	Y3	V3	Y4	...
----	----	----	----	----	----	----	----	-----

< Fig. 5> 4:2:2 YUV data sequence.

PO3030K supports 4:2:2 YUV data format where U and V components are horizontally sub-sampled such that U and V for every other pixel are omitted. PO3030K also supports ITU-R BT.601 $Y_C B_C R_C$ format which is a scaled, offset version of YUV. Y is the same in both formats but the $C_B C_R$ is formed as follows.

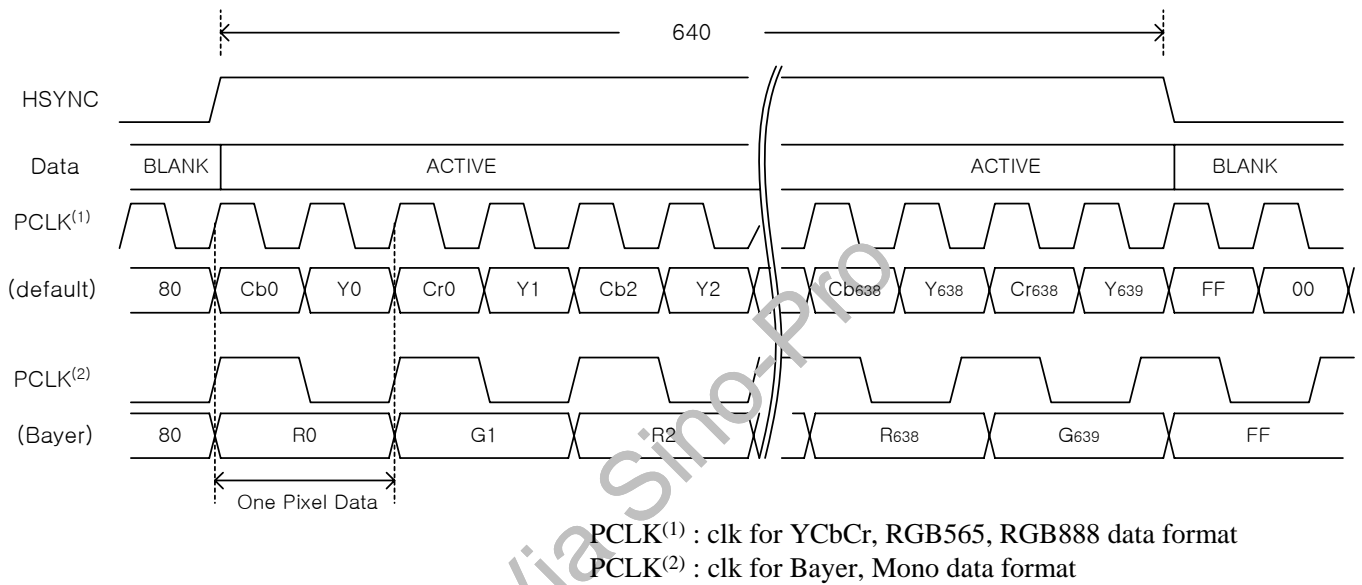
$$C_B = 0.564 (B - Y) + 128$$

$$C_R = 0.713 (R - Y) + 128$$

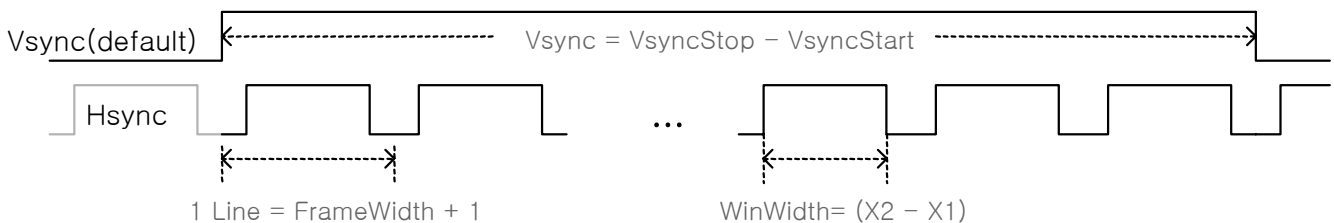
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and Integrated On-Chip Image Signal Processor**

Data and Synchronization Timing

In <Fig.6>, HSYNC / VSYNC / PCLK polarity can have any combinations possible (Except for RGB Bayer). Data can be latched at the rising or falling edge of PCLK. HSYNC and VSYNC can be set to be active high or active low. Every type of data (RGB or YUV) comes out at the fixed rate of PCLK, which can have the same or 1/2 ~ 1/128 the frequency of MCLK. The sequence RGB Raw Bayer data for even rows is RGRGRG... and for odd rows is GBGBGB....



< Figure. 6 > Timing diagram for HSYNC, PCLK and data

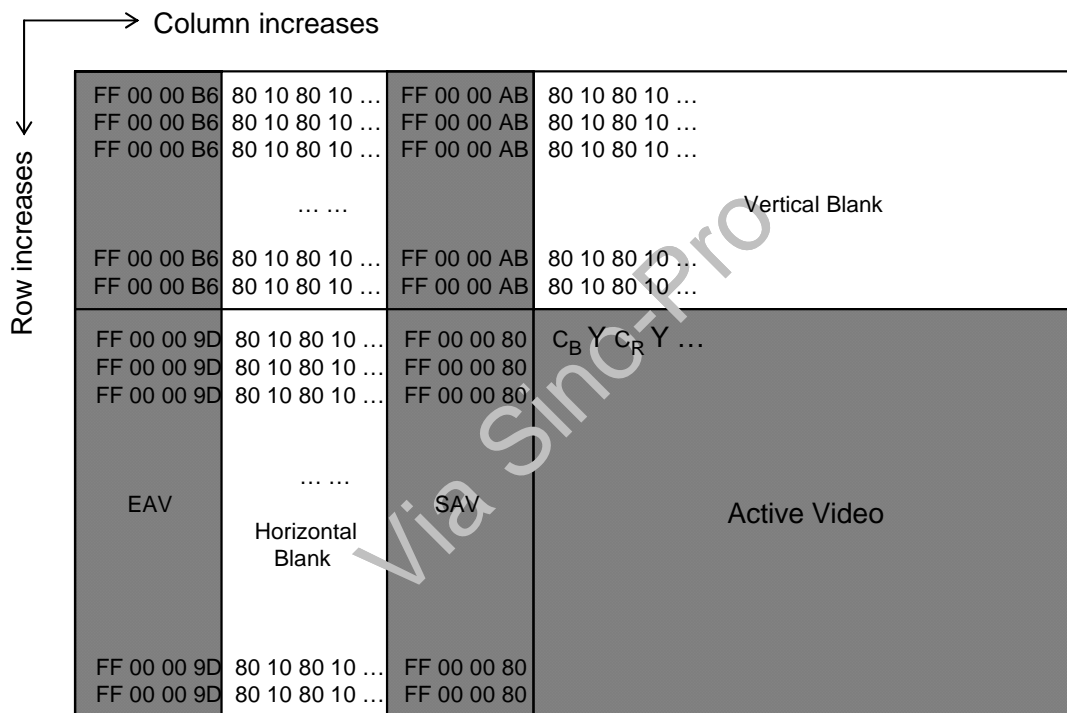


< Figure. 7 > Timing diagram for VSYNC and HSYNC

In <Fig.7>, The width of VSYNC can be controlled by VsyncStart/VsyncStop registers : Vsync Width = (VsyncStop - VsyncStart). The width of Hsync can be controlled by windowX1/X2 registers: Hsync Width = WindowX2 - WindowX1 (ref. reg08h ~ 0Fh, regA5h ~AAh descriptions)

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

In <Fig. 8>, EAV(End of Active Video) and SAV(Start of Active Video) signals are inserted for synchronization purposes. EAV is a 4 byte sequence of “FF 00 00 9D” for active lines, and “FF 00 00 B6” for blank lines. SAV is a 4 byte sequence of “FF 00 00 80” for active lines, and “FF 00 00 AB” for vertical blank lines. HSYNC signal is asserted right after the SAV sequence and de-asserted right before the EAV sequence. Horizontal and vertical blank area is repeatedly filled with “80 10”.



< Figure 8 > Frame data sequence including EAV and SAV.

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Video Mode(Preview Mode) and Still Image Capture Mode

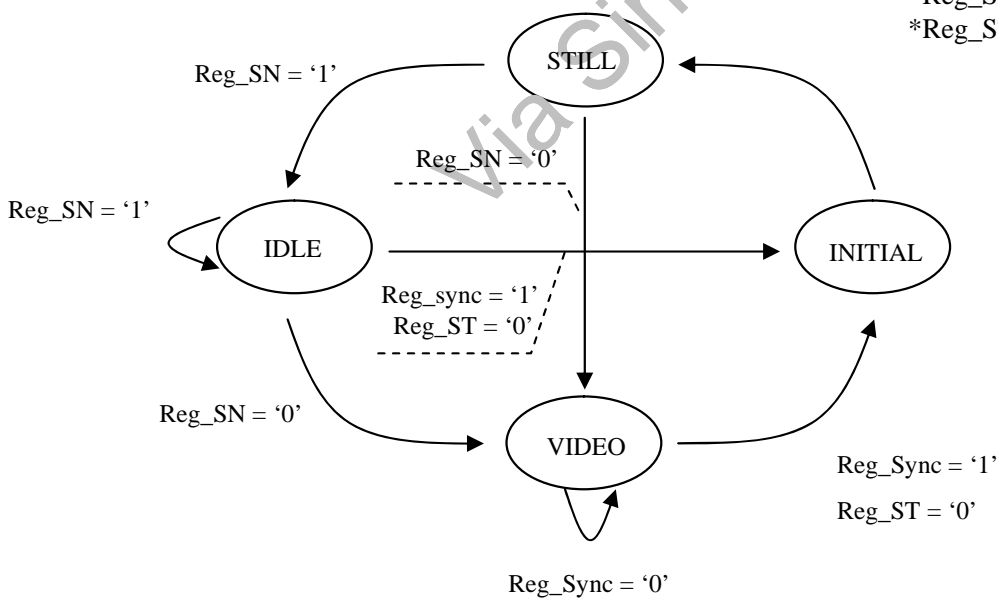
PO3030K normally operates in video mode. If you want to capture still image, User must do as follows.

- step1 : set register #20h (set appropriate register value : image resolution)
- step2 : set register #1Fh bit7 to '1'.

When bit7 of register 31d (1Fh) is set to '1', Sensor is under still state using electrical rolling shutter. After Still state, video mode may follow immediately or the sensor may be in idle state until an appropriate bit(reg_SN) is reset in the I²C register file. While the sensor is in idle state, there's no HSYNC or VSYNC pulse. Image resolution switch between video and still mode (for example, video in QVGA resolution and still image in VGA resolution) can be done manually or automatically.

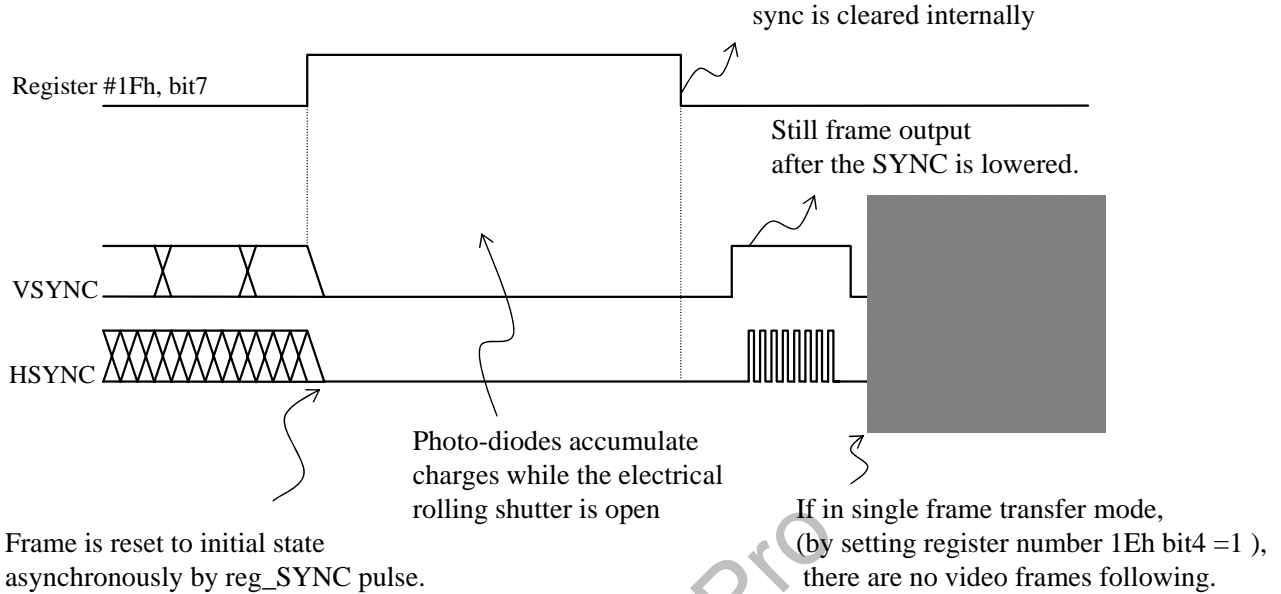
See Register description 1Eh.

- *Reg_SN means 1Eh bit4
- *Reg_ST means 1Eh bit5



< Figure 9 > Sensor state transition diagram

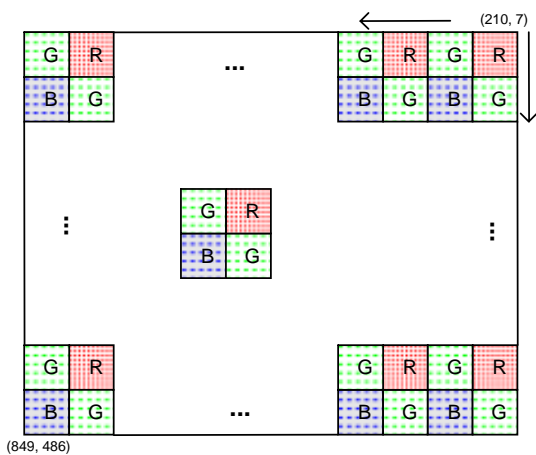
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and Integrated On-Chip Image Signal Processor**



<Figure 10> Still image capture with electrical shutter (register 1Eh bit5 = '0')

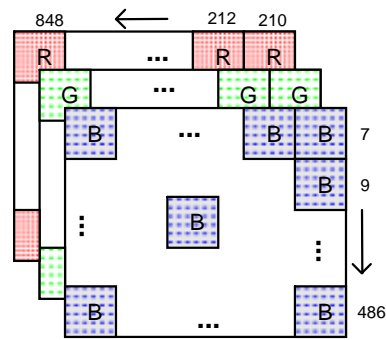
Scaling

PO3030K supports four modes of scaling : 1/4 scaling, 1/16 scaling. Figure 12 shows the scaling four modes. (Ref. reg20h)

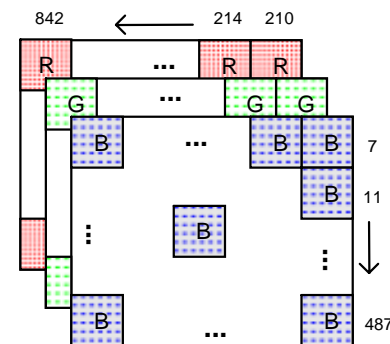


a. Normal Bayer Pattern

< Figure 11 > 1/4 , 1/16 Scaling



b. 1/4 scaling



c. 1/16 scaling

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

I2C Description

The registers of PO3030K are written and read through the I²C interface. The PO3030K has I²C slave. The PO3030K is controlled by the I²C clock (SCL), which is driven by the I²C master. Data is transferred into and out of the PO3030K through the I²C data (SDA) line. The SCL and SDA lines are pulled up to VDD by a 2k Ω off-chip resistor. Either the slave or master device can pull the lines down. The I²C protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of an I²C device consists of 7 bits of address and 1 bit of direction. A 0 in the LSB of the address indicates write mode, and a 1 indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The I²C clock pulse is provided by the master. The data must be stable during the HIGH period of the I²C clock : it can only change when the I²C clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a 0 indicates a write and a 1 indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PO3030K uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

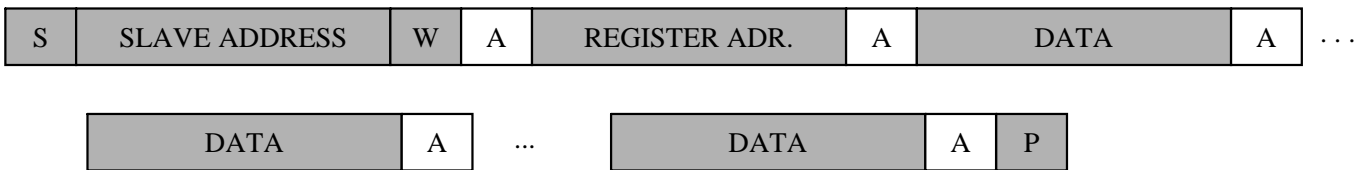
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and Integrated On-Chip Image Signal Processor**

I2C Functional Description

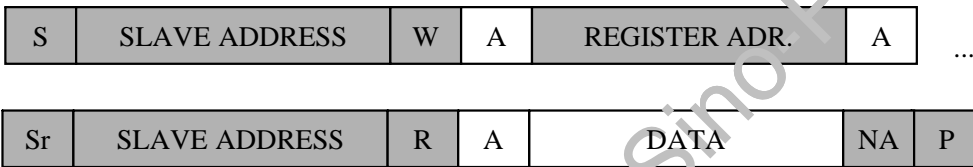
Single Write Mode operation



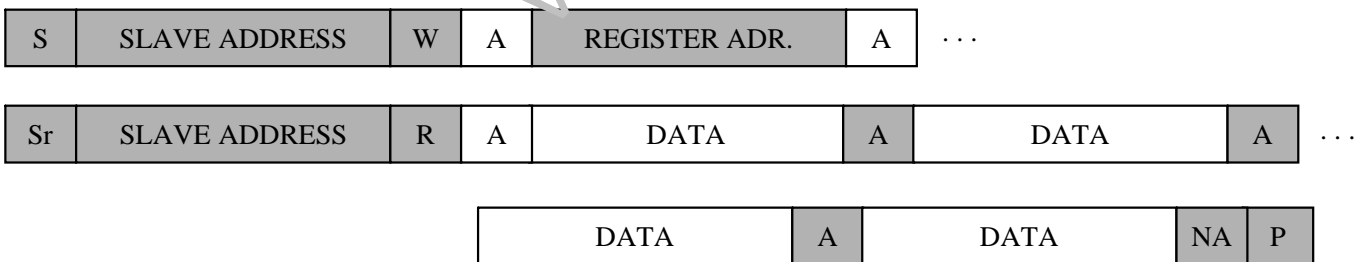
Multiple Write Mode (Register address is increased automatically)¹ operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)¹ operation



S: Start condition. Sr : Repeated Start (Start without preceding stop.)
 SLAVE ADDRESS: write address = DCh = 11011100b
 read address = DDh = 11011101b
 R/W: Read/Write selection. High = read / LOW = write.
 A: Acknowledge bit. NA : No Acknowledge.
 DATA: 8-bit data
 P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Register Table

Address	Name	R/W	Default Value	Description
0 (00h)	DeviceID_H	R	00110000 (30h)	PO3030K Device ID
1 (01h)	DeviceID_L	R	00110000 (30h)	
2 (02h)	RevNumber	R	00000001 (01h)	Revision Number
4 (04h)	FrameWidth_H	RW	xx000011 (03h)	Frame Width = 899d (0383h)
5 (05h)	FrameWidth_L	RW	10000011 (83h)	
6 (06h)	FrameHeight_H	RW	xx000001 (01h)	Frame Height = 499d (01F3h)
7 (07h)	FrameHeight_L	RW	11110011 (F3h)	
8 (08h)	WindowX1_H	RW	00000000 (00h)	Window X1 = 209d (00D1h)
9 (09h)	WindowX1_L	RW	11010001 (D1h)	
10 (0Ah)	WindowY1_H	RW	00000000 (00h)	Window Y1 = 7d (0007h)
11 (0Bh)	WindowY1_L	RW	00000111 (07h)	
12 (0Ch)	WindowX2_H	RW	00000011 (03h)	Window X2 = 849d (0351h)
13 (0Dh)	WindowX2_L	RW	01010001 (51h)	
14 (0Eh)	WindowY2_H	RW	00000001 (01h)	Window Y2 = 487d (01E7h)
15 (0Fh)	WindowY2_L	RW	11100111 (E7h)	
18 (12h)	AmpBias	RW	xxxx0010 (02h)	Global Current Bias
19 (13h)	PixelBias	RW	xxxx0010 (02h)	Pixel Array Current Bias
21 (15h)	GlobalGain	RW	00000000 (00h)	Gain Factor that is Common to R, G, B
22 (16h)	RedGain	RW	01000000 (40h)	R Pixel Gain Factor
23 (17h)	Green1Gain	RW	01000000 (40h)	G1 Pixel Gain Factor
24 (18h)	BlueGain	RW	01000000 (40h)	B Pixel Gain Factor
25 (19h)	Green2Gain	RW	01000000 (40h)	G2 Pixel Gain Factor
26 (1Ah)	IntTime_H	RW	xx000000 (00h)	Pixel Integration Time
27 (1Bh)	IntTime_M	RW	10000000 (80h)	
28 (1Ch)	IntTime_L	RW	000000xx (00h)	
29 (1Dh)	Tgcontrol1	RW	00000000 (00h)	TG Control
30 (1Eh)	Tgcontrol2	RW	00001010 (0Ah)	
31 (1Fh)	Tgcontrol3	RW	00011011 (1Bh)	
32 (20h)	Tgcontrol4	RW	01000100 (44h)	
59 (3Bh)	ADCOffset	RW	00000000 (00h)	ADC offset
70 (46h)	FdControl	RW	00000000 (00h)	Flicker Control Register
72 (48h)	regclk167	RW	10101111 (AFh)	# master clock for flicker detection standard time
73 (49h)	Period50H	RW	10010110 (96h)	Flicker Period(50Hz)
74 (4Ah)	Period50L	RW	00000000 (00h)	
75 (4Bh)	Period60H	RW	01111101 (7Dh)	Flicker Period(60Hz)
76 (4Ch)	Period60L	RW	00000000 (00h)	
78 (4Eh)	IspControl2	RW	00000000 (00h)	ISP Control Registers
79 (4Fh)	IspControl3	RW	00001010 (0Ah)	
80 (50h)	IspControl4	RW	01110000 (70h)	
89 (59h)	LensRGain	RW	xxxx0000 (00h)	
90 (5Ah)	LensGGain	RW	xxxx0000 (00h)	Lens Shading Green Gain
91 (5Bh)	LensBGain	RW	xxxx0000 (00h)	Lens Shading Blue Gain
92 (5Ch)	EdgeControl	RW	10101100 (ACh)	Moire Suppression & Edge Enhancement Factor
93 (5Dh)	EdgeTh	RW	00000010 (02h)	Edge Enhancement Threshold
118 (76h)	GmCoeff0	RW	00000000 (00h)	Gamma Coefficients
119 (77h)	GmCoeff1	RW	00011010 (1Ah)	
120 (78h)	GmCoeff2	RW	00101010 (2Ah)	
121 (79h)	GmCoeff3	RW	00110111 (37h)	
122 (7Ah)	GmCoeff4	RW	01000010 (42h)	
123 (7Bh)	GmCoeff5	RW	01010110 (56h)	
124 (7Ch)	GmCoeff6	RW	01101000 (68h)	

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Address	Name	R/W	Default Value	Description
125 (7Dh)	GmCoeff7	RW	10000111 (87h)	Gamma Coefficients
126 (7Eh)	GmCoeff8	RW	10100011 (A3h)	
127 (7Fh)	GmCoeff9	RW	10111100 (BCh)	
128 (80h)	GmCoeff10	RW	11010100 (D4h)	
129 (81h)	GmCoeff11	RW	11101010 (EAh)	
142 (8Eh)	ColorMatrix1	RW	00111000 (38h)	Color Correction Coefficients
143 (8Fh)	ColorMatrix2	RW	10100101 (A5h)	
144 (90h)	ColorMatrix3	RW	00001101 (0Dh)	
145 (91h)	ColorMatrix21	RW	10010011 (93h)	
146 (92h)	ColorMatrix22	RW	00101101 (2Dh)	
147 (93h)	ColorMatrix23	RW	00000110 (06h)	
148 (94h)	ColorMatrix31	RW	10000011 (83h)	
149 (95h)	ColorMatrix32	RW	10101010 (AAh)	
150 (96h)	ColorMatrix33	RW	01001101 (4Dh)	
151 (97h)	CG11C	RW	00100101 (25h)	Cb Color Gain
152 (98h)	CG22C	RW	00100101 (25h)	Cr Color Gain
155 (9Bh)	Bright	RW	00000000 (00h)	Y Brightness
156 (9Ch)	Contrast	RW	10010110 (96h)	Y Contrast
159 (9Fh)	CbTone	RW	10000000 (80h)	Cb sepia Data
160 (A0h)	CrTone	RW	10000000 (80h)	Cr sepia Data
161 (A1h)	BlankEAV	RW	10110110 (E0h)	CCIR 656 synchronization purposes
162 (A2h)	ActiveEAV	RW	10011101 (9Dh)	
163 (A3h)	BlankSAV	RW	10101011 (ABh)	
164 (A4h)	ActiveSAV	RW	10000000 (80h)	
165 (A5h)	VsyncStart_H	RW	00000000 (00h)	
166 (A6h)	VsyncStart_L	RW	00000111 (07h)	Out Vsync Row Start = 7d (0007h)
167 (A7h)	VsyncStop_H	RW	00000001 (01h)	Out Vsync Row Stop = 487d (001E7h)
168 (A8h)	VsyncStop_L	RW	11100111 (E7h)	
169 (A9h)	VsyncColumn_H	RW	00000000 (00h)	Out Vsync Column Start = 1d (0001h)
170 (AAh)	VsyncColumn_L	RW	00000001 (01h)	
173 (ADh)	ww control	RW	10011111 (9Fh)	weight window control
174 (AEh)	AE_lock	RW	00100010 (22h)	Auto Exposure Lock range
175 (AFh)	AE_speed	RW	10001100 (8Ch)	Auto Exposure speed
176 (B0h)	Exposure_H	RW	00000000 (00h)	Exposure
177 (B1h)	Exposure_M	RW	10000000 (80h)	
178 (B2h)	Exposure_L	RW	00000000 (00h)	
179 (B3h)	TargetExp	RW	01110000 (70h)	Y Bright Target
185 (B9h)	MaxFrmHeight_H	RW	00000011 (03h)	Maximum Frame Height
186 (BAh)	MaxFrmHeight_L	RW	11100110 (E6h)	
187 (BBh)	MaxExp_H	RW	00000111 (07h)	Maximum Exposure Time
188 (BCh)	MaxExp_M	RW	11001100 (CCh)	
189 (BDh)	MinExp_M	RW	00000000 (00h)	Minimum Exposure Time
190 (BEh)	MinExp_L	RW	00001100 (0Ch)	
193 (C1h)	RMinAwb	RW	00010000 (10h)	Minimum AWB R Gain
194 (C2h)	RMaxAwb	RW	11100000 (E0h)	Maximum AWB R Gain
195 (C3h)	BMinAwb	RW	00010000 (10h)	Minimum AWB B Gain
196 (C4h)	BMaxAwb	RW	11100000 (E0h)	Maximum AWB B Gain
197 (C5h)	Awb_rgratio	RW	10000000 (80h)	AWB Red Gain ratio
198 (C6h)	Awb_bgratio	RW	10000000 (80h)	AWB Blue Gain ratio
199 (C7h)	weightx1_H	RW	00000001 (01h)	Weight Window : X1 = 421d(01A5h)
200 (C8h)	weightx1_L	RW	10100101 (A5h)	
201 (C9h)	weightx2_H	RW	00000010 (02h)	Weight Window : X2 = 634d(027Ah)
202 (CAh)	weightx2_L	RW	01111010 (7Ah)	

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Address	Name	R/W	Default Value		Description
203 (CBh)	weighty1_H	RW	00000000	(00h)	Weight Window : Y1 = 167d(00A7h)
204 (CCh)	weighty1_L	RW	10100111	(A7h)	
205 (CDh)	weighty2_H	RW	00000001	(01h)	Weight Window : Y2 = 327d(0147h)
206 (CEh)	weighty2_L	RW	01000111	(47h)	
212 (D4h)	Auto Control	RW	00111100	(3Ch)	AE / AWB enable
216 (D8h)	Gamma control	RW	10000000	(80h)	Gamma curve selection

Via Sino-Pro

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Register Descriptions

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 8 master clock periods. This will initialize all of the registers to their default values.

(0-2) DeviceID, RevNumber

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
00h	0	0	1	1	0	0	0	0	R
01h	0	0	1	1	0	0	0	0	
02h	X	X	X	X	0	0	0	1	

Default : 00h = 30h, 01h = 30h, 02h = 01h

Description :

Indicate PO3030K (Rev.1) device ID, reversion number.

(4-5) Frame Width

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
04h	X	X	0	0	0	0	1	1	RW
05h	1	0	0	0	0	0	1	1	

Default : 04h = 03h, 05h = 83h Frame Width = 899d

Description :

Frame Width is the number of columns to be counted during one line time. Column counter value is incremented 1 by 1 until it reaches *Frame Width*, then it is reset to 0. It can be larger than physical frame width but cannot be smaller.

Frame Height and *Frame Width* determines the frame rate. Frame rate is given

as

$$\text{freq(MCLK)} / ((\text{Frame Height} + 1) \times (\text{Frame Width} + 1) \times 2)$$

For example, freq.MCLK = 27 MHz, *Frame Height* = 499 and *Frame Width* = 899. then, the frame rate is 30 fps. If you double the *Frame Width*, you cut the frame rate by half. *Frame Width* value must be set with respect to the full sampling mode. Changing to 1/4 or 1/16 sub-sampling mode does not require any change in *Frame Width*.

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(6-7) Frame Height

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
06h	X	X	0	0	0	0	0	1	RW
07h	1	1	1	1	0	0	1	1	

Default : 06h = 01h, 07h = F3h Frame Height = 499d

Description :

Frame Height is the number of rows to be counted during one frame time. Row counter value is incremented 1 by 1 until it reaches *Frame Height*, then it is reset to 0. It can be larger than physical frame height but cannot be smaller.

Frame Height and *Frame Width* determines the frame rate. Frame rate is given as

$$\text{freq(MCLK)} / ((\text{Frame Height} + 1) \times (\text{Frame Width} + 1) \times 2)$$

For example, freq.MCLK = 27 MHz, *Frame Height* = 499 and *Frame Width* = 899. then, the frame rate is 30 fps. If you double the *Frame Height*, you cut the frame rate by half, and the vertical blank time is increased, but the PCLK rate does not change.

(8-9) WindowX1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
08h	0	0	0	0	0	0	0	0	RW
09h	1	1	0	1	0	0	0	1	

Default : 08h = 00h, 09h = D1h WindowX1 = 209d

Description :

Window can be defined by 4 parameters : *WindowX1*, *WindowY1*, *WindowX2*, and *WindowY2*. Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. HSYNC signal indicates if the image data output is from a pixel that lies within the window area or not.

Output data stream does not stop for pixels lying outside the window : just the HSYNC signal is de-asserted. The actual window position in the frame is given as

$$\text{upper right corner} = (\text{Window X1} + 1, \text{Window Y1})$$

$$\text{lower left corner} = (\text{Window X2}, \text{Window Y2} - 1)$$

All the coordinates are with respect to the maximum window origin (0, 0) of Figure 3. Window position and size is with respect to the full sampling mode. It is not necessary to change the window parameters when sampling mode is switched between one and another.

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

(10-11) WindowY1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Ah	0	0	0	0	0	0	0	0	RW
0Bh	0	0	0	0	0	1	1	1	

Default : 0Ah = 00h, 0Bh = 07h WindowY1 = 7d

Description : refer to *Window X1*

(12-13) WindowX2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Ch	0	0	0	0	0	0	1	1	RW
0Dh	0	1	0	1	0	0	0	1	

Default : 0Ch = 03h, 0Dh = 51h WindowX2 = 849d

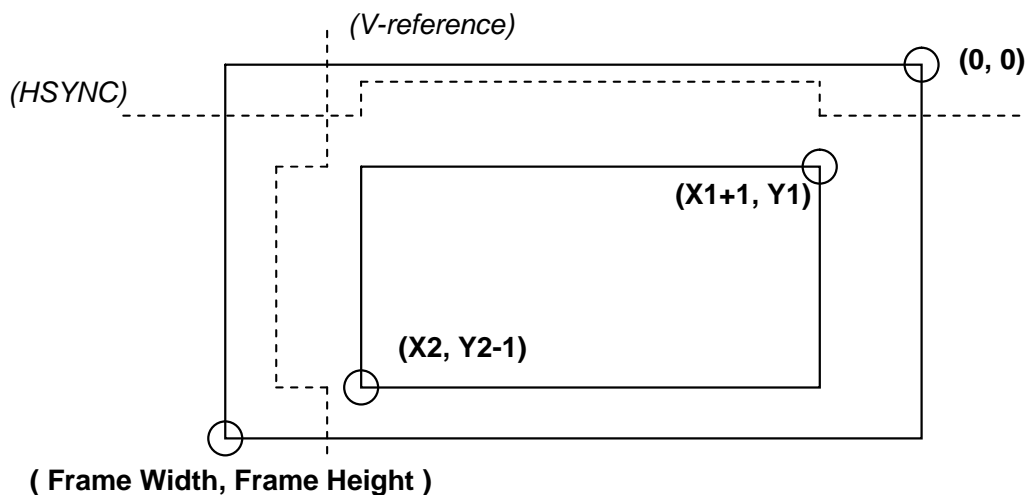
Description : refer to *Window X1*

(14-15) WindowY2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
0Eh	0	0	0	0	0	0	0	1	RW
0Fh	1	1	1	0	0	1	1	1	

Default : 0Eh = 01h, 0Fh = E7h WindowY2 = 487d

Description : refer to *Window X1*



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(18) Amp Bias

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
12h	X	X	X	X	0	0	1	0	RW

Default : 12h = 02h

Description :

All analog circuits such as opamp or reference voltage generators are biased using current mirrors. Current flowing in every branch of analog circuits is an integral multiple of 1uA.

$$I_{branch} = (Global I Bias) * 1uA$$

If an opamp has 4 branches and *Global I Bias* is set to 2, then the amplifier consumes total current of 8uA . As the current increases, frequency response of opamp improves and better images can be obtained, but the power consumption also increases.

(19) Pixel Bias

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
13h	X	X	X	X	0	0	1	0	RW

Default : 13h = 02h

Description :

Pixel array has a source follower circuit for each column to buffer the photo-diode signal voltage. The source follower bias current is determined as an integral multiple of 1uA.

$$I_{pixel} = PixelBias * 1uA$$

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

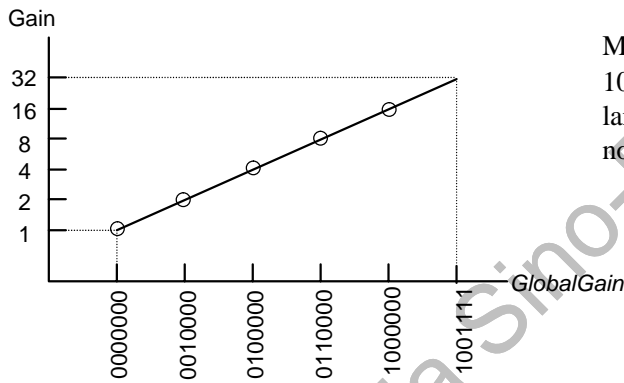
(21) Global Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
15h	0	0	0	0	0	0	0	0	RW

Default : 15h = 00h

Description :

Global Gain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of *Global Gain*. The relation between *Global Gain* and amplification factor is shown in the picture below.



Maximum value of *Global Gain* is 1001111. Gain factors for *GlobalGain* larger than or equal to 1010000 are not defined.

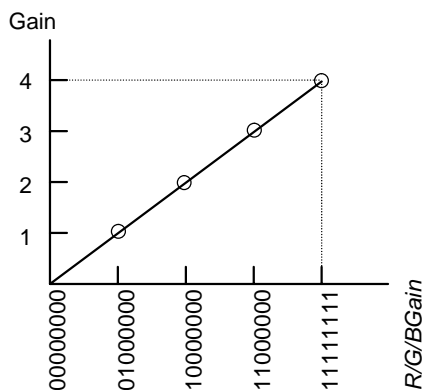
(22) Red Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
16h	0	1	0	0	0	0	0	0	RW

Default : 16h = 40h

Description :

RGain is the multiplication factor for red pixel output. Total gain factor for red pixels is (gain from *Global Gain*) * (gain from *RGain*).



R / G / B gain can be used for white balance control. Bit7 of *R/G/BGain* is weighted by 2, bit6 by 1 and the other consecutive bits are weighted by 1/2, 1/4, 1/8, ... respectively. That is, *R/G/Bgain* is a binary number with decimal point between bit6 and bit5.

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(23) Green 1 Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
17h	0	1	0	0	0	0	0	0	RW

Default : 17h = 40h

Description :

G1 pixels are those green pixels whose nearest neighbors are red pixels.

Refer to *Red Gain(16h)* register description.

(24) Blue Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
18h	0	1	0	0	0	0	0	0	RW

Default : 18h = 40h

Description : refer to *Red Gain(16h)* register description.

(25) Green 2 Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
19h	0	1	0	0	0	0	0	0	RW

Default : 19h = 40h

Description :

G2 pixels are those green pixels whose nearest neighbors are blue pixels.

Refer to *Red Gain(16h)* register description.

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

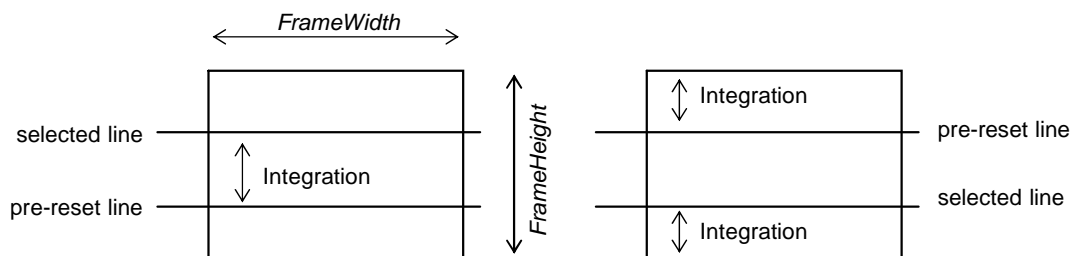
(26-28) Integration Time

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Ah	X	X	0	0	0	0	0	0	RW
1Bh	1	0	0	0	0	0	0	0	
1Ch	0	0	0	0	0	0	X	X	

Default : 1Ah = 00h, 1Bh = 80h, 1Ch = 00h, Integration Time = 8192d

Description :

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. 1Ah and 1Bh registers indicate how many line times the integration will continue until they are all reset. 1Ch register further sub-divides one line time into 64 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time. As the row counter value is incremented from 0 to *Frame Height*, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read-out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states. To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PO3030K is 1/ 64 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line

Case 2. Select line preceding reset line

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(29) Timing Generator Control Register 1

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Dh	Drop	CK2	CK1	CK0	X	X	X	X	RW
	0	0	0	0	X	X	X	X	

Default : 1Dh = 00h

Description :

Bit name	value	Description
Drop	0	Frame Drop Disable.
	1	Frame Drop Enable.
CK(2:0)	000	Internal clock = (external master clock) x 1 / 2 (Default)
	001	Internal clock = (external master clock) x 1 / 3
	010	Internal clock = (external master clock) x 1 / 4
	011	Internal clock = (external master clock) x 1 / 8
	100	Internal clock = (external master clock) x 1 / 16
	101	Internal clock = (external master clock) x 1 / 32
	110	Internal clock = (external master clock) x 1 / 64
	111	Internal clock = (external master clock) x 1 / 128

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(30) Timing Generator Control Register 2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Eh	HM	VM	ST	SN	RSV	RSV	RSV	RSV	RW
	0	0	0	0	1	0	1	0	

Default : 1Eh = 0Ah

Description :

Bit name	value	Description
HM	0	Horizontal Mirror Disable. (<i>default</i>)
	1	Horizontal Mirror Enable.
VM	0	Vertical Mirror Disable (<i>default</i>)
	1	Vertical Mirror Enable.
ST	0	Electrical Shutter Selection (<i>default</i>)
	1	Mechanical Shutter Selection (<i>not available</i>)
SN	0	single still image output disable (default)
	1	single still image output enable

(31) Timing Generator Control Register 3

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
1Fh	sync	stdby	X	RSV	RSV	RSV	RSV	RSV	RW
	0	0	X	1	1	0	1	1	

Default : 1Fh = 1Bh

Description :

Bit name	value	Description
sync	0	Sync input register
stdby	0	Stdby input register

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(32) Timing Generator Control Register 4

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
20h	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0	RW
	0	1	0	0	0	1	0	0	

Default : 20h = 44h

Description :

MSB 4 bits control sub sampling mode under Video State, while LSB 4bits under Still State.

Under Video State

- Sensor Full sampling mode. (frame rate constant)
- sm(7 : 4) : "X1XX" => VGA
- sm(7 : 4) : "X001" => QVGA
- sm(7 : 4) : "X011" => QQVGA

Under Still State,

- Sensor Full sampling mode. (frame rate constant)
- sm(3 : 0) : "X1XX" => VGA
- sm(3 : 0) : "X001" => QVGA
- sm(3 : 0) : "X011" => QQVGA

(59) ADC offset

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
3Bh	0	0	0	0	0	0	0	0	RW

Default : 3Bh = 00h

Description :

ADC offset value.

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(70) Flicker Control Register

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
46h	AF	F5	F6	FDM	FK1	FK0	FL1	FL0	RW
	0	0	0	0	0	0	0	0	

Default : 46h = 00h

Description :

Bit name	value	Description
AF	0	Manual Flicker Detection Enable Mode.
	1	Auto Flicker Detection Enable Mode
F5	0	50Hz Flicker Detection Mode Disable
	1	50Hz Flicker Detection Mode Enable
F6	0	60Hz Flicker Detection Mode Disable
	1	60Hz Flicker Detection Mode Enable
FDM	0	Flicker Duration long lasting Mode
	1	Flicker Duration only while the flicker exists.
FK (1:0)	00	Flicker Count Increase/Decrease step '0'.
	01	Flicker Count Increase/Decrease step '1'.
	10	Flicker Count Increase/Decrease step '2'.
	11	Flicker Count Increase/Decrease step '3'.
FL(1:0)	00	Flicker Tolerance '0'
	01	Flicker Tolerance '1'
	10	Flicker Tolerance '2'
	11	Flicker Tolerance '3'

FDM : flicker duration mode='0' : long lasting mode

flicker duration mode='1' : only while the flicker exists.

Auto Detect Setting : 60 or 50 Hz AF = '1', F6 = '0', F5 = '0'

60Hz : AF = '1', F6 = '1', F5 = '0'

50Hz : AF = '1', F6 = '0', F5 = '1'

Manual Setting 60Hz : AF = '0', F6 = '1', F5 = '0'

50Hz : AF = '0', F6 = '0', F5 = '1'

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

(72) Regclk167

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
48h	1	0	1	0	1	1	1	1	RW

Default : 48h = AFh

Description :

of Master clock for flicker detection standard time or 1.667 ms time ratio

$$\text{Regclk167} = 1.667\text{ms} / (\text{master clock period} \times 256)$$

(73-76) Flicker Free Mode Period

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
49h	1	0	0	1	0	1	1	0	RW
4Ah	0	0	0	0	0	0	0	0	
4Bh	0	1	1	1	1	1	0	1	
4Ch	0	0	0	0	0	0	0	0	

Default : 49h = 96h, 4Ah = 00h, 4Bh = 7Dh, 4Ch = 00h

Description :

Address	Name	Function
49h	period50 (H)	Flicker Period Control register for 50Hz light source
4Ah	period50 (L)	
4Bh	period60 (H)	Flicker Period Control register for 60Hz light source
4Ch	period60 (L)	

Refer to the application note for the calculation method of flicker free period.

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

(78) Image Signal Processor control 2 : ISP Control 2

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
4Eh	CEN	OCF2	OCF1	OCF0	ODF3	ODF2	ODF1	ODF0	RW
	0	0	0	0	0	0	0	0	

Default : 4Eh = 00h

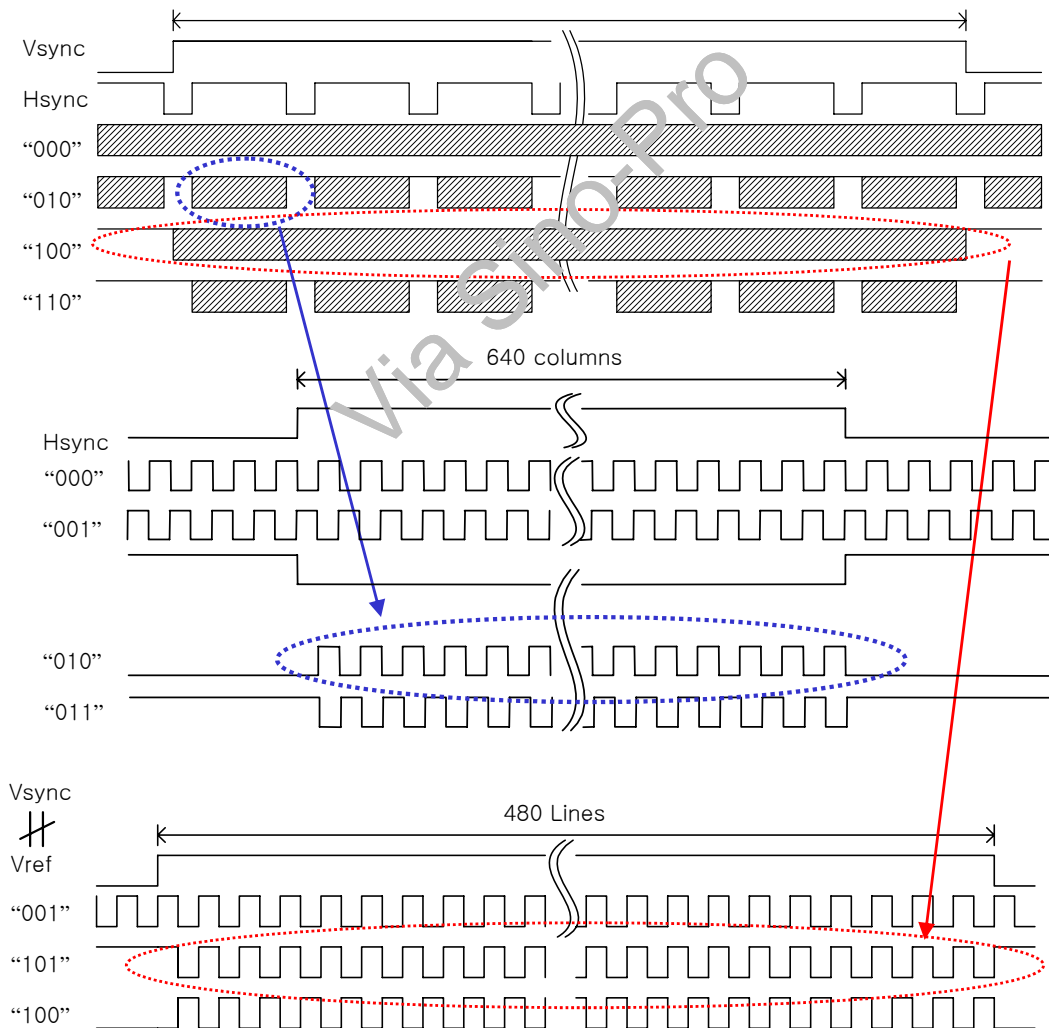
Description :

Bit name	value	Description
CEN	0	Normal condition. <i>(default)</i>
	1	Out Clock set to ground.
OCF[6:4]		Out Clock format Control
	000	Normal. <i>(default)</i>
	001	Invert.
	010	& H-ref
	011	invert & H-ref
	100	& V-ref
	101	invert & V-ref
	110	& H-ref & Vref
111	invert & H-ref & V-ref	
ODF[3:0]		Out Data Format
	0000	CB Y CR Y ... <i>(default)</i>
	0001	CR Y CB Y ...
	0010	Y CB Y CR ...
	0011	Y CR Y CB...
	0100	RGRG...GBGB ...
	0101	GBGB...RGRG ...
	0110	GRGR...BGBG ...
	0111	BGBG...GRGR ...
	1000	R5G3, G3B5
	1001	B5G3, G3R5
	1100	YYYY...

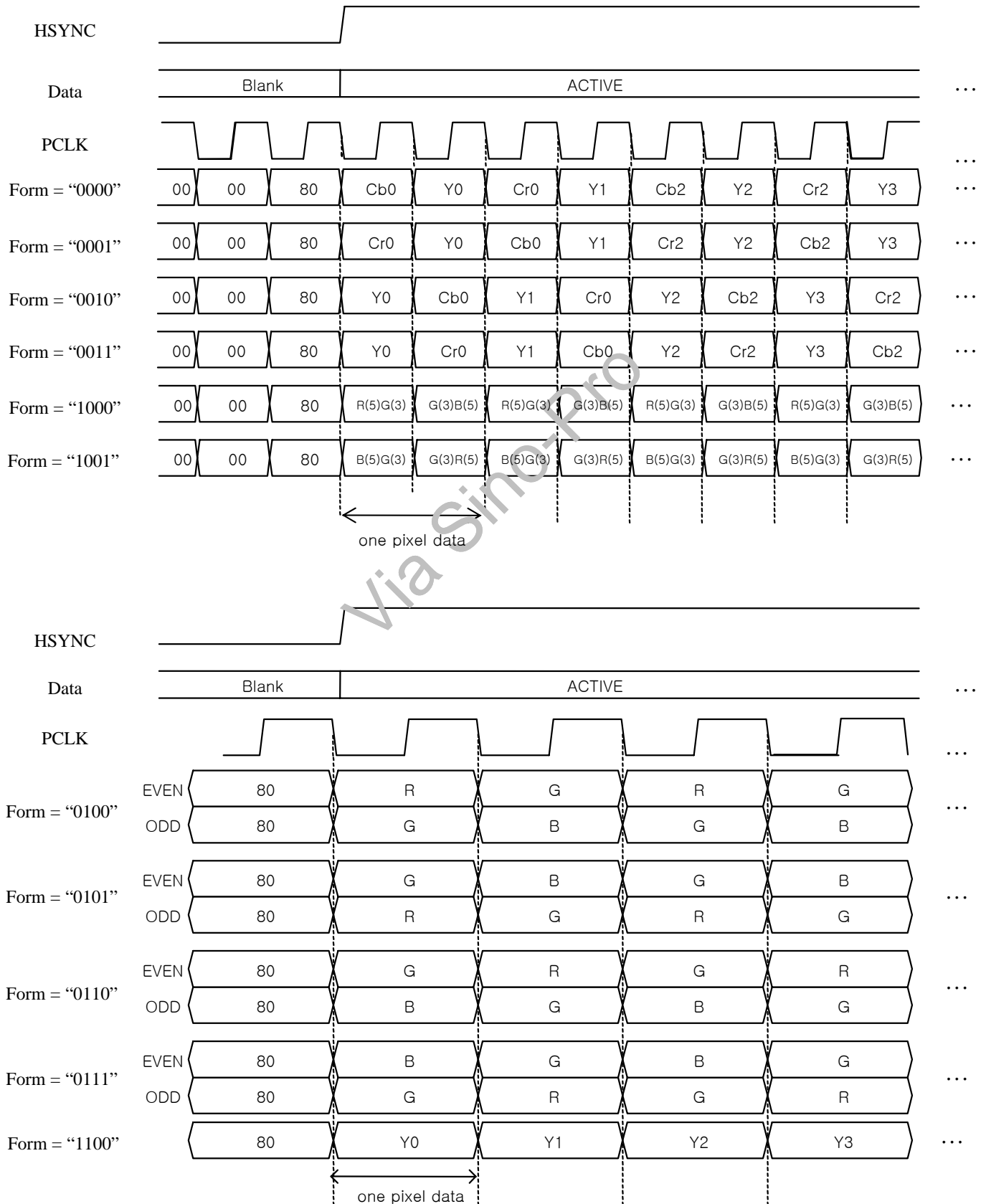
**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- OCF[6:4] : Out Clock Format

PCLK		Description
Normal type	Complementary type	
000 (default)	001	Normal Clock
010	011	Valid in Hsync high.
100	101	Valid in Active Window.
110	111	Valid in Active Window and Hsync high.



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(79) Image Signal Processor control 3 : ISP Control 3

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
4Fh	SCE	RSV	Vpol	Hpol	HD	RSV	RSV	RSV	RW
	0	0	0	0	1	0	1	0	

Default : 4Fh = 0Ah

Description :

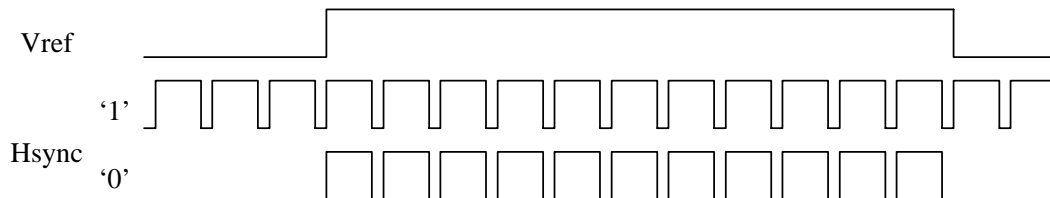
Bit name	value	Description
SCE	0	Sepia Color Disable. (<i>default</i>)
	1	Sepia Color Enable.
Vpol	0	VSYNC. (<i>default</i>)
	1	Invert VSYNC
Hpol	0	HSYNC. (<i>default</i>)
	1	Invert HSYNC
HD	0	Only Active region HSYNC
	1	All region HSYNC (<i>default</i>)

(1) Vpol : VSYNC polarity.

(2) Hpol : HSYNC polarity.



(3) HD



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(80) Image Signal Processor control 4 : ISP Control 4

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
50h	Hiz	SHiz	FY	FC	RSV	RGE	GGE	BGE	RW
	0	1	1	1	0	0	0	0	

Default : 50h = 70h

Description :

Bit name	value	Description
Hiz	0	Normal condition (<i>default</i>)
	1	Out PAD set to Hi-z condition.
SHiz	0	Don't care STDBY in Hi-z condition
	1	Out Pad set to Hi-z condition @ STDBY '1'
FY	0	Y Data range are 16 to 235
	1	Y Data range are 1 to 254 (<i>default</i>)
FC	0	CbCr Data range are 16 to 240
	1	CbCr Data range are 1 to 254 (<i>default</i>)
RGE	0	Red Gamma operation Enable. (<i>default</i>)
	1	Red Gamma operation Disable.
GGE	0	Green Gamma operation Enable. (<i>default</i>)
	1	Green Gamma operation Disable.
BGE	0	Blue Gamma operation Enable. (<i>default</i>)
	1	Blue Gamma operation Disable.

StdbbyHiz(SHiz)	Hiz	Stdbby	Out PAD condition
1	-	0	Normal
		1	Hi-Z
-	1	-	Hi-Z
		-	Hi-Z
0	1	-	Hi-Z
		0	Normal

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(89-91) Lens Shading Gain (RGB)

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
59h	X	X	X	X	0	0	0	0	RW
5Ah	X	X	X	X	0	0	0	0	
5Bh	X	X	X	X	0	0	0	0	

Default : 59h = 00h, 5Ah = 00h, 5Bh = 00h

Description :

Address	Name	Description
59h	<i>LensRgain</i>	Lens Gain for Red Pixel
5Ah	<i>LensGgain</i>	Lens Gain for Green Pixel
5Bh	<i>LensBgain</i>	Lens Gain for Blue Pixel

(92) Edge Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
5Ch	1	0	1	0	1	1	0	0	RW

Default : 5Ch = ACh

Description :

Edge enhancement gain & moire suppression gain factor.

	Description
[7:5]	<i>RSV</i>
EdgeControl[4:0]	Edge enhancement gain (0x08 = x1)

(93) Edge Threshold

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
5Dh	0	0	0	0	0	0	1	0	RW

Default : 5Dh = 02h

Description :

Edge Enhancement threshold.

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(118-129) Gamma Correction Coefficients

Address	Name	Value
76h	GC0	0 0 0 0 0 0 0 0 (00h)
77h	GC1	0 0 0 1 1 0 1 0 (1Ah)
78h	GC2	0 0 1 0 1 0 1 0 (2Ah)
79h	GC3	0 0 1 1 0 1 1 1 (37h)
7Ah	GC4	0 1 0 0 0 0 1 0 (42h)
7Bh	GC5	0 1 0 1 0 1 1 0 (56h)
7Ch	GC6	0 1 1 0 1 0 0 0 (68h)
7Dh	GC7	1 0 0 0 0 1 1 1 (87h)
7Eh	GC8	1 0 1 0 0 0 1 1 (A3h)
7Fh	GC9	1 0 1 1 1 1 0 0 (BCh)
80h	GC10	1 1 0 1 0 1 0 0 (D4h)
81h	GC11	1 1 1 0 1 0 1 0 (EAh)

Default : 00h, 1Ah, 2Ah, 37h, 42h, 56h, 68h, 87h, A3h, BCh, D4h, EAh

Description :

Related Register : Test Control6 (0xD8) bit6 | bit5 = Gamma Coefficient Selector

“00” : Address 0x76 ~ 0x81 is Red Data Gamma Coefficient

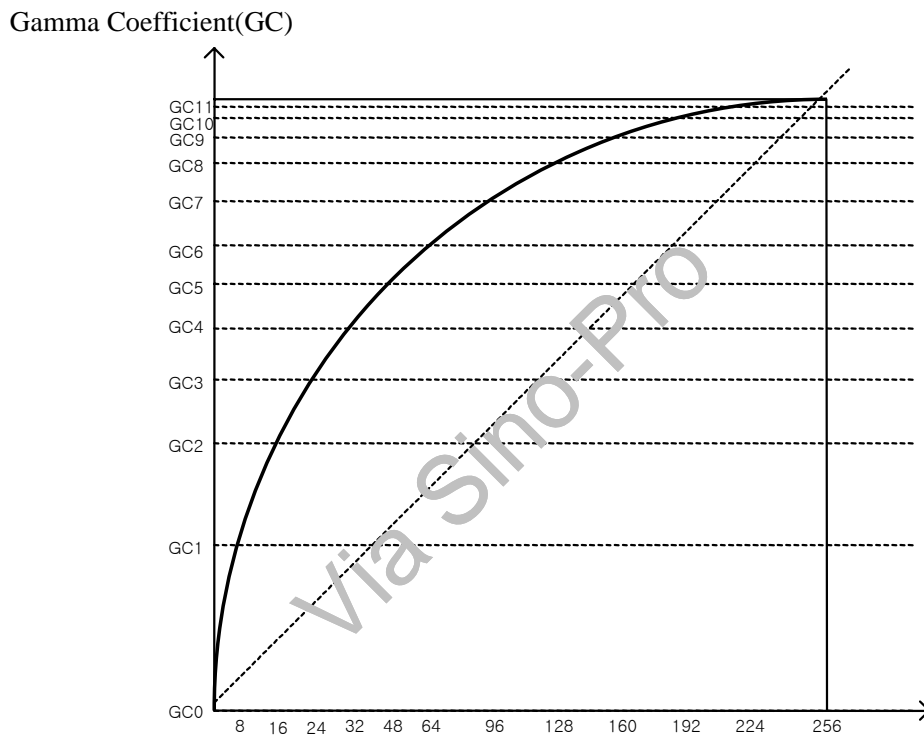
“01” : Green Data Gamma Coefficient

else : Blue Data Gamma Coefficient

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Description :

Gamma Correction is applied to RGB signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness.



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(142-150) Color Correction Coefficient

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
8Eh	0	0	1	1	1	0	0	0	RW
8Fh	1	0	1	0	0	1	0	1	
90h	0	0	0	0	1	1	0	1	
91h	1	0	0	1	0	0	1	1	
92h	0	0	1	0	1	1	0	1	
93h	0	0	0	0	0	1	1	0	
94h	1	0	0	0	0	0	1	1	
95h	1	0	1	0	1	0	1	0	
96h	0	1	0	0	1	1	0	1	

Default : 38h, A5h, 0Dh, 93h, 2Dh, 06h, 83h, AAh, 4Dh

Description :

Address	Name	Function
8Eh	<i>CT0</i>	Color Correction Matrix Coefficient, <i>m00</i>
8Fh	<i>CT1</i>	Color Correction Matrix Coefficient, <i>m01</i>
90h	<i>CT2</i>	Color Correction Matrix Coefficient, <i>m02</i>
91h	<i>CT3</i>	Color Correction Matrix Coefficient, <i>m10</i>
92h	<i>CT4</i>	Color Correction Matrix Coefficient, <i>m11</i>
93h	<i>CT5</i>	Color Correction Matrix Coefficient, <i>m12</i>
94h	<i>CT6</i>	Color Correction Matrix Coefficient, <i>m20</i>
95h	<i>CT7</i>	Color Correction Matrix Coefficient, <i>m21</i>
96h	<i>CT8</i>	Color Correction Matrix Coefficient, <i>m22</i>

- Color Coefficient : sign[7] | integer [6:5] | fractional [4:0]

$$\begin{matrix} \text{CC Coefficient} \\ \left(\begin{array}{ccc} 1.739627 & -1.14441 & 0.404786 \\ -0.60387 & 1.413677 & 0.190193 \\ -0.10247 & -1.30942 & 2.411888 \end{array} \right) \times 32 = \left(\begin{array}{ccc} 55.66805 & -36.6212 & 12.95316 \\ -19.3239 & 45.23768 & 6.08619 \\ -3.27892 & -41.9015 & 77.18042 \end{array} \right) = \left(\begin{array}{ccc} 38 & A5 & 0D \\ 93 & 2D & 06 \\ 83 & AA & 4D \end{array} \right)
 \end{matrix}$$

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(151-152) Color Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
97h	0	0	1	0	0	1	0	1	RW
98h	0	0	1	0	0	1	0	1	

Default : 97h = 25h, 98h = 25h

Description :

Color Gain = Sign[7] | Integer[6:5] | fractional[4:0]

Address	Name	Value
97h	CG11C	00100101 (25h)
98h	CG22C	00100101 (25h)

$$Cb' = Cb * CG11C$$

$$Cr' = Cr * CG22C$$

(155-156) Brightness & Contrast

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
9Bh	0	0	0	0	0	0	0	0	RW
9Ch	1	0	0	1	0	1	1	0	

Default : 9Bh = 00h, 9Ch = 96h

Description :

$$Y' = Y \times (Y_cont/128) + Y_bright$$

* Brightness(9Bh) : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

Contrast : 0x80 = x1

Address	Name	Value
9Bh	Brightness	00000000 (00h)
9Ch	Contrast	10010110 (96h)

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

(159-160) Cb Tone / Cr Tone

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
9Fh	1	0	0	0	0	0	0	0	RW
A0h	1	0	0	0	0	0	0	0	

Default : 9Fh = 80h, A0h = 80h

Description :

Cb/Cr Color Tone @ sepia color condition.(reg 4Fh[7])

Address	Name	Value
9Fh	Cb Tone	1 0 0 0 0 0 0 0 (80h)
A0h	Cr Tone	1 0 0 0 0 0 0 0 (80h)

(161-164) CCIR656 Sync Index Value

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
A1h	1	0	1	1	0	1	1	0	RW
A2h	1	0	0	1	1	1	0	1	
A3h	1	0	1	0	1	0	1	0	
A4h	1	0	0	0	0	0	0	0	

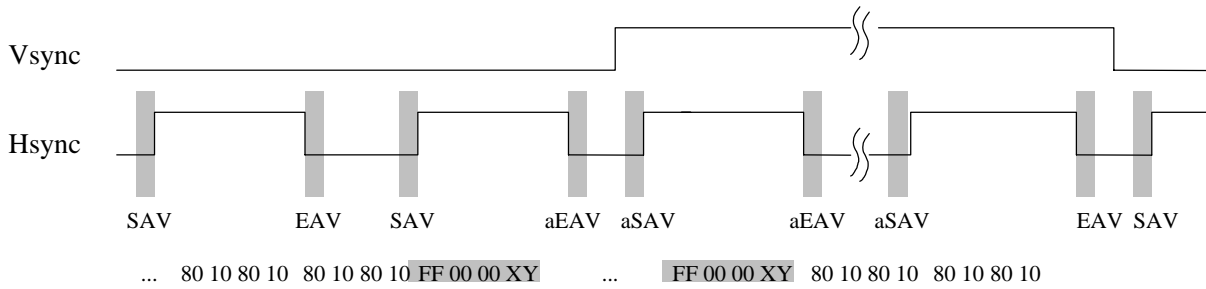
Default : B6h, 9Dh, ABh, 80h

Description :

EAV and SAV signals are inserted for synchronization purposes.

Address	Name	Description
A1h	<i>BlankEAV</i>	Blank Range End of Video
A2h	<i>ActiveEAV</i>	Active Range End of Video
A3h	<i>BlankSAV</i>	Blank Range Start of Video
A4h	<i>ActiveSAV</i>	Active Range Start of Video

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**



EAV : blank EAV,
aEAV : Active EAV,

SAV : blank SAV
aSAV : Active SAV

(165-170) Pad Vsync Start / Stop

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
A5h	0	0	0	0	0	0	0	0	RW
A6h	0	0	0	0	0	1	1	1	
A7h	0	0	0	0	0	0	0	1	
A8h	1	1	1	0	0	1	1	1	
A9h	0	0	0	0	0	0	0	0	
AAh	0	0	0	0	0	0	0	1	

Default : A5h = 00h, A6h = 07h, A7h = 01h, A8h = E7h, A9h = 00h, AAh = 01h

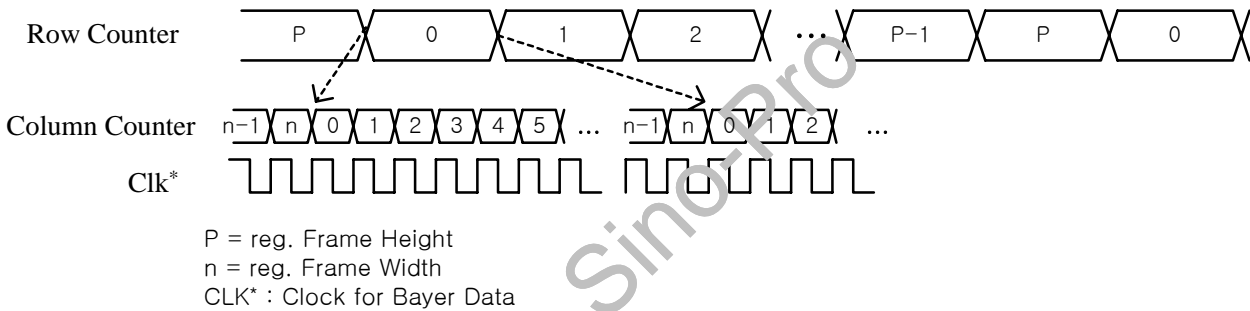
Description : VSYNC positions.

There are two counters to indicate the present coordinate of frame scanning :

Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *Frame Height* , and 0 to *Frame Width* respectively.

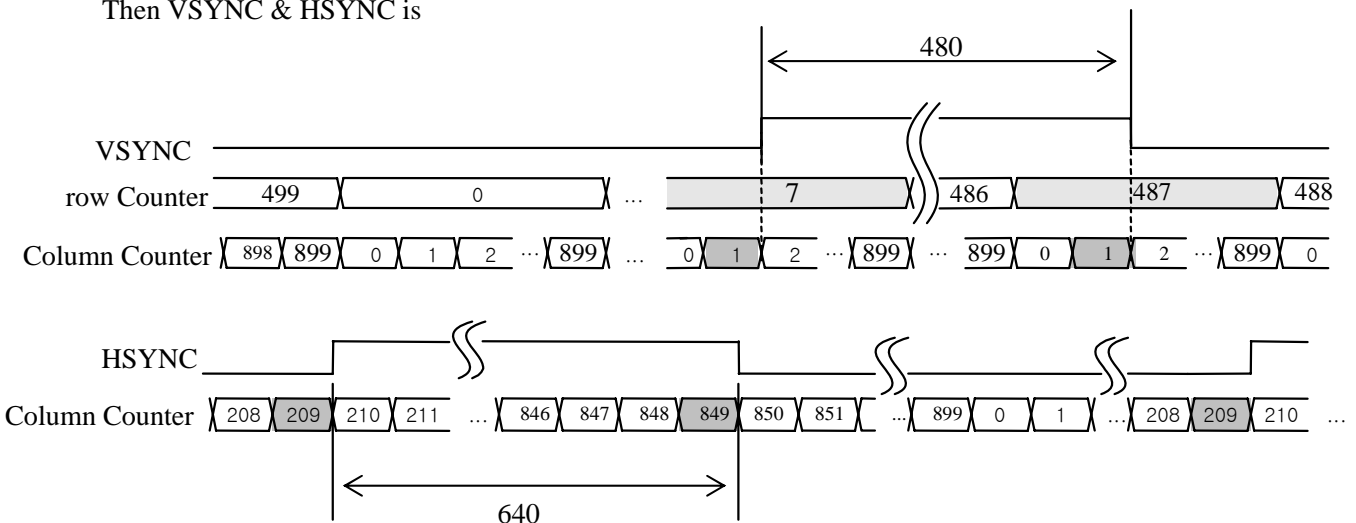
**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Address	Name	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	
A5h	VsyncStart (H)	0	0	0	0	0	0	0	0	(00h)
A6h	VsyncStart (L)	0	0	0	0	0	1	1	1	(07h)
A7h	VsyncStop (H)	0	0	0	0	0	0	0	1	(01h)
A8h	VsyncStop (L)	1	1	1	0	0	1	1	1	(E7h)
A9h	VsyncColumn (H)	0	0	0	0	0	0	0	0	(00h)
AAh	VsyncColumn (L)	0	0	0	0	0	0	0	1	(01h)



VSYNC rising : when (Row_counter = Reg. VsyncStart) & (Column_counter = Reg. VsyncColumn)
falling : when (Row_counter = Reg. VsyncStop) & (Column_counter = Reg. VsyncColumn)

(For example) VsyncStart = 7d, VsyncStop = 487d, VsyncColumn = 1d.
Frame Width(reg.04h, 05h) = 899d, Frame Height(reg.06h, 07h) = 499d,
Window X1(reg. 08h, 09h) = 209d, Window X2(reg.0Ch, 0Dh) = 849d.
Then VSYNC & HSYNC is



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(173) WW Control

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
ADh	CW3	CW2	CW1	CW0	RSV	RSV	RSV	RSV	RW
	1	0	0	1	1	1	1	1	

Default : ADh = 9Fh

Description :

Bit name	value	Description
CW[3:0]	1001	Center weight (Back Light compensation)

(174) AWB / AE Tolerance

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
AEh	0	0	1	0	0	0	1	0	RW

Default : AEh = 22h

Description :

[7:4] Set margin of AWB functions

[3:0] Set margin of AE functions

(175) AE speed

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
AFh	1	0	0	0	1	1	0	0	RW

Default : AFh = 8Ch

Description :

AE speed[3:0] : "Ae Speed Gain factor B" AE speed applied when exposure time is decreasing.

AE speed[7:4] : "Ae Speed Gain factor D" AE speed applied when exposure time is increasing.

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(176-178) Exposure

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
B0h	0	0	0	0	0	0	0	0	RW
B1h	1	0	0	0	0	0	0	0	
B2h	0	0	0	0	0	0	0	0	

Default : B0h = 00h, B1h = 80h, B2h = 00h

Exposure[23:0] : “*Exposure*” register means abstract exposure level of sensor. Larger the value of *Exposure*, effectively longer exposure time. LSB of *Exposure* corresponds to 1/64 line exposure time. User can write *Exposure* register only when AE function is disabled.

(179) Reference Exposure

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
B3h	0	1	1	1	0	0	0	0	RW

Default : B3h = 70h

Description :

Address	Name	Function
B0h	<i>TargetExp</i>	Target exposure level in auto-exposure mode

TargetExp determines target average brightness (Y target) for AE function. AE function controls Exposure register until captured image has brightness of target average brightness. The relationship between *TargetExp* and target average brightness is

$$\text{target average brightness} = \text{TargetExp}$$

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

(185-186) Maximum Frame Height

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
B9h	0	0	0	0	0	0	1	1	RW
BAh	1	1	1	0	0	1	1	0	

Default : B9h = 03h, BAh = E6h

Description :

Address	Name	Function
B9h	<i>MaxFrmHeight (H)</i>	Maximum Frame Height
BAh	<i>MaxFrmHeight (L)</i>	

During auto exposure mode, minimum frame rate is set by *MaxExpTime* register. If user set the *MaxExpTime* register larger value than *FrmHeight* register value so that *ExpTime* register have larger value than default(0413h), frame rate is automatically varied.

(187-188) Maximum Exposure

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
BBh	0	0	0	0	0	1	1	1	RW
BCh	1	1	0	0	1	1	0	0	

Default : BBh = 07h, BCh = CCh

Description :

Address	Name	Function
BBh	<i>MaxExp (H)</i>	Maximum Exposure
BCh	<i>MaxExp (M)</i>	

During auto exposure mode, maximum global gain is set by *MaxExp* register. If user set the *MaxExp* register larger value than *MaxFrmHeight* register value, global gain is automatically varied.

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

(189-190) Minimum Exposure Time

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
BDh	0	0	0	0	0	0	0	0	RW
BEh	0	0	0	0	1	1	0	0	

Default : BDh = 00h, BEh = 0Ch

Description :

Address	Name	Function
BDh	<i>MinExpTime (H)</i>	Minimum Exposure Time
BEh	<i>MinExpTime (L)</i>	

Under auto exposure mode, minimum exposure time of a pixel is set by *MinExpTime* register. LSB of *MinExpTime* corresponds to time for reading 1/64 line in each frame.

(193-196) Minimum / Maximum AWB Gain

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
C1h	0	0	0	1	0	0	0	0	RW
C2h	1	1	1	0	0	0	0	0	
C3h	0	0	0	1	0	0	0	0	
C4h	1	1	1	0	0	0	0	0	

Default : C1h = 10h, C2h = E0h, C3h = 10h, C4h = E0h

Description :

During auto white balance, *RedGain* and *BlueGain* register value varies between *MinAWB* and *MaxAWB*

Address	Name	Function
C1h	<i>Red Min Gain AWB</i>	0 0 0 1 0 0 0 0
C2h	<i>Red Max Gain AWB</i>	1 1 1 0 0 0 0 0
C3h	<i>Blue Min Gain AWB</i>	0 0 0 1 0 0 0 0
C4h	<i>Blue Max Gain AWB</i>	1 1 1 0 0 0 0 0

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(197-198) AWB RG / BG ratio

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
C5h	1	0	0	0	0	0	0	0	RW
C6h	1	0	0	0	0	0	0	0	

Default : C5h = 80h, C6h = 80h

Description :

Address	Name	Function
C5h	<i>AWB RG ratio</i>	AWB Color Ratio
C6h	<i>AWB BG ratio</i>	

Red Gm = Gm x AWB RGratio

Blue Gm = Gm x AWB BGratio

(AWB RG / BG ratio x1 = 80h)

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(199-206) Weighting Window

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
C7h	0	0	0	0	0	0	0	1	RW
C8h	1	0	1	0	0	1	0	1	
C9h	0	0	0	0	0	0	1	0	
CAh	0	1	1	1	1	0	1	0	
CBh	0	0	0	0	0	0	0	0	
CCh	1	0	1	0	0	1	1	1	
CDh	0	0	0	0	0	0	0	1	
CEh	0	1	0	0	0	1	1	1	

Default : 01h, A5h, 02h, 7Ah, 00h, A7h, 01h, 47h

Description : Refer to the description of WW bit of Auto Control [ADh].

$WeightX1 = 0x01A5h$, $WeightX2 = 0x027Ah$, $WeightY1 = 0x00A7h$, $WeightY2 = 0x0147h$

$WeightX1 > 421d$, $WeightX2 < 634d$

$WeightY1 > 167d$, $WeightY2 < 327d$

Address	Name	Function
C7h	<i>WeightX1 (H)</i>	X1 coordination of weight window of auto-exposure process
C8h	<i>WeightX1 (L)</i>	
C9h	<i>WeightX2 (H)</i>	X2 coordination of weight window of auto-exposure process
CAh	<i>WeightX2 (L)</i>	
CBh	<i>WeightY1 (H)</i>	Y1 coordination of weight window of auto-exposure process
CCh	<i>WeightY1 (L)</i>	
CDh	<i>WeightY2 (H)</i>	Y2 coordination of weight window of auto-exposure process
CEh	<i>WeightY2 (L)</i>	

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(212) Auto Control

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
D4h	X	X	AWBen	AEen	RSV	RSV	RSV	RSV	RW
	X	X	1	1	1	1	0	0	

Default : D4h = 3Ch

Description :

Mnemonic	Description
AWBen	AWB enable
AEen	AE enable

(216) Gamma Control

Address	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	R/W
D8h	RSV	GMS1	GMS0	X	RSV	RSV	RSV	RSV	RW
	1	0	0	X	0	0	0	0	

Default : D8h = 80h

Description :

Bit name	value	Description
GMS[6:5]		Gamma Coefficient(GC) select (0x76 ~ 0x81)
	00	Red Data GC
	01	Green Data GC
	Else	Blue Data GC

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Electrical Characteristics

Absolute Maximum Ratings *

HVDD Supply Voltage ----- -0.3V to 4.5V
 AVDD, DVDD Supply Voltage ----- -0.3V to 2.5V
 DC Voltage at any input pin ----- -0.3V to HVDD+0.3V
 DC Voltage at any output pin ----- -0.3V to HVDD+0.3V
 Storage Temperature ----- -40°C to +125°C

Table 4. DC Characteristics

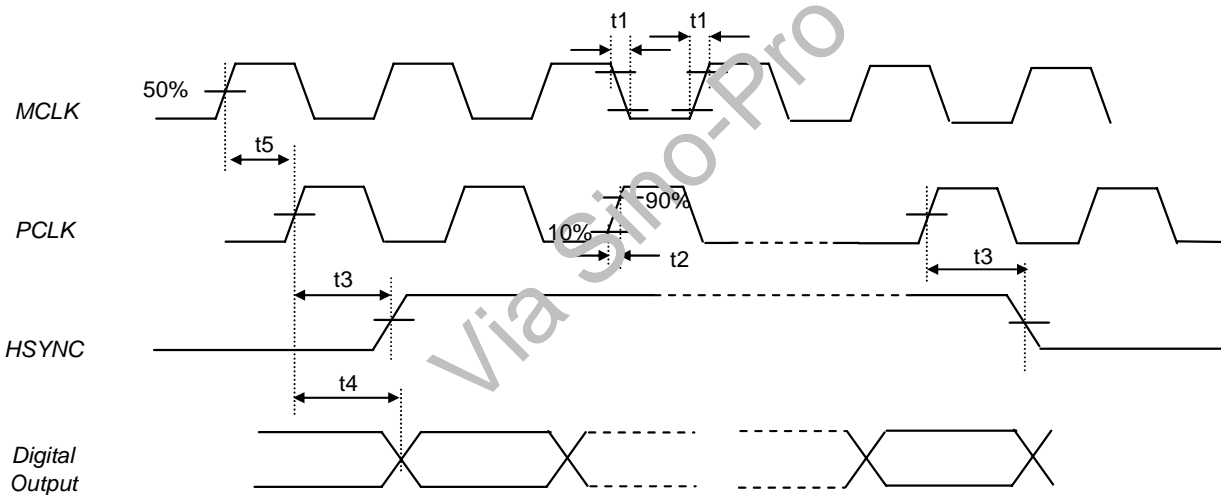
Symbol	Descriptions	Min	Typ	Max	Unit
V _{DD}	Digital, Analog, Pixel VDD voltage relative to GND(DGND, AGND, PGND) level.	1.62	1.8	1.98	V
HV _{DD}	High VDD(HVDD) voltage relative to GND(DGND) level.	1.62	1.8 2.5 3.3	3.6	V
I _{DDD}	Supply current at 30 fps. Currents are programmable through I2C serial interface. @2.5V I/O		23	30	mA
I _{DDS}	Standby supply current		10	15	uA
V _{IL1}	Input voltage LOW level			0.2*HVDD	V
V _{IH1}	Input voltage HIGH level	0.8*HVDD			V
V _{IL2}	Input voltage LOW level for SCL, SDA.			0.2*HVDD	V
V _{IH2}	Input voltage HIGH level for SCL, SDA.	0.8*HVDD			V
C _{IN}	Input pin capacitance			10	pF
V _{OL1}	Output Voltage LOW			0.1*HVDD	V
V _{OH1}	Output Voltage HIGH	0.9*HVDD			V
V _{OL2}	Output Voltage LOW level for SCL, SDA.			0.2	V
V _{OH2}	Output Voltage HIGH level for SDA.	HVDD-0.2			V
I _{IN}	Input leakage current		0.005	1	uA
I _{ot}	Output leakage current		0.005	1	uA

* CAUTION !! : Excessive stresses may cause permanent damage to the device.

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Table 5. AC Characteristics (Cout = 16pF, HVDD = 2.5V, MCLK = 27MHz, Output Format = YUV422)

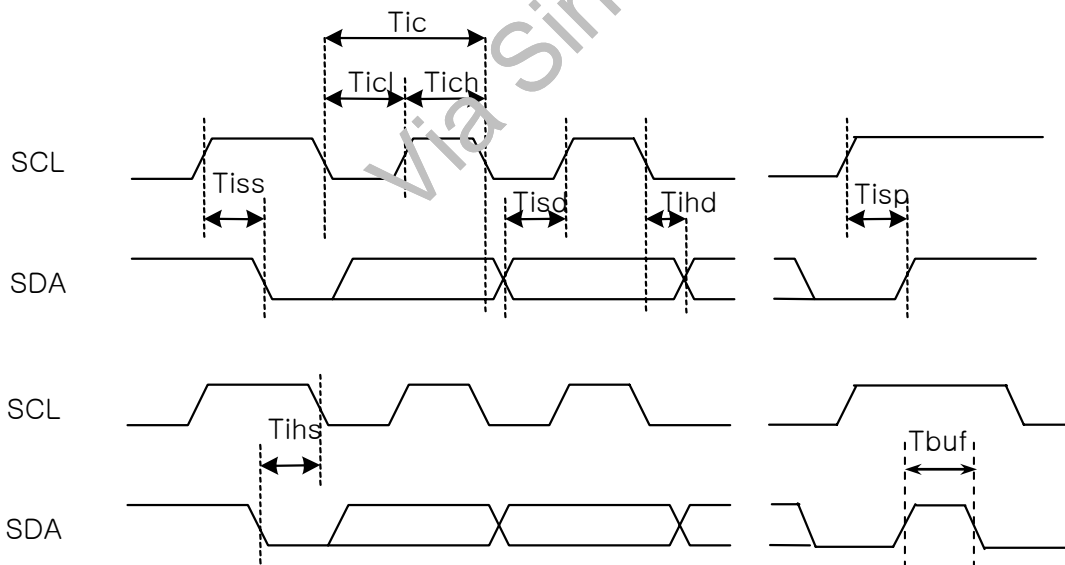
Symbol	Descriptions	Min	Typ	Max	Unit
f_{MCLK}	Master clock Frequency			27	MHz
duty	Master clock duty cycle		50		%
t1	Master clock rise/fall time		5		ns
t2	PCLK rise/fall time		5		ns
t3	PCLK rising edge to HSYNC		18		ns
t4	PCLK rising edge to digital output		19		ns
t5	MCLK rising edge to PCLK rising edge		15		ns


Fig. 14 Timing diagram of Clock, Data, and HSync

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Table 6. I2C bus signal timing

Symbol	Descriptions	Min	Max	Unit
Tic	I2C Clock frequency		400	kHz
Ticl	I2C Clock Low period	1.3		us
Tich	I2C Clock High period	600		ns
Tiss	setup time for start condition	600		ns
This	hold time for start condition	600		ns
Tisd	setup time for input data	300		ns
Tihd	hold time for input data	50		ns
Tisp	setup time of stop conditon	600		ns
Tbuf	Bus free time between a stop and start condition	1.3		us

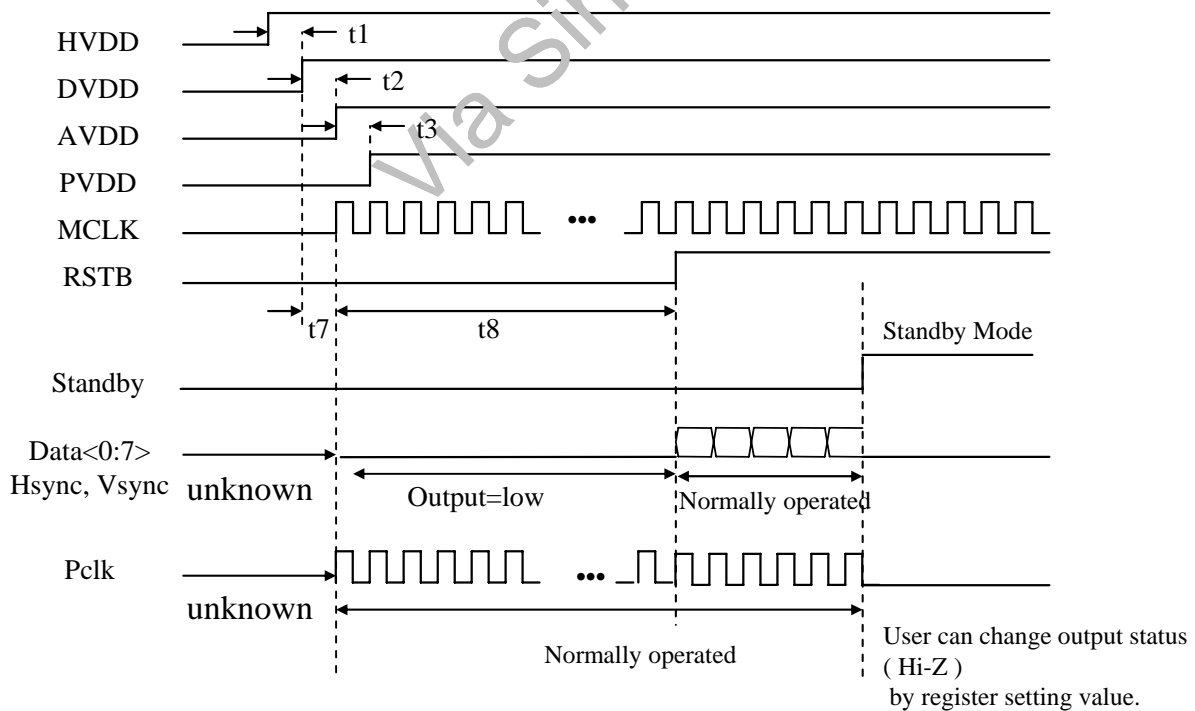
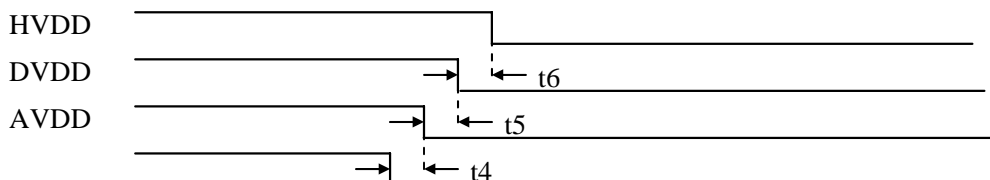


CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Table 7. Power ON,OFF Sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From HVDD rising to DVDD rising	0			ns
t2	From DVDD rising to AVDD rising	0			ns
t3	From AVDD rising to PVDD rising	0			ns
t4	From PVDD falling to AVDD falling	0			ns
t5	From AVDD falling to DVDD falling	0			ns
t6	From DVDD falling to HVDD falling	0			ns
t7	From DVDD rising to initial mclk rising	0			ns
t8	Minimum reset time	$8 \times (^*)T_{mclk}$			

(^{*}) $T_{mclk} = 1/f_{mclk}$, period time of mclk)

Power-On Sequence

Power-Off Sequence


**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Table 8. Electro- Optical Characteristics

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Sens	Sensitivity	1)		1.9		V/Lux.sec
Vsat	Saturation Level	2)		780		mV
Vdrk	Dark Signal	3)		9.24		mV/sec
PSNU	PIXEL Signal NON-Uniformity	4)		3.5		%
DR	Dynamic range	5)		62		dB

Notes :

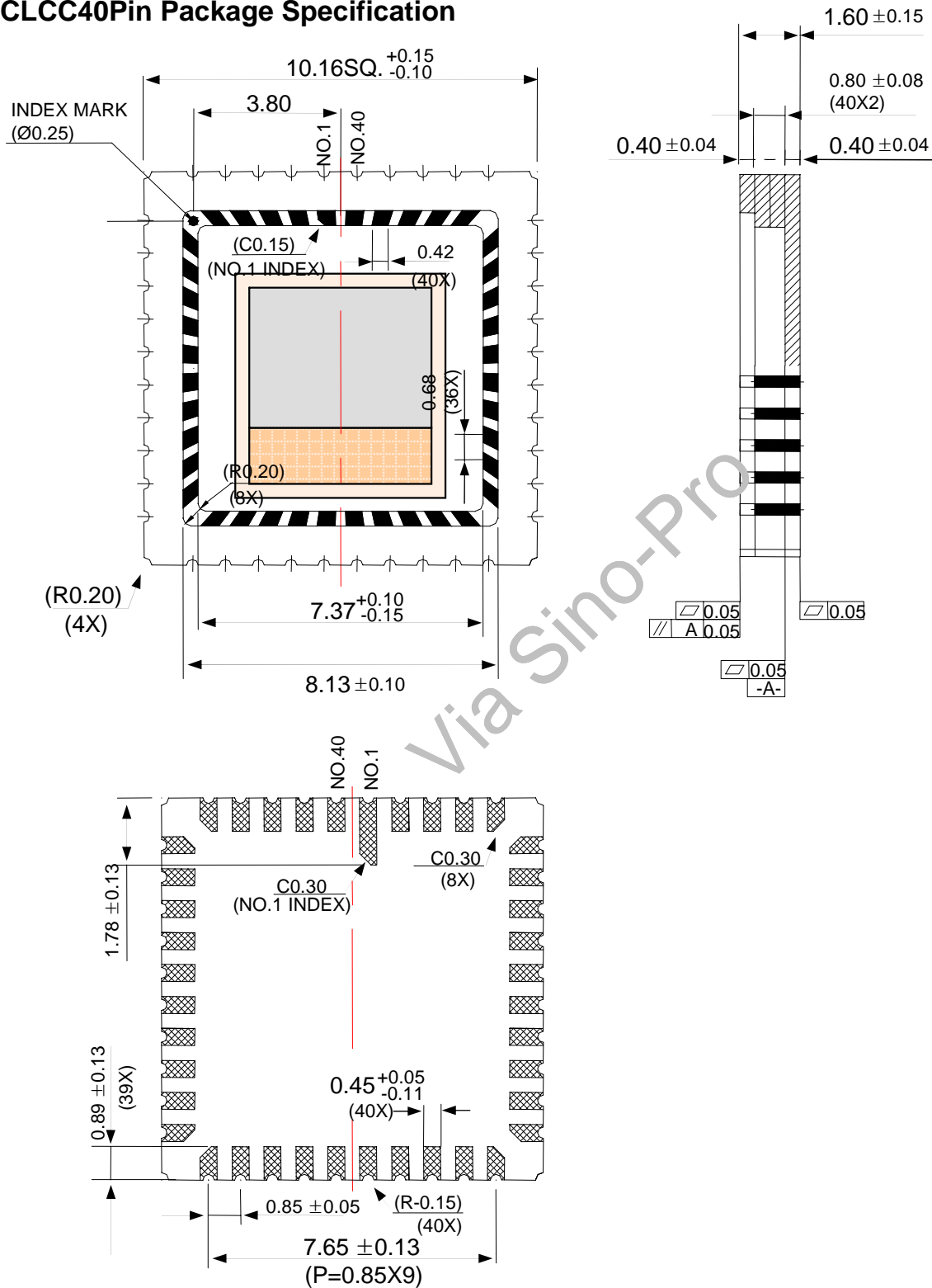
- 1) Measured sensitivity of Green pixel at 4lux illumination for 66ms integration time
- 2) For $\lambda=550$ wavelength
- 3) Measured at the zero illumination for 66ms at the 40 degree
- 4) For 16X16 pixel region under illumination with output signal equal to 50% of saturation signal.

$$\frac{\text{Max value of Block} - \text{Min value of Block}}{\text{Average value of all blocks}} \times 100$$

- 5) For frame rate = 15fps, 40 degree
20*Log [Saturation Signal /Dark signal] [dB]

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

CLCC40Pin Package Specification



NOTE:

1. NI 2.0um + Au 0.5um MIN
2. NO METALLIZATION ON SEAL RING AND DIE ATTACH PAD.
3. UNIT : mm

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Application Note

- Revision Number

Reg. Addr. (Hex)	Read Value (Hex)	Register Name	Descriptions
02	01	<i>RevNum</i>	Revision Number of PO3030K

- Recommended Register Values (Write I2C Addr. : 0xDC, Read I2C Addr. : 0xDD)

Overview

- The better image can be acquired to set up recommended register value.

(1) Initial Setting

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
12	06	<i>AmpBias</i>	02	
13	08	<i>PixelBias</i>	02	
1E	06	<i>TgControl2</i>	0A	
21	00	<i>Reserved</i>	52	
24	02	<i>Reserved</i>	00	
32	69	<i>Reserved</i>	68	
36	35	<i>Reserved</i>	3C	
39	60	<i>Reserved</i>	30	
4D	FE	<i>Reserved</i>	DD	
53	1C	<i>Reserved</i>	04	
5C	70	<i>EdgeGain</i>	AC	
5D	04	<i>EdgeThreshold</i>	02	
5F	08	<i>Reserved</i>	00	
60	08	<i>Reserved</i>	08	
61	08	<i>Reserved</i>	10	
62	08	<i>Reserved</i>	1F	
63	00	<i>Reserved</i>	00	
64	00	<i>Reserved</i>	08	

continue...

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
65	10	<i>Reserved</i>	1B	
66	14	<i>Reserved</i>	1F	
73	68	<i>Reserved</i>	70	
82	01	<i>Reserved</i>	00	
83	80	<i>Reserved</i>	40	
85	0C	<i>Reserved</i>	00	
86	B6	<i>Reserved</i>	88	
89	00	<i>Reserved</i>	88	
AD	3F	<i>WWControl</i>	9F	
AE	24	<i>AELock</i>	22	
B3	68	<i>RefExp</i>	70	
B4	03	<i>Reserved</i>	00	
B8	10	<i>Reserved</i>	00	
B9	07	<i>MaxFrmHeight(H)</i>	03	
BA	CC	<i>MaxFrmHeight(L)</i>	E6	
BB	1F	<i>MaxExp(H)</i>	07	
BC	30	<i>MaxExp(L)</i>	CC	
BF	02	<i>Reserved</i>	08	
8E	42	<i>ColorMatrix11</i>	38	Color Matrix
8F	95	<i>ColorMatrix12</i>	A5	
90	8D	<i>ColorMatrix13</i>	0D	
91	89	<i>ColorMatrix21</i>	93	
92	3A	<i>ColorMatrix22</i>	2D	
93	90	<i>ColorMatrix23</i>	06	
94	84	<i>ColorMatrix31</i>	83	
95	89	<i>ColorMatrix32</i>	AA	
96	2D	<i>ColorMatrix33</i>	4D	

continue...

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- Gamma Setting (**Keep The Following Sequence**)

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
D8	80	<i>GammaSelect</i>	80	Select R Gamma
76	00	<i>GmCoeff0</i>	00	R gamma
77	0D	<i>GmCoeff1</i>	1A	
78	18	<i>GmCoeff2</i>	2A	
79	22	<i>GmCoeff3</i>	37	
7A	2C	<i>GmCoeff4</i>	42	
7B	3E	<i>GmCoeff5</i>	56	
7C	4F	<i>GmCoeff6</i>	68	
7D	6F	<i>GmCoeff7</i>	87	
7E	8E	<i>GmCoeff8</i>	A3	
7F	AC	<i>GmCoeff9</i>	BC	
80	C8	<i>GmCoeff10</i>	D4	
81	E5	<i>GmCoeff11</i>	EA	
D8	A0	<i>GammaSelect</i>	80	Select G Gamma
76	00	<i>GmCoeff0</i>	00	G Gamma
77	0D	<i>GmCoeff1</i>	1A	
78	18	<i>GmCoeff2</i>	2A	
79	22	<i>GmCoeff3</i>	37	
7A	2C	<i>GmCoeff4</i>	42	
7B	3E	<i>GmCoeff5</i>	56	
7C	4F	<i>GmCoeff6</i>	68	
7D	6F	<i>GmCoeff7</i>	87	
7E	8E	<i>GmCoeff8</i>	A3	
7F	AC	<i>GmCoeff9</i>	BC	
80	C8	<i>GmCoeff10</i>	D4	
81	E5	<i>GmCoeff11</i>	EA	

continue...

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
D8	C0	<i>GammaSelect</i>	80	Select B Gamma
76	00	<i>GmCoeff0</i>	00	B Gamma
77	0D	<i>GmCoeff1</i>	1A	
78	18	<i>GmCoeff2</i>	2A	
79	22	<i>GmCoeff3</i>	37	
7A	2C	<i>GmCoeff4</i>	42	
7B	3E	<i>GmCoeff5</i>	56	
7C	4F	<i>GmCoeff6</i>	68	
7D	6F	<i>GmCoeff7</i>	87	
7E	8E	<i>GmCoeff8</i>	A3	
7F	AC	<i>GmCoeff9</i>	BC	
80	C8	<i>GmCoeff10</i>	D4	
81	E5	<i>GmCoeff11</i>	EA	

Above recommended setting includes the following functions

- **Max.Frame Rate : VGA 30 fps. @ MCLK = 27 MHz,**
- **Auto Frame Rate Control : Min.Frame Rate = Max.Frame Rate / 4**
- **Auto Gain Control : Max.Global Gain = 4X**
- **Output Format : YUV422 (1 ~ 254)**
- **Weight Window : 3X Center Weight**
- **VSYNC (positive level), HSYNC (positive level), PCLK (positive edge)**
- **Pixel Correction, Color Correction, Gamma Correction, AWB, AE**

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(2) Additional setting according to the resolution

PO3030K support the sub-sampling methods. Refer to Reg.20h description.

- VGA mode (640x480)

Address (Hex)	Recommended value (Hex)	Register Name	Default Value (Hex)	Descriptions
20	44	<i>TgContol4</i>	44	
5C	6C	<i>EdgeControl</i>	AC	

- QVGA mode (320x240)

20	14	<i>TgContol4</i>	44	
5C	66	<i>EdgeControl</i>	AC	

- QQVGA mode (160x120)

20	34	<i>TgContol4</i>	44	
5C	66	<i>EdgeControl</i>	AC	

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- Flicker Free Mode

-Related Registers : Period50H (Reg.49h) ~ Period60L(Reg.4C), FdControl (Reg.46h)

(1) Manual Flicker Free Mode (50Hz / 60Hz)

Reg. Addr. (Hex)	Appropriate value (Hex)	Register Name	Default Value (Hex)	Descriptions
49	Refer to following example	<i>Period50H</i>	12	
4A	„	<i>Period50L</i>	E4	
4B	„	<i>Period60H</i>	13	
4C	„	<i>Period60L</i>	14	

Reg. Addr. (Hex)	Flicker On	Register Name	Flicker Off	Descriptions
46	20 / 40	<i>FdControl</i>	00	60Hz / 50Hz Flicker Free Enable

-Flicker Period Control Register Setting

Related Registers : *Reg.49(h), Reg.4A(h)* – for 50Hz light source.

Reg.4B(h), Reg.4C(h) – for 60Hz light source.

Flicker Period Reg. Value = $256 * (MCLK \text{ Freq} / (\text{Frame Width} * 2)) / (\text{Flicker Freq} * 2)$

ex) If you using 24MHz MCLK,

- Flicker period for 60Hz (Reg.4Bh, 4Ch)

Frame Width = 900 column

*Flicker Period = $256 * (24000000 / (900 * 2)) / (60 * 2) = 28444 = 0x6F1C$*

Reg.4B(h) = 0x6F; Reg.4C(h) = 0x1C;

- Flicker period for 50Hz (Reg.49h, 4Ah)

Frame Width = 900 column

*Flicker Period = $256 * (24000000 / (900 * 2)) / (50 * 2) = 34133 = 0x8555$*

Reg.49(h) = 0x85; Reg.4A(h) = 0x55;

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(2) Auto Flicker Detection Mode

PO3030K support auto flicker detection mode.

Reg. Addr. (Hex)	Appropriate value	Register Name	Default Value (Hex)	Descriptions
48	(1.667ms * MCLK freq.) / 256	<i>Regclk</i>	2C	
49	Refer to the example in the previous page.	<i>Period50H</i>	00	
4A	„	<i>Period50L</i>	B0	
4B	„	<i>Period60H</i>	00	
4C	„	<i>Period60L</i>	94	

Reg. Addr. (Hex)	Flicker On (Hex)	Register Name	Flicker Off (Hex)	Descriptions
46	8F	<i>FdControl</i>	00	50Hz / 60Hz flicker Auto Detection

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- Output Format

Related Registers : ISPControl2 (Reg.4Eh), ISPControl4 (Reg.50), EdgeControl (Reg.5Ch), Brightness (Reg.9Bh), Y Contrast (Reg.9Ch), CG11C (Reg.97h), CG22C (Reg.98h)

1) YCbCr422 (8 Bit, Y range : 16 ~ 235, Cb & Cr range : 16 ~ 240) – CCIR.601

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4E	xxxx0000	<i>ISPControl2</i>	10	Cb Y Cr Y...
	xxxx0001			Cr Y Cb Y...
	xxxx0010			Y Cb Y Cr...
	xxxx0011			Y Cr Y Cb...

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
50	40	<i>Reserved</i>	70	
9B	10	<i>Brightness</i>	00	
9C	80	<i>Y Contrast</i>	96	

2) YUV422 (8 Bit, Y range : 1 ~ 254 , U & V range : 1 ~ 254)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4E	xxxx0000	<i>ISPControl2</i>	10	U Y V Y...
	xxxx0001			V Y U Y...
	xxxx0010			Y U Y V...
	xxxx0011			Y V Y U...

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
50	70	<i>Reserved</i>	70	
9B	00	<i>Brightness</i>	00	
9C	94	<i>Y Contrast</i>	96	

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

3) RGB565 (8 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4E	xxxx1000	<i>ISPControl2</i>	00	R5G3, G3B5...
	xxxx1001			B5G3, G3R5...

5) ISP BAYER (8 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4E	xxxx0100	<i>ISPControl2</i>	00	RGRG...GBGB...
	xxxx0101			GBGB...RGRG...
	xxxx0110			GRGR...BGBG...
	xxxx0111			BGBG...GRGR...

6) Raw RGB BAYER (8 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
4E	xxxx0100	<i>ISPControl2</i>	00	RGRG...GBGB...
	xxxx0101			GBGB...RGRG...
	xxxx0110			GRGR...BGBG...
	xxxx0111			BGBG...GRGR...
4D	E0	<i>Reserved</i>	DD	Color Correction Off
50	77	<i>ISPControl4</i>	70	Gamma Off
5C	00	<i>EdgeControl</i>	AC	Edge Enhancement Off

- 642 x 482

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
09	D0	<i>WindowX1_L</i>	D1	
0B	06	<i>WindowY1_L</i>	07	
0D	52	<i>WindowX2_L</i>	51	
0F	E8	<i>WindowY2_L</i>	E7	
A6	06	<i>VsyncStart_L</i>	07	
A8	E8	<i>VsyncStop_L</i>	E7	

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- 644 x 484

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
09	CF	<i>WindowX1_L</i>	D1	D1
0B	05	<i>WindowY1_L</i>	07	07
0D	53	<i>WindowX2_L</i>	51	51
0F	E9	<i>WindowY2_L</i>	E7	E7
A3	05	<i>VsyncStart_L</i>	07	07
A5	E9	<i>VsyncStop_L</i>	E7	E7

Via Sino-Pro

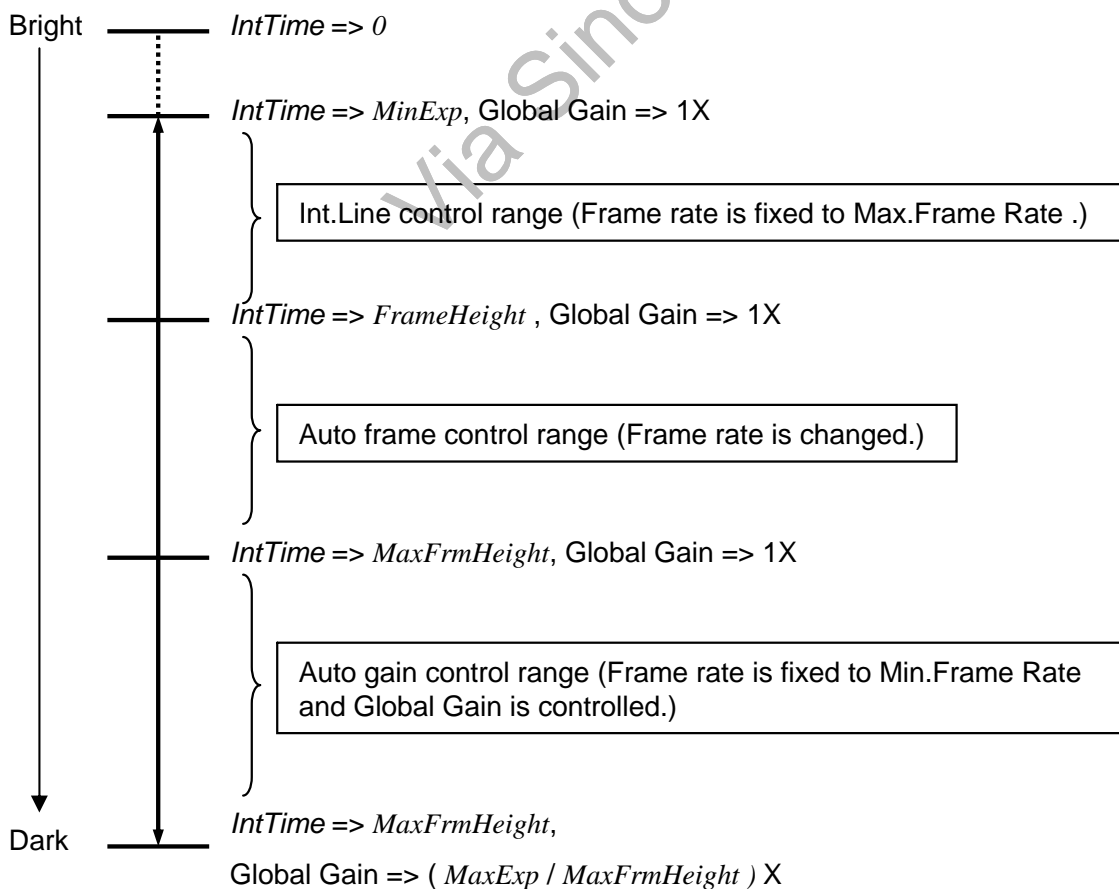
**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- AE Control

(1) Internal AE Control

Related Registers : Int.Time(Reg.1Ah ~ 1Ch), GlobalGain(Reg.15h), AutoControl(Reg.D4h), TargetExp (Reg.B3h), MaxFrmHeight (Reg.B9h, BAh), MaxExp (Reg.BB, BCh), MinExp (Reg.BDh, BEh), AutoLock (Reg.AEh)

If AE of *AutoControl(Reg.DDh)* register is set to '1', *IntTime(Reg.1A h ~ 1Ch)*, *GlbGain(Reg.15h)* registers are automatically controlled by ISP to control overall brightness of sensor image. The target brightness level of image is set by *TargetExp(Reg.B3h)* register. During auto exposure process, the average brightness of image is controlled to get close to *TargetExp* register value with the margin set by *AutoLock[3:0](Reg.AEh)* register. *IntTime* registers are controlled, at first. If Integration Line is limited to the *MaxFrmHeight(Reg.B9h, BAh)*, then Global Gain is controlled. Variation of *GlbGain* or *IntTime* register are limited by *MaxExp*, *MinExp*, *MaxFrameHeight* registers.



CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

1) Auto Frame Control

Auto Frame Control Method can be used to get brighter image in dark condition. Frame rate is automatically controlled by ISP between Max.Frame Rate and Min.Frame Rate.

$$\begin{aligned} \text{Max. Frame Rate} &= (\text{MCLK frequency}) / (\text{Frame Height} * \text{Frame Width} * 2) \\ \text{Min. Frame Rate} &= (\text{MCLK frequency}) / (\text{MaxFrmHeight} * \text{Frame Width} * 2) \end{aligned}$$

$$\begin{aligned} (\text{Frame Height} &= \text{FrameHeight (Reg. 06h, 07h)} + 1 \\ \text{Frame Width} &= \text{FrameWidth (Reg. 04h, 05h)} + 1) \end{aligned}$$

Min. Frame Rate is controlled by *MaxFrmHeight* register (Reg.B6h, B7h).

MaxFrmHeight must be bigger than *FrameHeight*..(*MaxFrmHeight* >= *FrameHeight*)

2) Auto Gain Control

Auto Gain Control Method can be used to get brighter image in dark condition. Global gain is controlled automatically by ISP between Max.Global Gain and Min.Global Gain.

$$\begin{aligned} \text{Max. Global Gain} &= (\text{MaxExp} / \text{MaxFrmHeight}) * X \\ \text{Min. Global Gain} &= \text{MinGlbGain} \end{aligned}$$

MaxExp must be bigger than *MaxFrmHeight*. (*MaxExp* >= *MaxFrmHeight*)

(2) External AE Control

Related Registers : *AutoControl*(Reg.D4h), *Exposure* (Reg.B0h, B1h, B2h),

If you turn off internal AE function of PO3030K, you can control Integration line and Global gain through *Exposure* (Reg.B0h ~ B2h) registers for implementing external Auto Exposure function. *IntTime* (Reg.1Ah ~ 1Ch) and *GlobalGain* (Reg.15h) registers aren't accessible by user. *Exposure* (Reg.B0h ~ B2h) registers aren't controllable while internal AE is working.

- Disable Internal AE Function

Reg. Addr. (Hex)	Register Name	Descriptions
D4	<i>AutoControl</i>	Set Bit 4 (AE) to '0' to turn off internal AE function.
AF	<i>AEspeed</i>	Set this register to 00h

- Registers for External AE Control

Reg. Addr. (Hex)	Register Name	Descriptions
B0	<i>Exposure(H)</i>	
B1	<i>Exposure(M)</i>	
B2	<i>Exposure(L)</i>	

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

(1) $MinExp < Exposure \leq FrameHeight$ (Int.Line Control Range)

(2) $FrameHeight < Exposure \leq MaxFrmHeight$ (Frame Rate Control Range)

Current Frame Rate = (MCLK frequency) / (Exposure * Frame Width * 2)
Min. Frame Rate is limited by *MaxFrmHeight*.

(3) $MaxFrmHeight < Exposure \leq MaxExp$ (Global Gain Control Range)

Current Global Gain = (Exposure / *MaxFrmHeight*) * *RefGain* + *MinGlbGain*
Exposure is limited by *MaxExp*.

Via Sino-Pro

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

- AWB Control

(1) Internal AWB Control

Related Registers : *RGain(Reg.16h)*, *G1Gain(Reg.17h)*, *BGain(Reg.18h)*, *G2Gain(Reg.19h)*, *AWBRratio(Reg.C5h)*, *AWBBratio(Reg.C6h)*,

If AWB of *AutoControl(Reg.D4h)* register is set to '1', *RGain(Reg.16h)* and *BGain(Reg.18h)* registers are automatically controlled by ISP to control the RGB ratio of sensor image. The ratio of average of R, G, B components can be controlled by *AWBRratio* and *AWBBratio* registers. Those ratios are defined according to the following relation,

$$\overline{B} = \frac{AWBBratio}{128} \times \overline{G} \qquad \overline{R} = \frac{AWBRratio}{128} \times \overline{G}$$

(2) External AWB Control

If you turn off internal AWB function of PO3030K, you can control R, G and B gains through *R*, *G1*, *B* and *G2 Gain (Reg.16h ~ 19h)* registers for implementing external Auto White Balance function. *R* and *B gain* registers aren't controllable while internal AWB is working.

- Disable Internal AWB Function

Reg. Addr.	Register Name	Descriptions
(Hex) D4	<i>AutoControl</i>	Set Bit 5 (AWB) to '0' to turn off internal AWB function.

- Registers for external AWB control

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Descriptions
16	<i>R Gain</i>	40	1X R Gain = 0x40 (2X = 0x80)
17	<i>G1 Gain</i>	40	1X G1 Gain = 0x40
18	<i>B Gain</i>	40	1X B Gain = 0x40
19	<i>G2Gain</i>	40	1X G2 Gain = 0x40

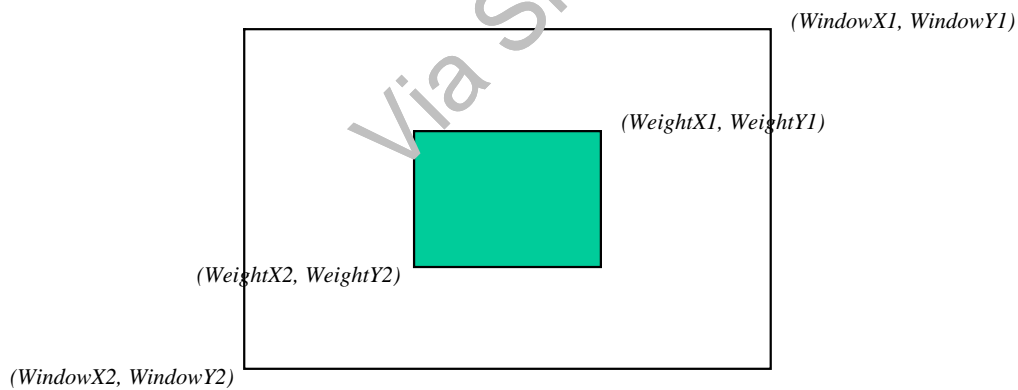
CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

- Backlight Compensation

*Related Registers : WeightX1 (Reg.C7h, C8h), WeightX2 (Reg.C9h, CAh), WeightY1 (Reg.CBh, CCh),
WeightY2 (Reg.CDh, CEh), WeightControl (Reg.ADh),*

1) Weight Window

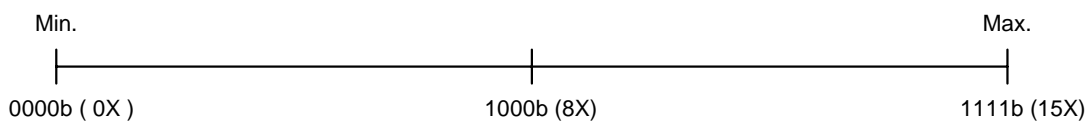
Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Description
C7	WeightX1(H)	03	Minimum : WindowX1(Reg.08h, 09h)
C8	WeightX1(L)	14	
C9	WeightX2(H)	05	Maximum : WindowX2(Reg.0Ch, 0Dh)
CA	WeightX2(L)	28	
CB	WeightY1(H)	01	Minimum : WindowY1(Reg.0Ah, 0Bh)
CC	WeightY1(L)	9A	
CD	WeightY2(H)	03	Maximum: WindowY2(Reg.0Eh, 0Fh)
CE	WeightY2(L)	33	



2) Weight Factor

Weight Factor is controlled by $CW[3..0]$ (bit7 ~ 4) of *WeightControl* register (Reg.ADh).

$$0000b \leq \text{Weight Factor } (CW[3..0]) \leq 1111b$$



CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

- Brightness / Y Contrast / Saturation (Only for YCbCr422 & YUV422)

-Related Registers : *Brightness (Reg.9Bh)*, *YContrast (Reg.9Ch)*, *CG11C (CbGain, Reg.97h)*, *CG22C (CrGain, Reg.98h)*

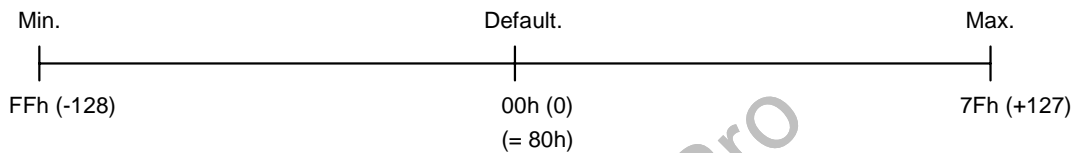
$$Y \text{ result} = Y * (Ycontrast / 128) + Ybrightness$$

$$Cb \text{ result} = Cb * CbGain / 32$$

$$Cr \text{ result} = Cr * CrGain / 32$$

(1) Brightness

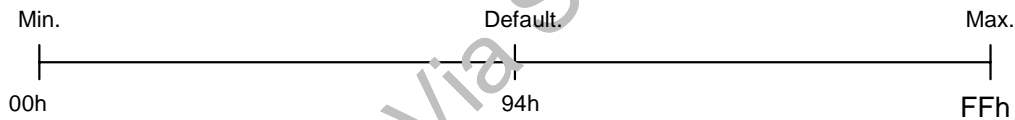
Brightness is controlled by *Brightness* register (*Reg.9Bh*). The default value of this register is 00h.



* Brightness(9Bh) : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

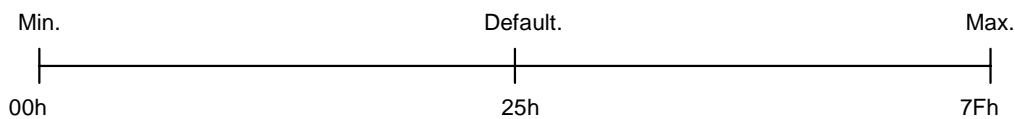
(2) Y Contrast

Contrast is controlled by *Y Contrast* register (*Reg.9Ch*). The default value of this register is 96h.



(3) Saturation

Saturation is controlled by *CG11C (CbGain)* and *CG22C (CrGain)* registers (*Reg.97h, 98h*) with the same values. The default value of these registers are 25h and these are controllable separately for adjusting color tone.



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- Color Correction Matrix

Related Registers : ColorMatrix11 (Reg.8Eh) ~ ColorMatrix33 (Reg.96h)

Color correction can be accomplished by color transform registers (Reg.8Eh ~ 96h) by means of the following equation, where **CC** is 3x3 color correction matrix.

$$\begin{pmatrix} CT0 & CT1 & CT2 \\ CT3 & CT4 & CT5 \\ CT6 & CT7 & CT8 \end{pmatrix} = \begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * CC$$

* m00 ~ m22 : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

<Ex.>

$$\begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * \begin{pmatrix} 1.7396 & -1.1444 & 0.4048 \\ -0.6039 & 1.4137 & 0.1902 \\ -0.1025 & -1.3094 & 2.4119 \end{pmatrix}$$

$$= \begin{pmatrix} 55.6672 & -36.6208 & 12.9536 \\ -19.3248 & 45.2384 & 6.0864 \\ -3.28 & -41.9008 & 77.1808 \end{pmatrix} = \begin{pmatrix} 38h & A5h & 0Dh \\ 93h & 2Dh & 06h \\ 83h & AAh & 4Dh \end{pmatrix}$$

- Y target Control

Related Registers : TargetExp (Reg.B3h, Reg.73h)

Y target is controlled by *TargetExp* register (Reg.B3h, Reg.73h).

<Ex.>

LEVEL	1	2	3	4	5	6	7	8	9
Reg.B3h	30	40	50	60	70	80	90	A0	B0
Reg.73h									

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

- Sharpness Control

Related Registers : EdgeControl (Reg.5Ch), EdgeThreshold (Reg.5Dh)

Sharpness is controlled by *EdgeControl* (Reg.5Ch) and *EdgeThreshold* register (Reg.5Dh). All three values have the following Min. and Max. value.

$$00000b \leq EdgeGain (EdgeControl[4..0]) \leq 11111b$$

$$00h \leq EdgeThreshold \leq FFh$$

The lowest sharpness level can be gotten by setting registers as follows.

$$EdgeGain = 00000b, EdgeThreshold = FFh$$

And, the highest sharpness level can be gotten by setting registers as follows.

$$EdgeGain = 11111b, EdgeThreshold = 00h$$

But, we recommend to set *EdgeThreshold* register value greater than 01h.

Ex.)

Sharpness Level	Reg. Addr. (Hex)	Recommended value	Register Name	Default Value
0	5C	xxx00000 (b)	<i>EdgeControl</i>	xxx01100 (b)
	5D	04 (h)	<i>EdgeThreshold</i>	02 (h)
1	5C	xxx00100 (b)		
	5D	04 (h)		
2	5C	xxx01000 (b)		
	5D	04 (h)		
3	5C	xxx01100 (b)		
	5D	04 (h)		
4	5C	xxx10000 (b)		
	5D	04 (h)		
5	5C	xxx10100 (b)		
	5D	04 (h)		
6	5C	xxx11000 (b)		
	5D	04 (h)		

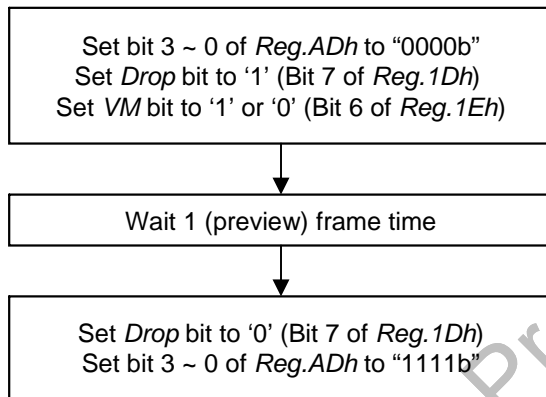
CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

- Vertical / Horizontal Mirror

Related Registers : TgControl1(Reg.1Dh), TgControl2(Reg.1Eh)

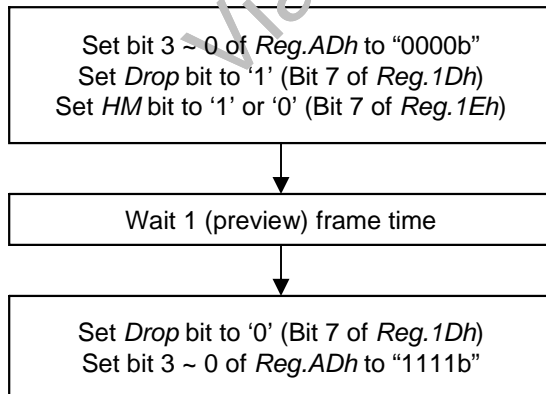
(1) Vertical Mirror

Vertical Mirror is controlled by *VM* bit (Bit 6 of *Reg.1Eh*).



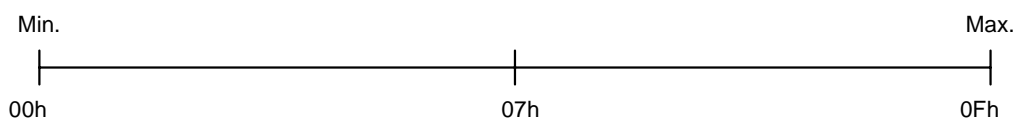
(2) Horizontal Mirror

Horizontal Mirror is controlled by *HM* bit (Bit 7 of *Reg.1Eh*).



- Lens shading Compensation

Related Registers : LensRGain (Reg.59h), LensGGain (Reg.5Ah), LensBGain (Reg.5Bh)



**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- Color Tone

Related Registers : ISPControl3 (Reg.4Fh), CbTone (Reg.9Fh), CrTone (Reg.A0h)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
4F	1xxxxxxx	<i>ISPControl3</i>	0xxxxxxx (b)	
9F	<i>Appropriate Value</i>	<i>CbTone</i>	00	
A0	<i>Appropriate Value</i>	<i>CrTone</i>	00	



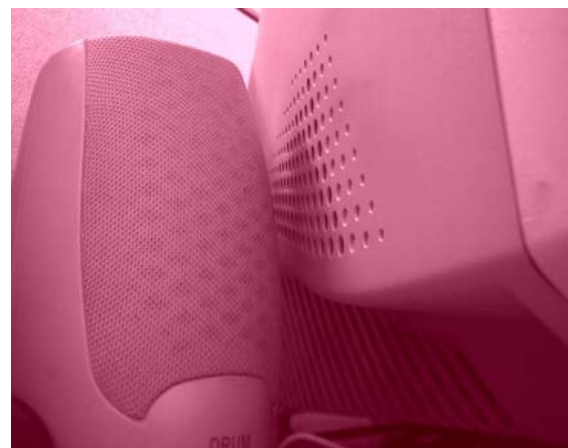
Sepia (Reg.9Fh = 98h, Reg.A0h = 1Ch)



Green (Reg.9Fh = 98h, Reg.A0h = 98h)



Aqua (Reg.9Fh = 28h, Reg.A0h = A0h)



Red (Reg.9Fh = 80h, Reg.A0h = 28h)

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**



Cool (Reg.9Fh = 20h, Reg.A0h = 98h)



Warm (Reg.90h = 9Fh, Reg.A0h = 28h)



BW (Reg.9Fh = 80h, Reg.A0h = 80h)



Antique (Reg.9Fh = 10h, Reg.A0h = 90h)

**CMOS Image Sensor with 640 X 480 Pixel Array
and Integrated On-Chip Image Signal Processor**

- PC Board Layout Considerations

It is important that care be given to the PC board layout to reduce power noise. Figure 1 shows a recommended connection diagram for the PO3030K.

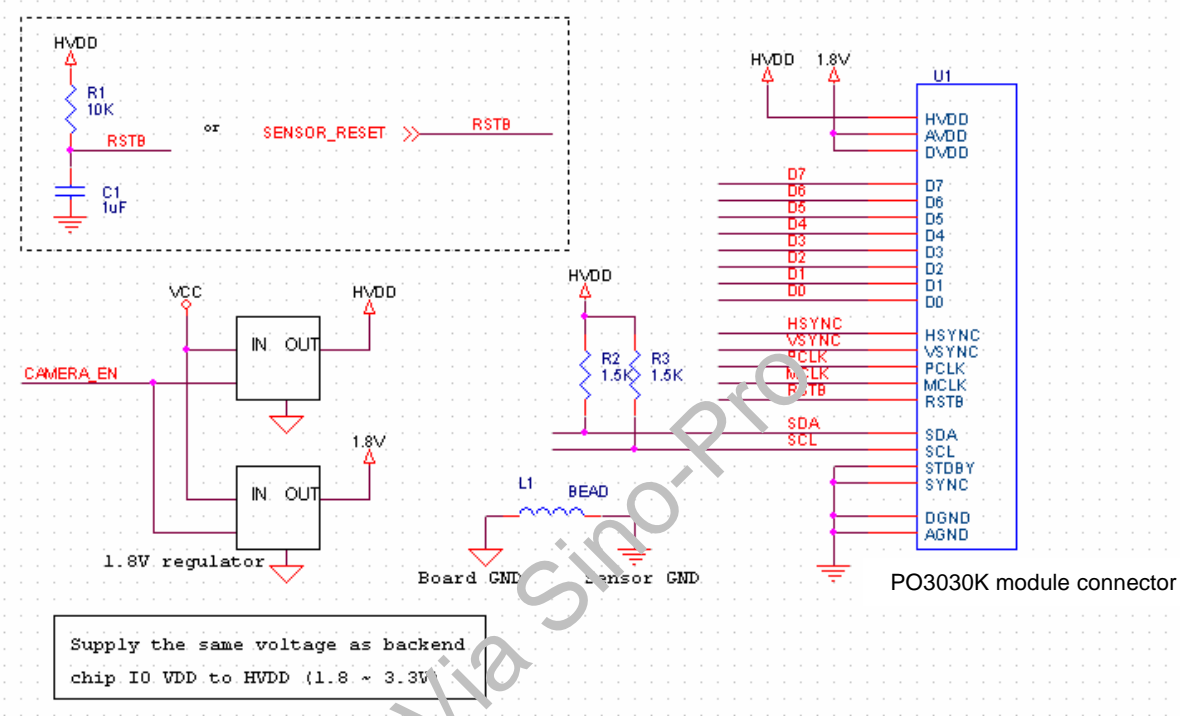


Figure 1. PO3030xC module typical connection diagram

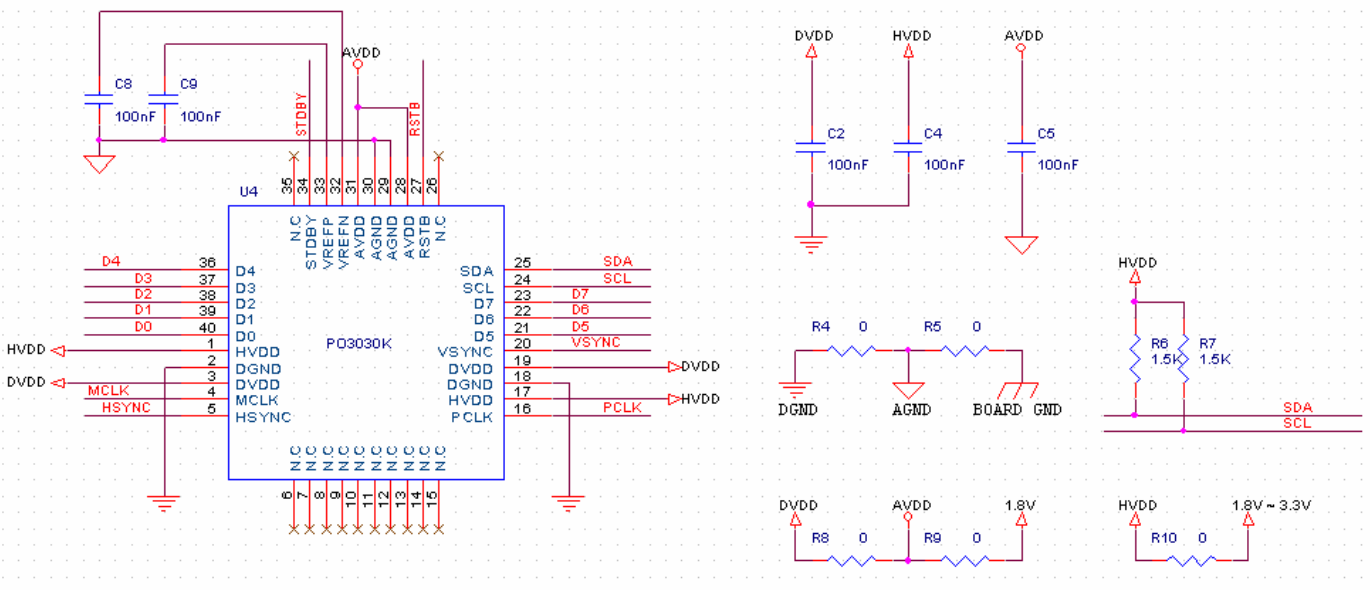


Figure 2. PO3030xC CLCC typical connection diagram

CMOS Image Sensor with 640 X 480 Pixel Array and Integrated On-Chip Image Signal Processor

Ground Planes

The ground plain should connect to the regular PCB ground plane at a single point

Power Planes

The PC board layout should have the distinct power plane for PO3030xC. This power plane should have the separate regulator or be connected to the regular PCB power plane(VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This power plane also has two distinct power planes, one for analog pins and one for digital pins. The analog power plane should encompass AVDD and PVDD pins, and the digital power plane should encompass DVDD pin.

Supply Decoupling

Noise on the PO3030xC power plane can be reduced by the use of multiple decoupling capacitors. (See Figure 2.) Optimum performance is achieved by the use of 0.1uF ceramic capacitors. Each of the power pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to power pins with the capacitor leads as short as possible, thus minimizing lead inductance.

- Stand-by method

1. Power cut-off

- ⇒ *Sensor reset can be controlled by power cut-off by connecting RSTB pin to HVDD not other VDD using 10K resistor and 1uF capacitor as shown in above Figure 1.*
- ⇒ *STDBY pin must be connected to DGND*
- ⇒ CAMERA_EN signal can be controlled by Backend chip or MCU.

2. Standby pin

- ⇒ You can control stand-by mode by using STDBY pin.

'0' : normal mode

'1' : stand-by (sleep) mode

3. I2C Stand-by

- ⇒ You can control stand-by mode by setting STDBY bit (bit 6) of Reg.1Fh.
- ⇒ *STDBY pin must be connected to DGND*

'0' : normal mode

'1' : stand-by (sleep) mode