PIXELPLUS CO., LTD.

Preliminary
Data sheet

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1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

PO6030K

Rev 0.52

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1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ *Revision History*

Version	Date [D/M/Y]	Notes	Writer
0.0	19/09/2007	*(Preliminary)*	Jong Hwan Kim
0.1	04/10/2007	Customer datasheet	Sung Je Cheon
0.2	01/11/2007	Modified application note	Sung Je Cheon
0.3	03/12/2007	Filled in Typical Table	Ju Yeon Kim
0.31	13/12/2007	Modified application note	Sung Je Cheon
0.4	10/01/2008	Add DC characteristics and Electro-Optical characteristics	Jun Hee Cho
0.5	15/01/2008	Add IDDS and IDDD characteristics @AVDD=1.8V Add AC characteristics	Jun Hee Cho
0.51	06/03/2008	Changed PVDD to AVDD1 at 4page	Ju Yeon Kim
0.52	10/03/2008	Modified I_{DDD} in DC characteristics	Ju Yeon Kim

Caution : This datasheet can be changed without prior notice !! If you want to get up-to-date version, please send a mail to support@pixelplus.co.kr.

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

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1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Features

▷ 656 x 496 total pixel array with RGB bayer color filters and micro-lens.

▷ Power supply :
AVDD : 2.8V, AVDD1 : 2.8V
DVDD : 1.5/1.8V, HVDD : 1.5 ~ 3.3V

▷ Output formats : CCIR656, 8bit YCbCr422, 8bit RGB Bayer, RGB565, RGB444, 8bit Mono.

▷ Image processing on chip : lens shading compensation, gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, brightness, contrast, saturation, auto black level compensation, auto white balance, auto exposure control and back light compensation.

▷ Max. 30 frames/sec progressive scan @ 24 MHz master clock for VGA

▷ Frame size, window size and position can be programmed through a 2 wire serial interface bus.

▷ VGA / QVGA / QQVGA / CIF / QCIF Scaling.

▷ Horizontal / Vertical mirroring.

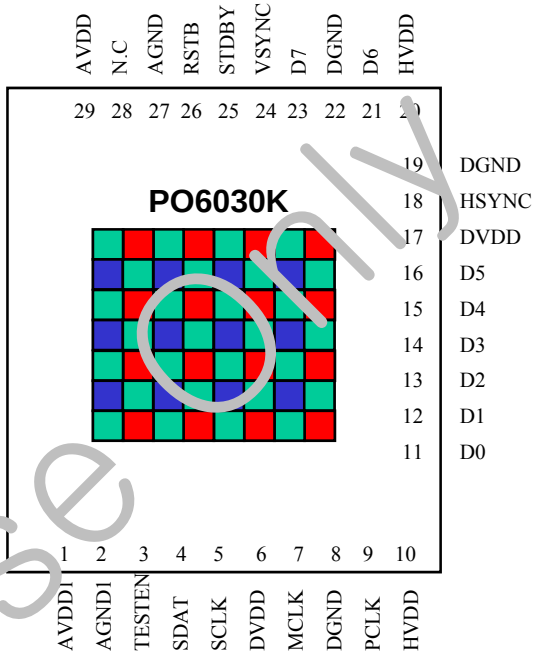
▷ 50Hz, 60Hz flicker automatic cancellation.

▷ Soft reset.

▷ High Image Quality and High low light performance.

▷ Large angle response.

▷ Support Chip scale package.



[Fig. 1] PIN Description (DIE)

Total Pixel Array	656 x 496
Pixel Size	3.6 um x 3.6 um
Effective Image Area	2.361mm x 1.785 mm
Clock Frequency	24 MHz
Frame Rate	Variable up to 30fps
Dark Signal	28.6 [mV/sec] @60'C
Sensitivity	1.46 [V/Lux.sec]
Saturation Level	1200 [mV]
Power Consumption	66.85 [mW] @ Dynamic @DVDD 1.5V
	40.68 [uW] @ Standby @DVDD 1.5V
Operating Temp. (Fully Functional Temp.)	-30'C ~ 70'C
Dynamic Range	50.3 [dB] @60'C
SNR	43 [dB] @60'C

[Table 1] Typical Parameters

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ PIN Descriptions

[Table 2] Pin Descriptions

Pin #	Name	I/O	Functions / Descriptions
1	AVDD1	P	Analog VDD1 : 2.8V DC. 0.1uF to AGND1
2	AGND1	P	Analog ground1.
3	TESTEN	I	Chip Test Mode enable. User must connect this terminal to DGND
4	SDAT	I/O	2-wire serial interface data bus.
5	SCLK	I	2-wire serial interface clock input.
6	DVDD	P	Digital vdd for core logic : 1.5V or 1.8V DC. 0.1uF capacitor to DGND.
7	MCLK	I	Master clock input pad.
8	DGND	P	Digital ground for core circuits.
9	PCLK	O	Pixel clock. Data can be latched by external devices at the rising or falling edge of PCLK. The polarity can be controlled.
10	HVDD	P	Digital vdd for I/O : 1.5 ~ 3.3V DC. Voltage range for all output signals is 0V ~ HVDD. 0.1uF to DGND
11	D0	O	Bit 0 of data output.
12	D1	O	Bit 1 of data output.
13	D2	O	Bit 2 of data output.
14	D3	O	Bit 3 of data output.
15	D4	O	Bit4 of data output.
16	D5	O	Bit5 of data output.
17	DVDD	P	Digital vdd for core logic : 1.5V or 1.8V DC. 0.1uF capacitor to DGND.
18	HSYNC	O	Horizontal synchronization pulse. HSYNC is high (or low) for the horizontal window of interest. It can be programmed to appear or not outside the vertical window of interest.
19	DGND	P	Digital ground for core.
20	HVDD	P	Digital vdd for I/O : 1.5 ~ 3.3V DC. Voltage range for all output signals is 0V ~ HVDD. 0.1uF to DGND
21	D6	O	Bit 6 of data output.
22	DGND	P	Digital ground for core.
23	D7	O	Bit 7 of data output.
24	VSYNC	O	Vertical sync : Indicates the start of a new frame.
25	STDBY	I	Power standby mode. When Standby='1' there's no current flow in any analog circuit branch, neither any beat of digital clock. D<7:0> and PCLK, HSYNC, VSYNC pins can be programmed to tri-state or all '1' or all '0'. But it is possible to control internal registers through 2-wire serial interface bus in Standby mode. All registers retain their current values.
26	RSTB	I	System reset must remain low for at least 16 master clocks after power is stabilized. When the sensor is reset, all registers are set to their defaults.
27	AGND	P	Analog ground.
28	N.C		No Connection
29	AVDD	P	Analog VDD : 2.8V DC. 0.1uF to AGND

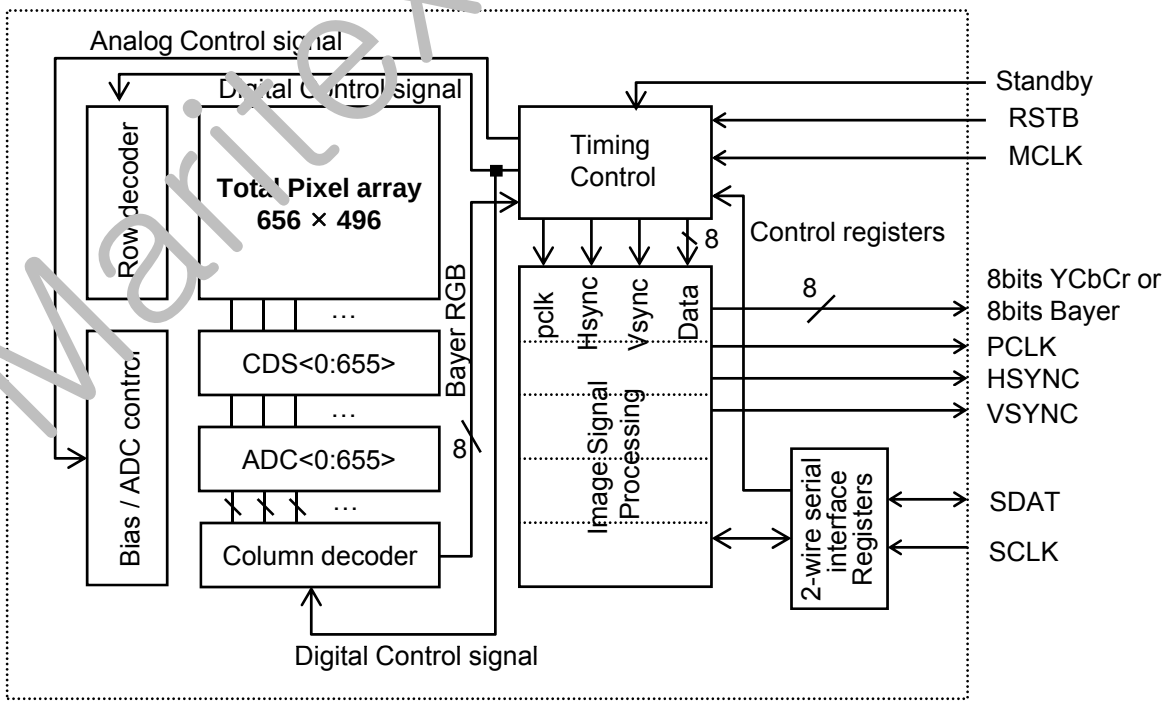
1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Signal Environment

PO60300K has 3.3V tolerant Input pads. Input signals must be higher than or equal to HVDD but cannot be higher than 3.3V. PO60300K input pad has built in reverse current protection circuit, which makes it possible to apply input voltage even if the HVDD is disconnected or floating. Voltage range for all output signals is 0V ~ HVDD.

▶ Chip Architecture

PO60300K has 656 x 496 total pixel array and column/row driver circuits to read out the pixel data progressively. CDS circuit reduces noise signals generated from various sources mainly resulting from process variations. Pixel output is compared with the reset level of its own and only the difference signal is sampled, thus reducing fixed error signal level. Each of R, G, B pixel output can be multiplied by different gain factors to balance the color of images in various light conditions. The analog signals are converted to digital forms one line at a time and 1 line data are streamed out column by column. The Bayer RGB data are passed through a sequence of image signal processing blocks to finally produce YCbCr 4:2:2 output data. Image signal processing includes such operations as gamma correction, defect correction, low pass filter, color interpolation, edge enhancement, color correction, contrast stretch, color saturation, white balance, exposure control and back light compensation. Internal functions and output signal timing can be programmed simply by modifying the register files through 2-wire serial interface.

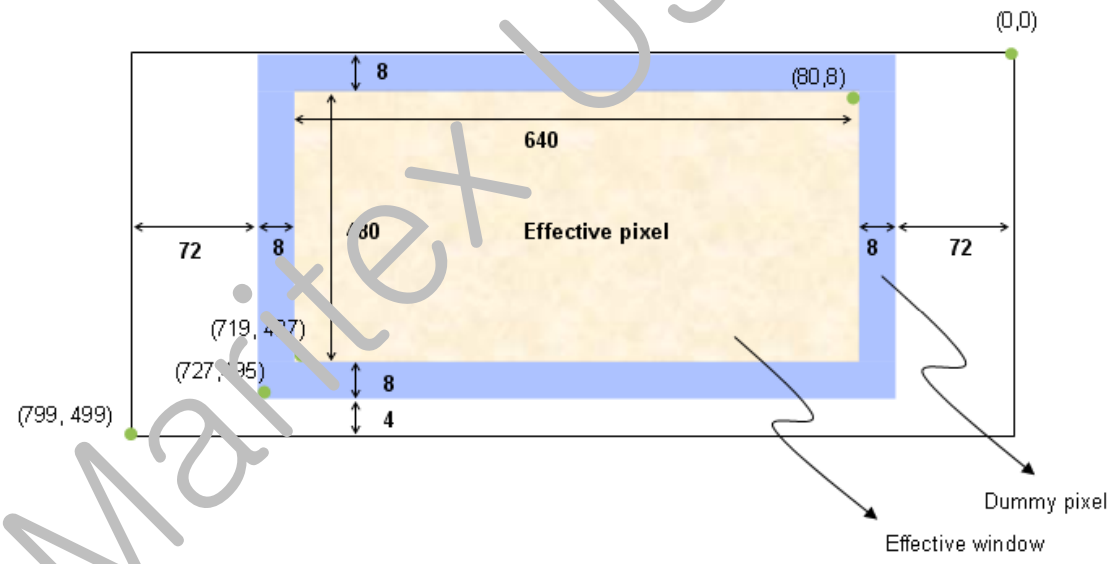


[Fig. 2] Block Diagram

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

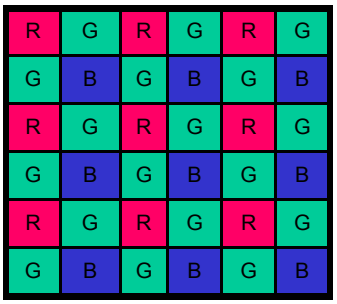
▶ *Frame Structure and Windowing*

Origin *(0, 0)* of the frame is at the upper right corner. Size of the frame is determined by two registers : *framewidth(Reg.B-48h, B-49h)* and *frameheight(Reg.B-29h, B-2Ah).* One frame consists of *framewidth + 1* columns and *frameheight + 1* rows. *framewidth* and *frameheight* can be programmed to be larger than total array size. Default window array of 640 x 480 pixels is positioned at *(80, 8).* It is possible to define a specific region of the frame as a window. Pixel scanning begins from *(0, 0)* and proceeds row by row downward, and for each line scan direction is from right to the left. Hsync signal indicates if the output is from a pixel that belongs to the window or not. There are two counters to indicate the present coordinate of frame scanning : Frame row counter and frame column counter. Counter values repeat the cycle of 0 to *frameheight* , and 0 to *framewidth* respectively. The counter values increase at the pace of pixel clock (PCLK), which does not change as the frame size is altered. The pixel data rate is fixed and is independent of frame size(frame rate).



[Fig. 3] Default data structure of frame and window. (Top view)

▶ Data Formats



[Fig. 4] Bayer Color filter pattern

Pixel array is covered by Bayer color filters as can be seen in the [Fig. 4]. Since each pixel can have only one type of filter on it, only one color component can be produced by a pixel. PO6030K provides this Bayer pattern RGB data through an 8bit channel. It takes one PCLK to pass one pixel RGB data to output bus. But since it is necessary to know all 3 color components R, G, B to produce a color for a pixel, the other two components must be inferred from other pixel data. For example, G component for a B pixel is calculated as an average of its four nearest G neighbors, and its R component as an average of its four nearest R neighbors. This operation of inferring missing data from existing ones is called the color interpolation. Color interpolation produces an undesirable artifact in image. Sampling nature of color filter can leave an interference pattern around an area with repetitive fine lines. PO6030K adopts a low pass filter to prevent the interference patterns (called Moire pattern) from degrading the image quality too much. After color interpolation, every pixel has all three color components. These three color components R, G, B can be routed to 8 bits output pins in such a way RGB565. It takes two PCLK's to pass one pixel RGB data to output bus.

It is possible to extract monochrome luminance data from RGB color components and the conversion equation is : Y = 0.299R + 0.587G + 0.114B where R,G and B are gamma corrected color components. And the color information is separated from luminance information according to following equations.

$$Cb = -0.148R - 0.291G + 0.439, \quad Cr = 0.439R - 0.368G - 0.071B$$

Since human eyes are less sensitive to color variation than to luminance, color components can be sub-sampled to reduce the amount of data to be transmitted, but preserving almost the same image quality.

PO6030K supports 4:2:2 YCbCr data format where Cb and Cr components are horizontally sub-sampled such that U and V for every other pixel are omitted. PO6030K also support 4:2:2 YUV data format.

Cb1	Y1	Cr1	Y2	Cb3	Y3	Cr3	Y4	…

[Fig. 5] 4:2:2 YCbCr data sequence.

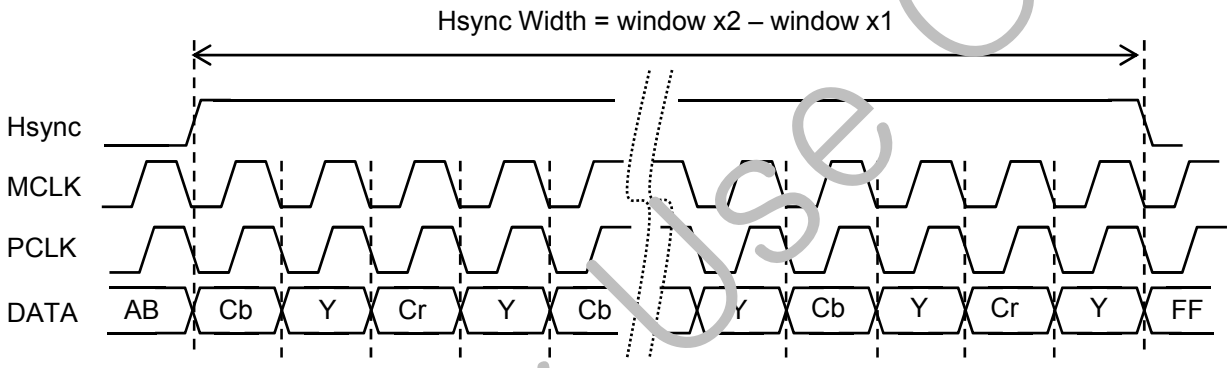
▶ Data and Synchronization Timing

[Fig. 6] shows the default data sequence of PO6030K. In [Fig. 6] Hsync / PCLK polarity can have any combinations possible. Data can be latched at the rising or falling edge of PCLK. Hsync can be set to be active high or active low. The sequence default YCbCr data is [Cb,Y, Cr, Y, …] for common even / odd rows.

The width of Hsync can be programmed by *windowx1 / x2(Reg.B-50h, 51h, 54h, 55h)* and given by

Hsync Width = *windowx2* - *windowx1*

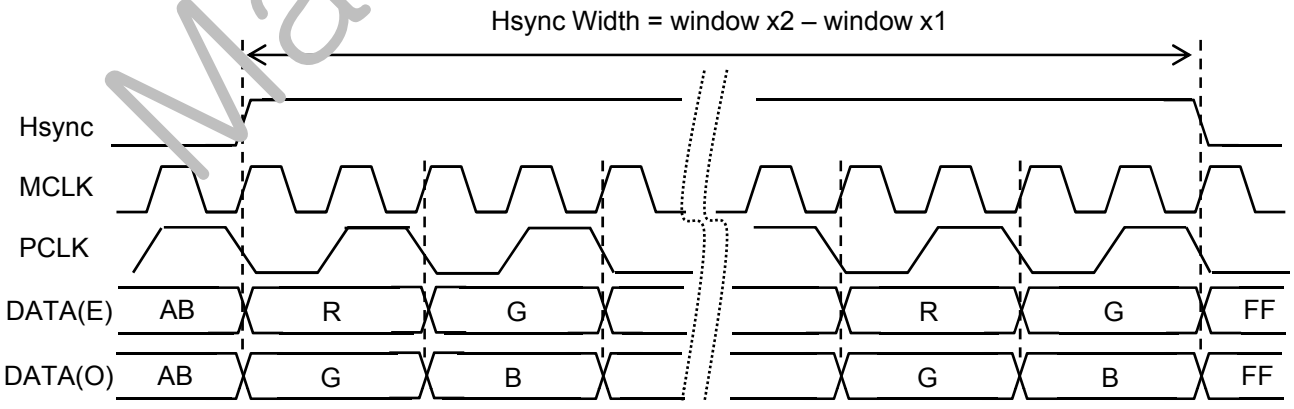
Data value can be selected in Invalid or blanking region . (Reg.B-74h ~ 7Bh)



[Fig. 6] Timing diagram for Hsync, MCLK, PCLK and Data (default)

The default sequence Bayer data is [RGRG…] for even rows and [GBGB…] for odd rows. The data order can be changed by register (*bit7 and bit6 of Reg.B-33h).*

[Fig. 7] shows the bayer data sequence of PO6030K. PCLK frequency is MCLK/2 when output data is bayer data.



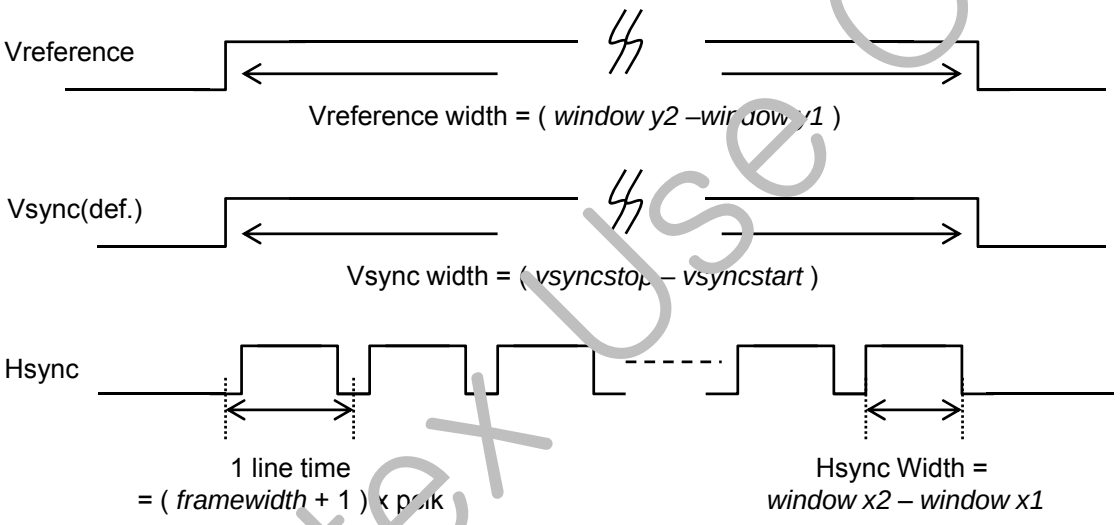
[Fig. 7] Timing diagram for Hsync, MCLK, PCLK and Data (Bayer)

In [Fig. 8], Vsync polarity also can have any combinations possible and can be set to be active high or active low. The width of Vsync can be programmed by *vsyncstart / vsyncstop(Reg.B-60h ~ 65h)* and given by

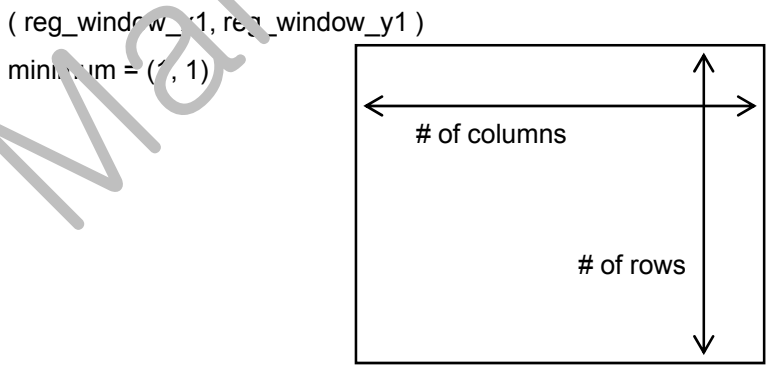
Vsync Width = (*vsyncstop – vsyncstart*).

The width of Vreference can be programmed by register *windowy1 / y2(Reg.B-52h, 53h, 56h, 57h)* and given by

Vreference width = (*windowy2 - windowy1*).



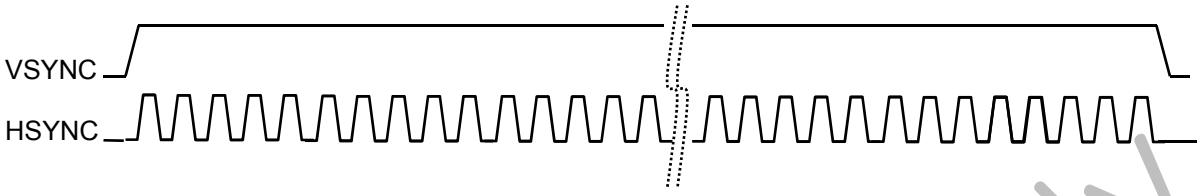
[Fig. 8] Timing diagram for Vsync and Hsync



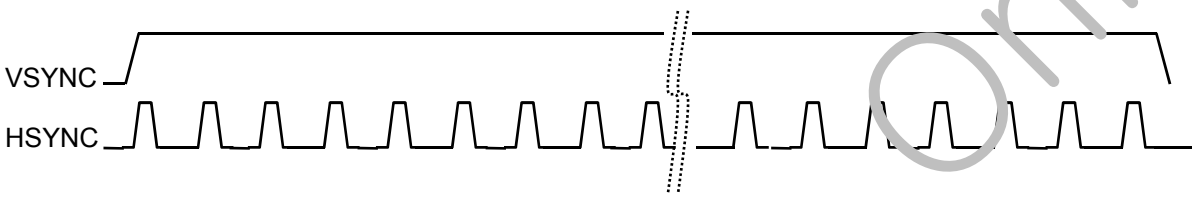
[Fig. 9] Effective Image Size

Effective Image. # of columns = reg_window_x2 - reg_window_x1

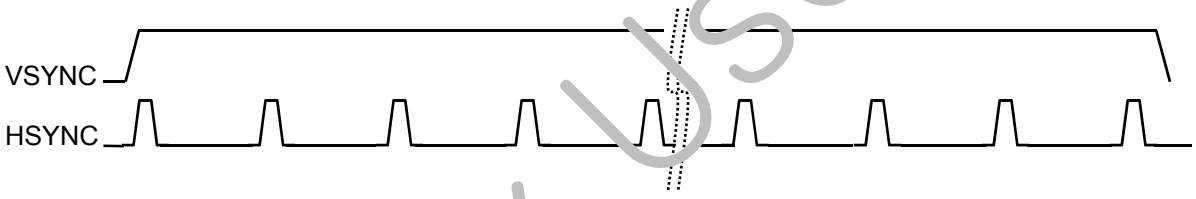
Effective Image. # of rows = reg_window_y2 - reg_window_y2



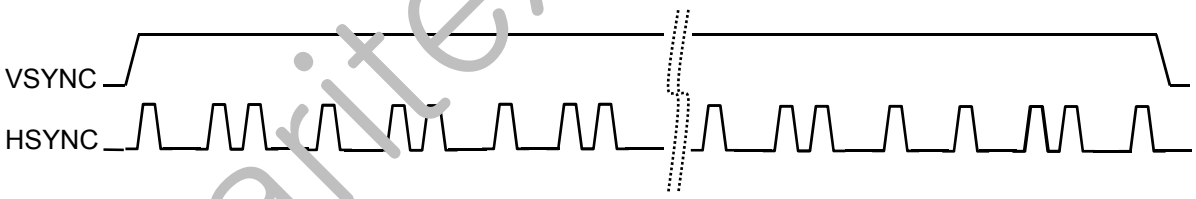
[No scaling case : default]



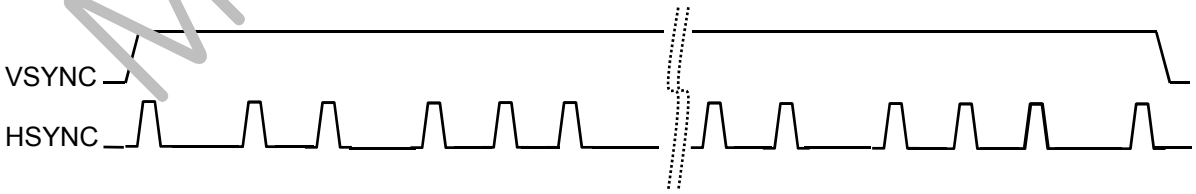
[QVGA scaling case]



[QQVGA scaling case]

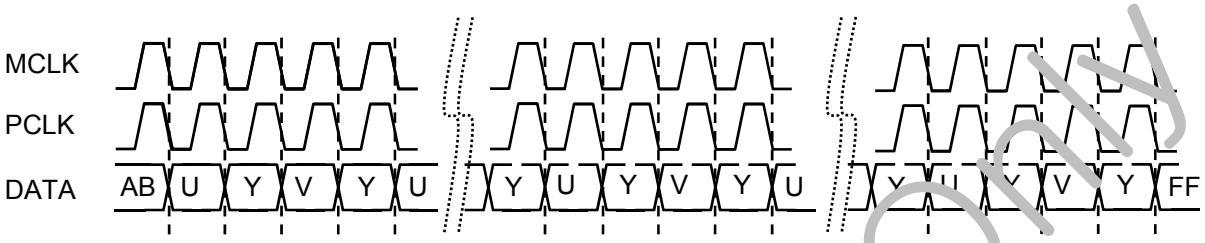


[CIF scaling case]

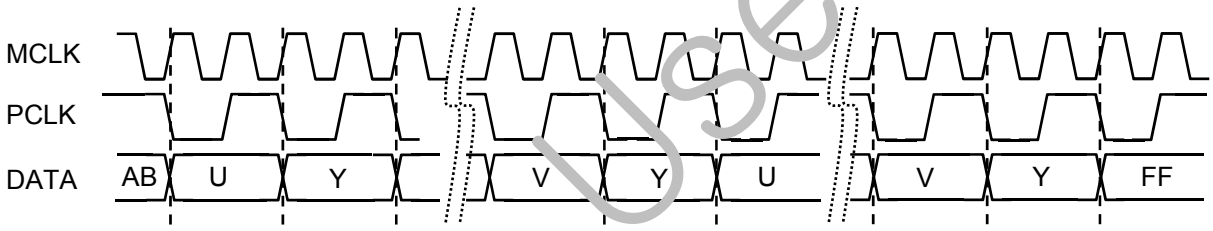


[QCIF scaling case]

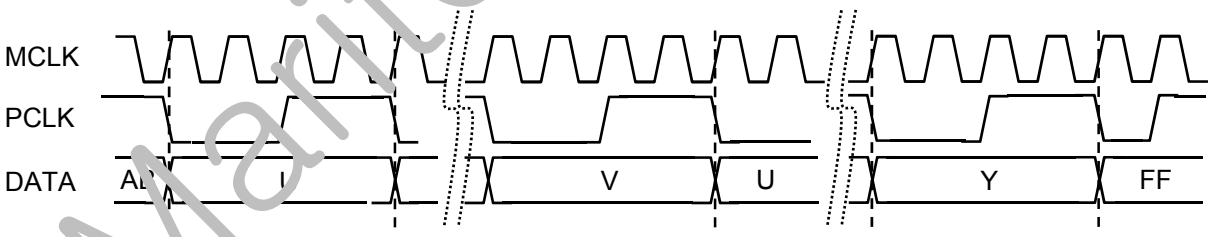
[Fig. 10] Timing diagram for VSYNC and HSYNC (scaling modes)



[No scaling case : default]



[QVGA/CIF scaling case]



[QQVGA/QCIF scaling case]

[Fig. 11] Timing diagram for PCLK and Data (scaling modes)

▶ 2-wire Serial Interface Description

The registers of PO6030K are written and read through the 2-wire Serial Interface. The PO6030K has 2-wire Serial Interface slave. The PO6030K is controlled by the Register Access Clock (SCLK), which is driven by the 2-wire Serial Interface master. Data is transferred into and out of the PO6030K through the Register Access Data (SDAT) line. The SCLK and SDAT lines are pulled up to VDD by a 2kΩ off-chip resistor. Either the slave or master device can pull the lines down. The 2-wire Serial Interface protocol determines which device is allowed to pull the two lines down at any given time.

Start bit

The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH.

Stop bit

The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a 2-wire Serial Interface device consists of 7-bit of address and 1-bit of direction. A '0' in the LSB of the address indicates write mode, and a '1' indicates read-mode.

Data bit transfer

One data bit is transferred during each clock pulse. The SCLK pulse is provided by the master. The data must be stable during the HIGH period of the SCLK : it can only change when the SCLK is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge bit

The receiver generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse.

No-acknowledge bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

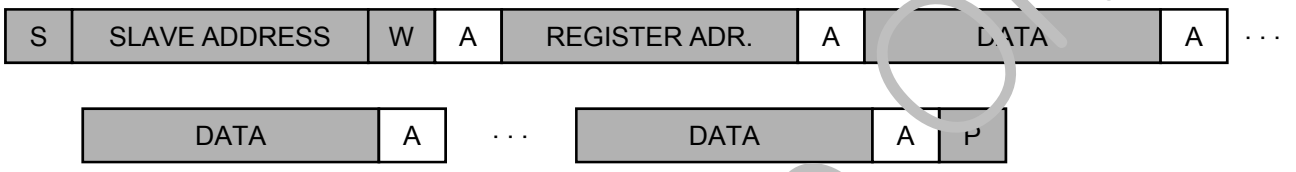
Sequence

A typical read or write sequence begins by the master sending a start bit. After start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master. If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PO6030K uses 8 bit data for its internal registers, thus requiring one 8-bit transfer to write to one register. After 8 bits are transferred, the register address is automatically incremented, so that the next 8 bits are written to the next register address. The master stops writing by sending a start or stop bit. A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after each 8 bit is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

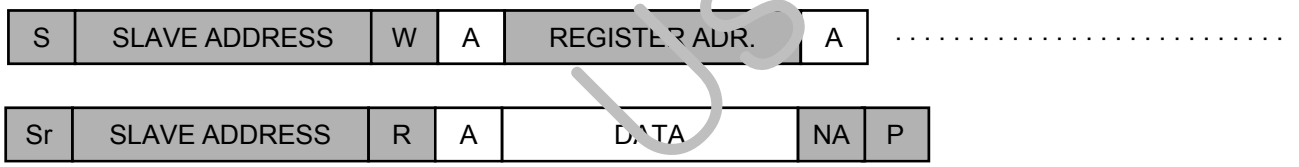
▶ 2-wire Serial Interface Functional Description

Single Write Mode operation

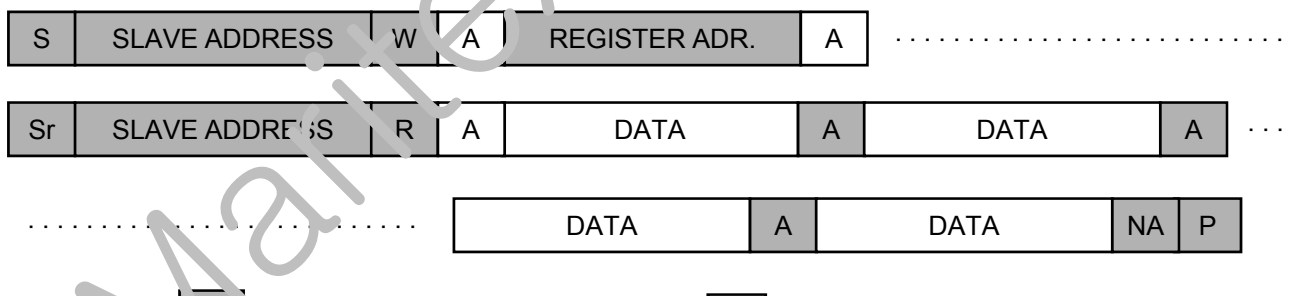
Multiple Write Mode (Register address is increased automatically)[1] operation



Single Read Mode operation



Multiple Read Mode (Register address is increased automatically)[1] operation



S: Start condition. Sr : Repeated Start (Start without preceding stop.)
SLAVE ADDRESS: write address = DCh = 11011100b
read address = DDh = 11011101b
R/W: Read/Write selection. High = read / LOW = write.
A: Acknowledge bit. NA : No Acknowledge.
DATA: 8-bit data
P: Stop condition

Note 1: Continuous writing or reading without any interrupt increases the register address automatically. If the address is increased above valid register address range, further writing does not affect the chip operation in write mode. Data from invalid registers are undefined in read mode.

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▶ Register Tables (Group A)

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
0	00	DeviceID_H	96	60	01100000	RO	0	device ID
1	01	DeviceID_L	48	30	00110000	RO	0	
2	02	RevNumber	1	01	00000001	RO	0	revision number
3	03	bank	1	00	xxxxxx01	RW	4	register group selector
21	15	analog_control_06	23	17	00010111	RW	4	analog control register 06
144	90	bayer_control_01	53	35	00110101	RW	2	bayer control register 01
145	91	bayer_control_02	16	10	00010000	RW	2	bayer control register 02

(Group A : continue)

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables (Group B)

#		register name	default value			type	stage	
dec	hex		dec	hex	bin			
256	00	DeviceID_H	96	60	01100000	RO	0	device ID
257	01	DeviceID_L	48	30	00110000	RO	0	
258	02	RevNumber	1	01	00000001	RO	0	revision number
259	03	bank	1	00	xxxxxx01	RW	4	register group selector
273	11	flicker_control2	0	00	00000000	RW	0	flicker mode control register 2
289	21	fd_period_60_h	0	00	00000000	RW	4	flicker period for 60Hz (H)
290	22	fd_period_a_m	80	50	01010000	RW	4	flicker period for 60Hz (M)
291	23	fd_period_a_l	192	C0	11000000	RW	4	flicker period for 60Hz (L)
292	24	fd_period_b_h	0	00	00000000	RW	4	flicker period for 50Hz (H)
293	25	fd_period_b_m	67	43	01000011	RW	4	flicker period for 50Hz (M)
294	26	fd_period_b_l	74	4A	01001010	RW	4	flicker period for 50Hz (L)
295	27	fd_period_c_h	1	01	00000001	RW	4	flicker period for CASE C (H)
296	28	fd_period_c_m	147	93	10010011	RW	4	flicker period for CASE C (M)
297	29	fd_fheight_a_h	1	01	00000001	RW	4	flicker frameheight for 60Hz (H)
298	2A	fd_fheight_a_l	243	F3	11110011	RW	4	flicker frameheight for 60Hz (L)
299	2B	fd_fheight_b_h	1	01	00000001	RW	4	flicker frameheight for 50Hz (H)
300	2C	fd_fheight_b_l	243	F3	11110011	RW	4	flicker frameheight for 50Hz (L)
304	30	isp_func_0	255	FF	11111111	RW	2	ISP control register 00
306	32	isp_func_2	1	01	00000001	RW	2	ISP control register 02
307	33	isp_func_3	216	D8	11011000	RW	2	ISP control register 03
308	34	i2c_control_1	80	50	01010000	RW	4	I2C control register 01
312	38	format	0	00	00000000	RW	4	Output Format control register
320	40	tp_control_0	0	00	00000000	RW	4	Test Pattern control register 00
321	41	tp_control_1	255	FF	11111111	RW	4	Test Pattern control register 01
322	42	tp_control_2	255	FF	11111111	RW	4	Test Pattern control register 02
323	43	tp_control_3	255	FF	11111111	RW	4	Test Pattern control register 03
324	44	tp_control_4	255	FF	11111111	RW	4	Test Pattern control register 04
325	45	tp_control_5	0	00	00000000	RW	4	Test Pattern control register 05
328	48	framewidth_h	3	03	00000011	RW	4	framewidth (H)
329	49	framewidth_l	31	1F	00011111	RW	4	framewidth (L)
336	50	windowx1_h	0	00	00000000	RW	2	window X1 (H)
337	51	windowx1_l	7	07	00000111	RW	2	window X1 (L)
338	52	windowy1_h	0	00	00000000	RW	2	window Y1 (H)
339	53	windowy1_l	7	07	00000111	RW	2	window Y1 (L)
340	54	windowx2_h	2	02	00000010	RW	2	window X2 (H)
341	55	windowx2_l	134	86	10000110	RW	2	window X2 (L)
342	56	windowy2_h	1	01	00000001	RW	2	window Y2 (H)
343	57	windowy2_l	230	E6	11100110	RW	2	window Y2 (L)
352	60	vsyncstartrow_h	0	00	00000000	RW	4	Output Vsync Row Start (H)
353	61	vsyncstartrow_l	12	0C	00001100	RW	4	Output Vsync Row Start (L)
354	62	vsyncstoprow_h	1	01	00000001	RW	4	Output Vsync Row Stop (H)
355	63	vsyncstoprow_l	236	EC	11101100	RW	4	Output Vsync Row Stop (L)
356	64	vsynccolumn_h	0	00	00000000	RW	4	Output Vsync Column Start (H)
357	65	vsynccolumn_l	16	10	00010000	RW	4	Output Vsync Column Start (L)
360	68	sync_control_0	0	00	00000000	RW	2	Synchronization control register 00
361	69	sync_control_1	2	02	00000010	RW	4	Synchronization control register 01
372	74	sync_ccirFF	255	FF	11111111	RW	4	CCIR data format FFh
373	75	sync_ccir00	0	00	00000000	RW	4	CCIR data format 00h
374	76	sync_ccir80	128	80	10000000	RW	4	CCIR data format 80h
375	77	sync_ccir10	16	10	00010000	RW	4	CCIR data format 10h
376	78	sync_blankSAV	182	B6	10110110	RW	4	blank SAV
377	79	sync_blankEAV	157	9D	10011101	RW	4	blank EAV
378	7A	sync_activSAV	171	AB	10101011	RW	4	active SAV
379	7B	sync_activEAV	128	80	10000000	RW	4	active EAV
384	80	scale_x	32	20	00100000	RW	2	Horizontal scale factor (20h =x1)
385	81	scale_y	32	20	00100000	RW	2	Vertical scale factor (20h =x1)

(Group B : continue)

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables (Group B)

388	84	sephia_cb	192	C0	11000000	RW	2	Cb sephia
389	85	sephia_cr	64	40	01000000	RW	2	Cr sephia
392	88	sketchoffset1	32	20	00100000	RW	2	scatch offset 1
393	89	sketchoffset2	200	C8	11001000	RW	2	scatch offset 2
394	8A	sketchoffset3	16	10	00010000	RW	2	scatch offset 3
395	8B	sketchoffset4	128	80	10000000	RW	2	scatch offset 4
400	90	cs_max	255	FF	11111111	RW	2	max. color
401	91	ycontrast	64	40	01000000	RW	2	Y contrast
402	92	ybrightness	1	01	00000001	RW	2	Brightness
403	93	ymax	254	FE	11111110	RW	2	max. Y
412	9C	edge_gain	36	24	00100100	RW	4	Edge Gain
413	9D	edge_th	16	10	00010000	RW	4	Edge Threshold
420	A4	cc11	56	38	00111000	RW	4	Color correction matrix (11)
421	A5	cc12	165	A5	10100101	RW	4	Color correction matrix (12)
422	A6	cc13	13	0D	00001101	RW	4	Color correction matrix (13)
423	A7	cc21	147	93	10010011	RW	4	Color correction matrix (21)
424	A8	cc22	45	2D	00101101	RW	4	Color correction matrix (22)
425	A9	cc23	6	06	00000110	RW	4	Color correction matrix (23)
426	AA	cc31	131	83	10000011	RW	4	Color correction matrix (31)
427	AB	cc32	170	AA	10101010	RW	4	Color correction matrix (32)
428	AC	cc33	77	4D	01001101	RW	4	Color correction matrix (33)
432	B0	gm_y0	0	00	00000000	RW	4	Gamma Y0
433	B1	gm_y1	10	0A	00001010	RW	4	Gamma Y1
434	B2	gm_y2	23	17	00010111	RW	4	Gamma Y2
435	B3	gm_y3	36	24	00100100	RW	4	Gamma Y3
436	B4	gm_y4	47	2F	00101111	RW	4	Gamma Y4
437	B5	gm_y5	65	41	01000001	RW	4	Gamma Y5
438	B6	gm_y6	80	50	01010000	RW	4	Gamma Y6
439	B7	gm_y7	103	67	01100111	RW	4	Gamma Y7
440	B8	gm_y8	119	77	01110111	RW	4	Gamma Y8
441	B9	gm_y9	149	95	10010101	RW	4	Gamma Y9
442	BA	gm_y10	174	AE	10101110	RW	4	Gamma Y10
443	BB	gm_y11	197	C5	11000101	RW	4	Gamma Y11
444	BC	gm_y12	218	DA	11011010	RW	4	Gamma Y12
445	BD	gm_y13	237	ED	11101101	RW	4	Gamma Y13
446	BE	gm_y14	255	FF	11111111	RW	4	Gamma Y14
460	CC	lens_gainr	0	00	00000000	RW	4	Red lens gain
461	CD	lens_gaing	0	00	00000000	RW	4	Green lens gain
463	CF	lens_gainb	0	00	00000000	RW	4	Blue lens gain
464	D0	lens_offset_h	6	06	00000110	RW	4	lens column offset (H)
465	D1	lens_offset_l	95	5F	01011111	RW	4	lens column offset (L)
466	D2	lens_rx	0	00	00000000	RW	4	red lens x origin
467	D3	lens_ry	0	00	00000000	RW	4	red lens y origin
468	D4	lens_gx	0	00	00000000	RW	4	green lens x origin
469	D5	lens_gy	0	00	00000000	RW	4	green lens y origin
472	D8	lens_bx	0	00	00000000	RW	4	blue lens x origin
473	D9	lens_by	0	00	00000000	RW	4	blue lens y origin
474	DA	lens_scale	81	51	01010001	RW	4	East/West/South/North lens scale factor

(Group B : continue)

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables (Group C)

#		register name	default value			type	stage	
dec	hex		dec	hex	bin			
512	00	DeviceID_H	96	60	01100000	RO	0	device ID
513	01	DeviceID_L	48	30	00110000	RO	0	
514	02	RevNumber	1	01	00000001	RO	0	revision number
515	03	bank	1	00	xxxxxx01	RW	4	register group selector
516	04	auto_control_1	152	98	10011000	RW	2	auto control register 01
517	05	auto_control_2	13	0D	00001101	RW	2	auto control register 02
528	10	ae_winx_h	0	00	00000000	RW	4	AE window X (H)
529	11	ae_winx_l	37	25	00100101	RW	4	AE window X (L)
530	12	ae_winy_h	0	00	00000000	RW	4	AE window Y (H)
531	13	ae_winy_l	28	1C	00011100	RW	4	AE window Y (L)
532	14	ae_width_h	2	02	00000010	RW	4	AE window Width (H)
533	15	ae_width_l	96	60	01100000	RW	4	AE window Width (L)
534	16	ae_height_h	1	01	00000001	RW	4	AE window Height (H)
535	17	ae_height_l	190	BE	10111110	RW	4	AE window Height (L)
536	18	ae_cwinx_h	0	00	00000000	RW	4	AE Center window X (H)
537	19	ae_cwinx_l	229	E5	11100101	RW	4	AE Center window X (L)
538	1A	ae_cwiny_h	0	00	00000000	RW	4	AE Center window Y (H)
539	1B	ae_cwiny_l	135	87	10000111	RW	4	AE Center window Y (L)
540	1C	ae_cwidth_h	0	00	00000000	RW	4	AE Center window Width (H)
541	1D	ae_cwidth_l	160	A0	10100000	RW	4	AE Center window Width (L)
542	1E	ae_cheight_h	0	00	00000000	RW	4	AE Center window Height (H)
543	1F	ae_cheight_l	160	A0	10100000	RW	4	AE Center window Height (L)
548	24	ext_inttime_h	0	00	00000000	RW	2	External Integration Time (H)
549	25	ext_inttime_m	128	80	10000000	RW	2	External Integration Time (M)
550	26	ext_inttime_l	0	00	00000000	RW	2	External Integration Time (L)
552	28	ext_glbg_h	1	01	00000001	RW	2	External Globalgain (H)
553	29	ext_glbg_l	0	00	00000000	RW	2	External Globalgain (L)
556	2C	exposure_t	0	00	00000000	RW	2	Current Exposure (T)
557	2D	exposure_h	0	00	00000000	RW	2	Current Exposure (H)
558	2E	exposure_m	128	80	10000000	RW	2	Current Exposure (M)
559	2F	exposure_l	0	00	00000000	RW	2	Current Exposure (L)
564	34	midfrmheight_h	3	03	00000011	RW	4	Middle FrameHeight (H)
565	35	midfrmheight_l	230	E6	11100110	RW	4	Middle FrameHeight (L)
566	36	maxfrmheight_h	7	07	00000111	RW	4	Max FrameHeight (H)
567	37	maxfrmheight_l	204	CC	11001100	RW	4	Max FrameHeight (L)
572	3C	midexp_t	0	00	00000000	RW	4	Middle Exposure (T)
573	3D	midexp_h	31	1F	00011111	RW	4	Middle Exposure (H)
574	3E	midexp_m	48	30	00110000	RW	4	Middle Exposure (M)
576	40	maxexp_t	0	00	00000000	RW	4	Max Exposure (T)
577	41	maxexp_h	62	3E	00111110	RW	4	Max Exposure (H)
578	42	maxexp_m	96	60	01100000	RW	4	Max Exposure (M)
580	44	minexp_h	0	00	00000000	RW	4	Min Exposure (H)
581	45	minexp_m	0	00	00000000	RW	4	Min Exposure (M)
582	46	minexp_l	12	0C	00001100	RW	4	Min Exposure (L)
584	48	expFrmH_H	1	01	00000001	RW	4	Reference Exposure FrameHeight (H)
585	49	expFrmH_L	243	F3	11110011	RW	4	Reference Exposure FrameHeight (L)
588	4C	inttime_H	0	00	00000000	RW	2	Integration Time (H)
589	4D	inttime_M	128	80	10000000	RW	2	Integration Time (M)
590	4E	inttime_L	0	00	00000000	RW	2	Integration Time (L)
592	50	globalgain	0	00	00000000	RW	2	Globalgain
593	51	digitalgain	64	40	01000000	RW	2	Digital Gain
596	54	ae_c_weight	3	03	00000011	RW	2	AE Center Weight
597	55	ae_up_speed	8	08	00001000	RW	2	AE upside Speed
598	56	ae_down_speed	12	0C	00001100	RW	2	AE downside Speed
599	57	ae_lock	2	02	00000010	RW	2	AE lock range

(Group C : continue)

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables (Group C)

618	6A	ymean_h	0	00	00000000	RO	4	Ymean (H)
619	6B	ymean_l	128	80	10000000	RO	4	Ymean (L)
623	6F	user_wyt	128	80	10000000	RW	2	user Y target
644	84	awb_rgratio	128	80	10000000	RW	4	AWB Red/Green Ratio
645	85	awb_bgratio	128	80	10000000	RW	4	AWB Blue/Green Ratio
646	86	awb_lock	2	02	00000010	RW	4	AWB lock range
647	87	awb_speed	8	08	00001000	RW	4	AWB speed
672	A0	wb_rgain_min	0	00	00000000	RW	2	min Red gain for white balance
673	A1	wb_rgain_max	255	FF	11111111	RW	2	max Red gain for white balance
674	A2	wb_bgain_min	0	00	00000000	RW	2	min Blue gain for white balance
675	A3	wb_bgain_max	255	FF	11111111	RW	2	max Blue gain for white balance
676	A4	wb_rgain	64	40	01000000	RW	2	Red gain for white balance
677	A5	wb_ggain	64	40	01000000	RW	2	Green gain for white balance
678	A6	wb_bgain	64	40	01000000	RW	2	Blue gain for white balance
692	B4	user_cs	32	20	00100000	RW	2	User color saturation offset

(Group C : continue)

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Register Tables (Group D)

#		register name	default value			type	stage	
dec	hex		dec	hex	bin			
768	00	DeviceID_H	96	60	01100000	RO	0	device ID
769	01	DeviceID_L	48	30	00110000	RO	0	
770	02	RevNumber	1	01	00000001	RO	0	revision number
771	03	bank	1	00	xxxxxx01	RW	4	register group select
997	E5	avg_r	0	0		RO	0	Green average
998	E6	avg_g	0	0		RO	0	Blue average
999	E7	avg_b	0	0		RO	0	

▶ Register Tables (Detailed) : Group A

Register names are written in *slanted* characters. To differentiate between decimal, binary, and hexa numbers, (d, b, and h) are appended. The sensor should be reset by RSTB pin set low, after power is up, for at least 16 master clock periods. This will initialize all of the registers to their default values.

(0-3) DeviceID, RevNumber, Register Selector

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
0	00	DeviceID_H	96	60	01100000	RO	0	device ID
1	01	DeviceID_L	48	30	00110000	RO	0	
2	02	RevNumber	1	01	00000001	RO	0	revision number
3	03	bank	1	00	xxxxxx01	RW	4	register group selector

Default : 00h(Device_ID_H) = 60h, 01h(Device_ID_L) = 30h,
02h(Rev_Number) = 01h,
03h(Register Selector)= 00h.

Description :

Indicate PO6030K device ID, reversion number, Register Select.
Common registers of Group A(00h) / B(01h) / C(02h) / D(03h).

Register type
RO : Available Read Only
RW : Available Read and Write

< Group A >

(21) Analog control 06

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
21	15	analog_control_06	23	17	00010111	RW	4	analog control register 06

Default : 15h = 17h

Description :

register name : analog_control_06								
register #	bit#	name	default	23	default(h)	17	default(b)	00010111
21(d) 15(h)	7	x	0	x				
	6	x	0	x				
	5	pad_drivability	0	pad drivability Control 00b : x1 01b : x2 10b : x4(default) 11b : X8				
	4		1					
	3	x	0	x				
	2	Reserved	1					
	1	Reserved	1					
	0	Reserved	1					

< Group A >

(144) Bayer Control 01

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
144	90	bayer_control_01	53	35	00110101	RW	2	bayer control register 01

Default : 90h = 35h

Description :

register name : bayer_control_01								
register #	bit#	name	default	**53**	default(h)	**35**	default(b)	**00110101**
144(d) 90(h)	7	vm	0	**Vertical Mirror (VM)** '0' : Vertical Mirror disable. (default) '1' : Vertical Mirror enable.				
	6	hm	0	**Horizontal Mirror (HM)** '0' : Horizontal Mirror disable. (default) '1' : Horizontal Mirror enable.				
	5	Reserved	1					
	4	Reserved	1					
	3	Reserved	0					
	2	Reserved	1					
	1	Reserved	0					
	0	Reserved	1					

< Group A >

(145) Bayer Control 02

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
145	91	bayer_control_02	16	10	00010000	RW	2	bayer control register 02

Default : 90h = 10h

Description :

register name : bayer_control_02								
register #	bit#	name	default	16	default(h)	0	default(b)	00010000
145(d) 91(h)	7	clkdiv(2:0)	0	Clock Divide 000b : x 1 (default) 001b : x 2/3 010b : x 1/2 011b : x 1/3 100b : x 1/4 101b : x 1/5 else : x				
	6		0					
	5		0					
	4	Reserved	1					
	3	Reserved	0					
	2	Reserved	0					
	1	Reserved	0					
	0	Reserved						

< Group A >

(273) Filcker Control 2

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
273	11	flicker_control2	0	00	00000000	RW	0	flicker mode control register 02

Default : 11h = 00h

Description :

register name : flicker_control_2								
register #	bit#	name	default	0	default(h)	0	default(b)	00000000
273(d) 11(h)	7	x	0	x				
	6	x	0	x				
	5	Reserved	0					
	4	Reserved	0					
	3	manual60	0	Manual 60Hz flicker mode select				
	2	manual50	0	Manual 50Hz flicker mode select				
	1	fd_en	0	Auto Flicker Detection Enable 0 : Disable 1 : Enable				
	0	Reserved	0					

Mode	Bit3 (manual60)	Bit2 (manual50)	Bit1 (fd_en)
Normal (flicker mode off)	0	0	0
Manual 60Hz flicker mode	1	0	0
Manual 50Hz flicker mode	0	1	0
Auto Flicker Detection	0	0	1

< Group B >

(281-301) Flicker

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
289	21	fd_period_60_h	0	00	00000000	RW	4	flicker period for 60Hz (H)
290	22	fd_period_60_m	80	50	01010000	RW	4	flicker period for 60Hz (M)
291	23	fd_period_60_l	192	C0	11000000	RW	4	flicker period for 60Hz (L)
292	24	fd_period_50_h	0	00	00000000	RW	4	flicker period for 50Hz (H)
293	25	fd_period_50_m	67	43	01000011	RW	4	flicker period for 50Hz (M)
294	26	fd_period_50_l	74	4A	01001010	RW	4	flicker period for 50Hz (L)
295	27	fd_period_c_h	1	01	00000001	RW	4	flicker period for CASE C (H)
296	28	fd_period_c_m	147	93	10010011	RW	4	flicker period for CASE C (M)
297	29	fd_fheight_60_h	1	01	00000001	RW	4	flicker frameheight for 60Hz (H)
298	2A	fd_fheight_60_l	243	F3	11110011	RW	4	flicker frameheight for 60Hz (L)
299	2B	fd_fheight_50_h	1	01	00000001	RW	4	flicker frameheight for 50Hz (H)
300	2C	fd_fheight_50_l	243	F3	11110011	RW	4	flicker frameheight for 50Hz (L)

Default : 21h = 00h, 22h = 50h, 23h = C0h, 24h = 00h, 25h = 43h, 26h = 4Ah, 27h = 01h, 28h = 93h,
29h = 01h, 2Ah = F3h, 2Bh = 01h, 2Ch = F3h

Description :

FD Period A : 21h ~ 23h, Exposure period 60
FD Period B : 24h ~ 26h, Exposure period 50
FD Period B : 27h ~ 28h, Exposure period C
FD Frame Height A : 29h~2Ah, Frame Height for each state 60
FD Frame Height B : 2Bh~2Ch, Frame Height for each state 50

< Group B >

(304) ISP Function Control 0

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
304	30	isp_func_0	255	FF	11111111	RW	2	ISP control register 00

Default : 30h = FFh

Description :

register name : isp_function_control_00								
register #	bit#	name	default	255	default(h)	FF	default(b)	11111111
304(d) 30(h)	7	ccr_en	1	**Color Correction** '0' : Color correction disable '1' : Color correction enable (default)				
	6	Reserved	1					
	5	lpf_en	1	**Low Pass Filter** '0' : Disable. '1' : Enable. (default)				
	4	Reserved	1					
	3	Reserved	1					
	2	edge_en	1	**Edge Enhancement** '0' : Disable '1' : Enable (default)				
	1	x	1	x				
	0	x	1	x				

< Group B >

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(306) ISP Function Control 2

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
306	32	isp_func_2	1	01	00000001	RW	2	ISP control register 02

Default : 32h = 01h

Description :

register name : isp_function_control_02								
register #	bit#	name	default	1	default(h)	01	default(b)	00000001
306(d) 32(h)	7	sephia_en	0	**Sephia** '0' : Disable (default) '1' : Enable				
	6	sketch_en	0	**Sketch** '0' : Disable (default) '1' : Enable				
	5	emboss_en	0	**Emboss ing (reg_ae_ysel='0', interpolation Y selection)** '0' : Disable (default) '1' : Enable				
	4	emboss_se	0	**Embossing mode** '0' : Disable (default) '1' : Enable				
	3	reverse	0	**Reverse (reg_ae_ysel='3', Y601 selection)** '0' : Disable (default) '1' : Enable				
	2	x	0	x				
	1	x	0	x				
	0	lens_en	1	**Lens Shading Enable** '0' : Disable '1' : Enable (default)				

< Group B >

(307) ISP Function Control 3

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
307	33	isp_func_3	216	D8	11011000	RW	2	ISP control register 03

Default : 33h = D8h

Description :

register name : isp_function_control_03								
register #	bit#	name	default	216	default(h)	D8	default(b)	11011000
307(d) 33(h)	7	Reserved	1					
	6		1					
	5	Reserved	0					
	4		1					
	3	gm_en	1	Gamma Correction '0' : Disable '1' : Enable (default)				
	2	Reserved	0					
	1	x	0	x				
	0	x	0	x				

< Group B >

(308) I2C control 1

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
308	34	i2c_control_1	80	50	01010000	RW	4	I2C control register 01

Default : 34h = 50h

Description :

register name : i2c_control_1								
register #	bit#	name	default	80	default(h)	50	default(b)	01010000
308(d) 34(h)	7	Reserved	0					
	6		1					
	5		0					
	4		1					
	3	Reserved	0					
	2	clkoff	0	**Clock kill control register** '0' : Clock kill disable (default) '1' : Clock kill enable				
	1	stdby	0	**Register stanby mode** '0' : Off (default) '1' : On				
	0	rstb	0	**Register reset mode (Soft reset)** '0' : Disable (default) '1' : Enable				

< Group B >

(312) Format

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
312	38	format	0	00	00000000	RW	2	Output Format control register

Default : 38h = 00h

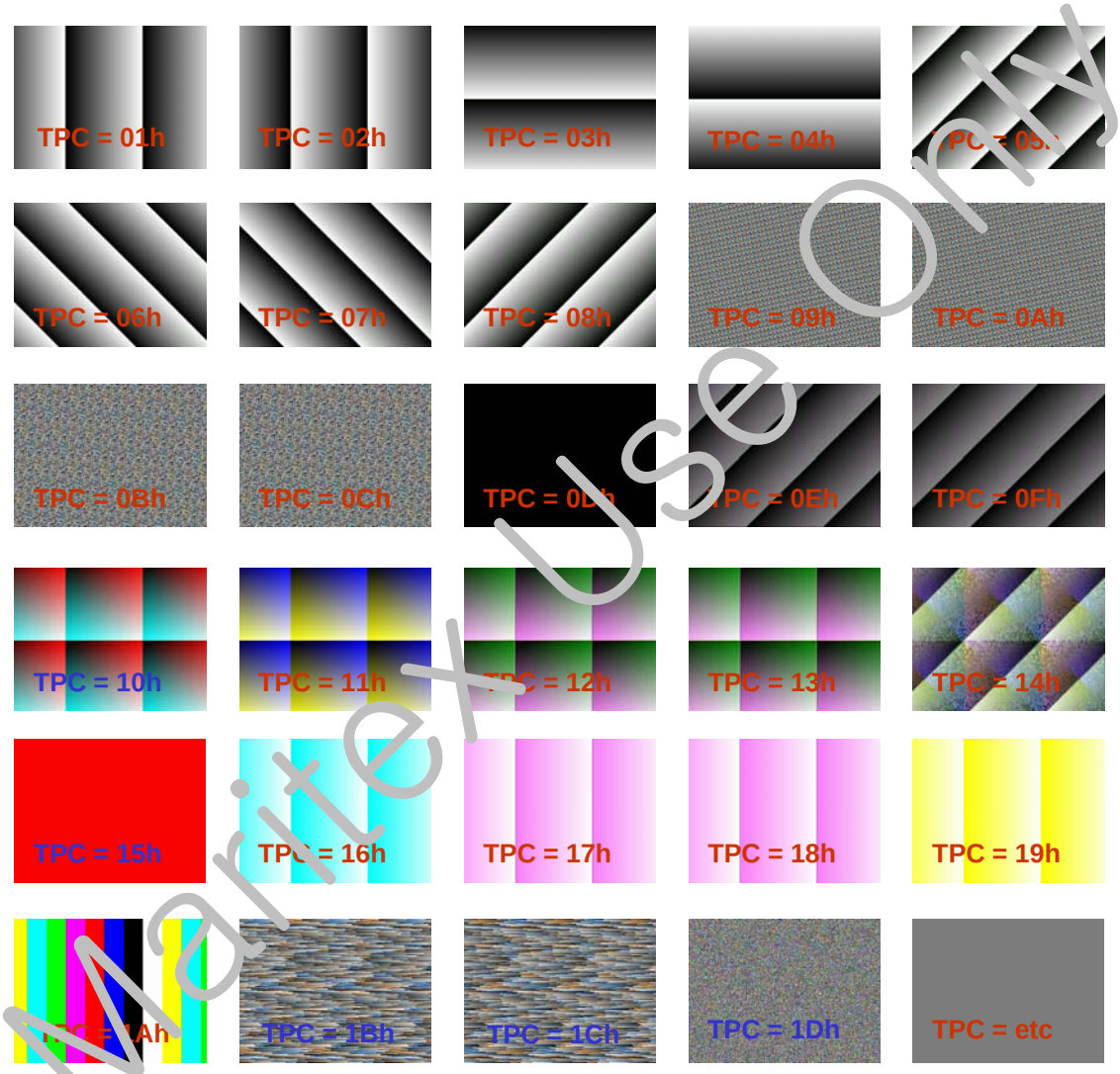
Description :

register name : format_control								
register #	bit#	name	default	0	default(h)	00	default(b)	00000000
312(d) 38(h)	7	format_control	0	00h : CB Y CR Y 01h : CR Y CB Y 02h : Y CB Y CR 03h : Y CR Y CB 04h : RGRG…GBGB 05h : GBGB...RGRG 06h : GRGR....BGBG 07h : BGBG...GRGR 08h : R5G6B5 09h :B5G6R5 0Ch : mono sensor 0Dh : YYY… 0Eh : R4G4B4				
	6		0					
	5		0					
	4		0					
	3		0					
	2		0					
	1		0					
	0		0					

< Group B >

(320) TP control 0

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
320	40	tp_control_0	0	00	00000000	RW	4	Test Pattern control register 00



< Group B >

(321-324) TP control 1 ~ 4

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
321	41	tp_control_1	255	FF	11111111	RW	4	Test Pattern control register 01
322	42	tp_control_2	255	FF	11111111	RW	4	Test Pattern control register 02
323	43	tp_control_3	255	FF	11111111	RW	4	Test Pattern control register 03
324	44	tp_control_4	255	FF	11111111	RW	4	Test Pattern control register 04

Default : 41h = FFh, 42h = FFh, 43h = FFh, 44h = FFh

Description :

Controls each color registers component of G1, R, B, G2

(328-329) FrameWidth

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
328	48	framewidth_h	3	03	00000011	RW	4	framewidth (H)
329	49	framewidth_l	31	1F	00011111	RW	4	framewidth (L)

Default : 48h = 03h, 49h = 1Fh Frame Width = 799d

Description :

FrameWidth is the number of columns to be counted during one line time. Column counter value is incremented by 1 until it reaches *FrameWidth*, then it is reset to 0. *FrameHeight* and *FrameWidth* determines the frame rate. Frame rate is given as follows.

Frame Rate = freq (PCLK) / ((*FrameHeight* +1) X (*FrameWidth*+1)) *(Bayer)*

Frame Rate = freq (PCLK) / ((*FrameHeight* +1) X (*FrameWidth*+1)) / 2 *(YCbCr)*

For example, If Pixel clock (PCLK) = 24 MHz, *FrameHeight* = 499d and *FrameWidth* = 799d. then, the frame rate is 30 fps for VGA Mode. If you double the *Frame Width* , you cut the frame rate by half.

< Group B >

(336-343) WindowX / Y

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
336	50	windowx1_h	0	00	00000000	RW	2	window X1 (H)
337	51	windowx1_l	7	07	00000111	RW	2	window X1 (L)
338	52	windowy1_h	0	00	00000000	RW	2	window Y1 (H)
339	53	windowy1_l	7	07	00000111	RW	2	window Y1 (L)
340	54	windowx2_h	2	02	00000010	RW	2	window X2 (H)
341	55	windowx2_l	134	86	10000110	RW	2	window X2 (L)
342	56	windowy2_h	1	01	00000001	RW	2	window Y2 (H)
343	57	windowy2_l	230	E6	11100110	RW	2	window Y2 (L)

Default : 50h = 00h, 51h = 07h, 52h = 00h, 53h = 07h, 54h = 02h, 55h = 86h, 56h = 01h, 57h = E6h

Description :

WindowX1 : 50h, 51h

WindowX2 : 54h, 55h

WindowY1 : 52h, 53h

WindowY2 : 56h, 57h

Window can be defined by 4 parameters : *WindowX1, WindowY1, WindowX2*, and *WindowY2.* Serial image data stream out pixel by pixel. Window specifies the area of pixels that we are interested in. Hsync signal indicates if the image data output is from a pixel that lies within the window area or not. Output data stream does not stop for pixels lying outside the window : just the Hsync signal is de-asserted.

The actual window position in the frame is given as

upper right corner = (*Window X1 + 1*, *Window Y1*)

lower left corner = (*Window X2*, *Window Y2 - 1*)

All the coordinates are with respect to the maximum window origin (0, 0) of <Fig. 3>. Window position and size are with respect to the full sampling mode. It is not necessary to change the window parameters when sampling mode is switched between one and another.

< Group B >

(352-355) VsyncStartrow / VsyncStoprow

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
352	60	vsyncstartrow_h	0	00	00000000	RW	4	Output Vsync Row Start (H)
353	61	vsyncstartrow_l	12	0C	00001100	RW	4	Output Vsync Row Start (L)
354	62	vsyncstoprow_h	1	01	00000001	RW	4	Output Vsync Row Stop (H)
355	63	vsyncstoprow_l	236	EC	11101100	RW	4	Output Vsync Row Stop (L)

Default : 60h = 00h, 61h = 0Ch, 62h = 01h, 63h = ECh

Description :

Output Vsync Row Start points : 60h, 61h

Output Vsync Row Stop points : 62h, 63h

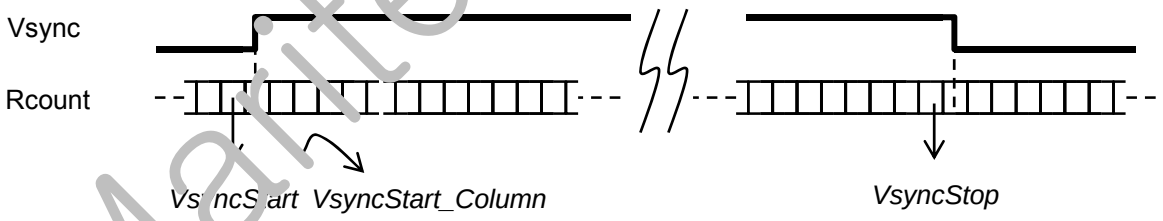
(356-357) VsyncColumn

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
356	64	vsynccolumn_h	0	00	00000000	RW	4	Output Vsync Column Start (H)
357	65	vsynccolumn_l	16	10	00010000	RW	4	Output Vsync Column Start (L)

Default : 64h = 00h, 65h = 10h

Description :

Output Vsync Column start points



< Group B >

(360) Sync control 0

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
360	68	sync_control_0	0	00	00000000	RW	2	Synchronization control register 00

Default : 68h = 00h

Description :

register name : sync_control_00								
register #	bit#	name	default	0	default(h)	00	default(b)	00000000
360(d) 68(h)	7	x	0	x				
	6	sync_drop[1:0]	0	Vsync Drop (VD), sync_drop[1] '0' : disable. (default) '1' : enable. Hsync Drop (HD), sync_drop[0] '0' : disable. (default) '1' : enable.				
	5		0					
	4	sync_pclkrate	0	pclk rate control				
	3		0					
	2		0					
	1		0					
	0		0					

< Group B >

(361) Sync control 1

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
361	69	sync_control_1	2	02	00000010	RW	4	Synchronization control register 01

Default : 69h = 02h

Description :

register name : sync_control_01								
register #	bit#	name	default	2	default(h)	02	default(b)	00000010
361(d) 69(h)	7	hiz	0	**Output Pad set to Hi Impedance (HiZ)** '0' : disable. (default) '1' : enable.				
	6	sync_vsyncPolarity	0	**Vsync Polarity Change** '0' : disable. (default) '1' : enable.				
	5	sync_hsyncAllLines	0	**Active High of Hsync All Lines** '0' : Disable. (default) '1' : Enable.				
	4	sync_hsyncPolarity	0	**Hsync Polarity Change** '0' : Disable. (default) '1' : Enable.				
	3	sync_pclkwindow	0	**PCLK Window** '0' : Disable. (default) '1' : Enable.				
	2	sync_pclkPolarity	0	**PCLK Polarity** '0' : Disable. (default) '1' : Enable.				
	1	stdby_level	1	**Stand by Level** '0' : Output level in stand by mode. (default) '1' : Hiz in stand by mode.				
	0	x	0	x				

< Group B >

(372-375) Sync CCIR

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
372	74	sync_ccirFF	255	FF	11111111	RW	4	CCIR data format FFh
373	75	sync_ccir00	0	00	00000000	RW	4	CCIR data format 00h
374	76	sync_ccir80	128	80	10000000	RW	4	CCIR data format 80h
375	77	sync_ccir10	16	10	00010000	RW	4	CCIR data format 10h

Default : 74h = FFh, 75h = 00h, 76h = 80h, 77h = 10h

Description :

CCIR data format FFh : 74h

CCIR data format 00h : 75h

CCIR data format 80h : 76h

CCIR data format 10h : 77h

(376-379) CCIR656 Sync Index Value

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
376	78	sync_blankSAV	182	B6	10110110	RW	4	blank SAV
377	79	sync_blankEAV	157	9D	10011101	RW	4	blank EAV
378	7A	sync_activSAV	171	AB	10101011	RW	4	active SAV
379	7B	sync_activEAV	128	80	10000000	RW	4	active EAV

Default : 78h = B6h, 79h = 9Dh, 7Ah = ABh, 7Bh = 80h

Description :

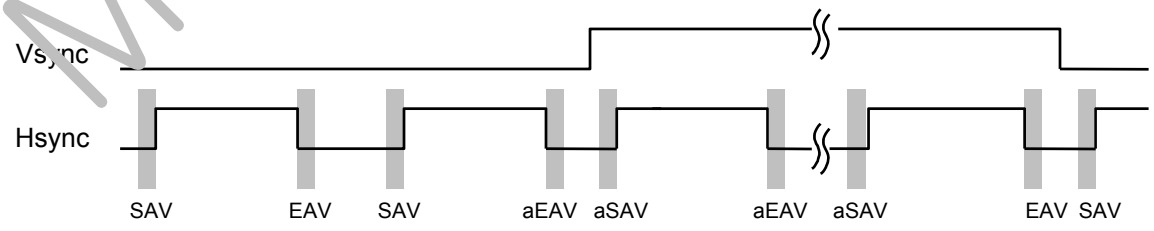
EAV and SAV signals are inserted for synchronization purposes.

BlankSAV : 78h, Blank Range Start of Video

BlankEAV : 79h, Blank Range End of Video

ActiveSAV : 7Ah, Active Range Start of Video

ActiveEAV : 7Bh, Active Range Stop of Video



EAV : blank EAV, SAV : blank SAV

aEAV : Active EAV, aSAV : Active SAV

< Group B >

(384-386) Scale

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
384	80	scale_x	32	20	00100000	RW	2	Horizontal scale factor (20h = x1)
385	81	scale_y	32	20	00100000	RW	2	Vertical scale factor (20h = x1)

Default : 80h = 20h, 81h = 20h

Description :

Scale X : 80h, Horizontal scale factor 20h = x1

Scale Y : 81h, Horizontal scale factor 20h = x1

(388-389) Sepia Color : Cb tone / Cr tone

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
388	84	sephia_cb	192	C0	11000000	RW	2	Cb sephia
389	85	sephia_cr	64	40	01000000	RW	2	Cr sephia

Default : 84h = C0h, 85h = 40h

Description :

fixed color (Cb / Cr) data when sepia or color vignette mode.

Cb Color tone : 84h

Cr Color tone : 85h

(392-395) Sketch Offset

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
392	88	sketchoffset1	32	20	00100000	RW	2	scatch offset 1
393	89	sketchoffset2	200	C8	11001000	RW	2	scatch offset 3
394	8A	sketchoffset3	16	10	00010000	RW	2	scatch offset 3
395	8B	sketchoffset4	128	80	10000000	RW	2	scatch offset 4

Default : 88h = 20h, 89h = C8h, 8Ah = 10h, 8Bh = 80h

Description :

Address	Name	Description
88h	*Sketch offset 1*	sketch offsets related to sketch effect color
89h	*Sketch offset 2*	
8Ah	*Sketch offset 3*	sketch offsets related to sketch effect edge
8Bh	*Sketch offset 4*	

(400) CS Max

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
400	90	cs_max	255	FF	11111111	RW	2	max. color

Default : 90h = FFh

Description :

Color Maximum (Clamping) data. : 0xFF = 128

color range in YCbCr : 16 ~ 240

=> cs_max = 112 = 0xE0

color range in YUV : 1 ~ 254 * 0, 255 : CCIR656 special number.

=> cs_max = 127 = 0xFE

(401-402) yContast / yBrightness

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
401	91	ycontrast	64	40	01000000	RW	2	Y contrast
402	92	ybrightness	1	01	00000001	RW	2	Brightness

Default : 91h = 40h, 92h = 01h

Description :

Luminous (Y) = Conversion Y x Contrast + Brightness

(403) Y Max

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
403	93	ymax	254	FE	11111110	RW	2	max. Y

Default : 93h = FEh,

Description :

Y Maximum (Clamping) data.

Y range in YCbCr : 16 ~ 235

=> Y Max = 235 = 0xEB

Y range in YUV : 1 ~ 254 * 0, 255 : CCIR656 special number.

=> Y Max = 254 = 0xFE

< Group B >

(412-415) Edge Enhancement

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
412	9C	edge_gain	36	24	00100100	RW	4	Edge Gain
413	9D	edge_th	16	10	00010000	RW	4	Edge Threshold

Default : 9Ch = 36h

Description :

Edge Gain : 9Ch, (0x04 = x1)

Edge Threshold : 9Dh, Edge enhancement threshold.

(420-428) Color Correction

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
420	A4	cc11	56	38	00111000	RW	4	Color correction matrix (11)
421	A5	cc12	165	A5	10100101	RW	4	Color correction matrix (12)
422	A6	cc13	13	0D	00001101	RW	4	Color correction matrix (13)
423	A7	cc21	147	93	10010011	RW	4	Color correction matrix (21)
424	A8	cc22	45	2D	00101101	RW	4	Color correction matrix (22)
425	A9	cc23	6	06	00000110	RW	4	Color correction matrix (23)
426	AA	cc31	131	83	10000011	RW	4	Color correction matrix (31)
427	AB	cc32	170	AA	10101010	RW	4	Color correction matrix (32)
428	AC	cc33	77	4D	01001101	RW	4	Color correction matrix (33)

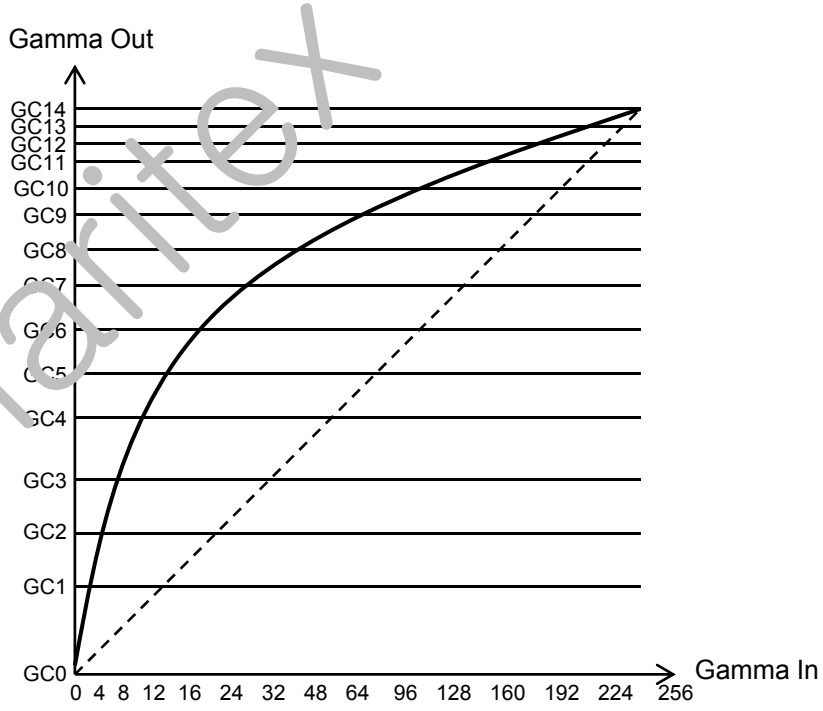
(432-446) Gamma Coefficient

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
432	B0	gm_y0	0	00	00000000	RW	4	Gamma Y0
433	B1	gm_y1	10	0A	00001010	RW	4	Gamma Y1
434	B2	gm_y2	23	17	00010111	RW	4	Gamma Y2
435	B3	gm_y3	36	24	00100100	RW	4	Gamma Y3
436	B4	gm_y4	47	2F	00101111	RW	4	Gamma Y4
437	B5	gm_y5	65	41	01000001	RW	4	Gamma Y5
438	B6	gm_y6	80	50	01010000	RW	4	Gamma Y6
439	B7	gm_y7	103	67	01100111	RW	4	Gamma Y7
440	B8	gm_y8	119	77	01110111	RW	4	Gamma Y8
441	B9	gm_y9	149	95	10010101	RW	4	Gamma Y9
442	BA	gm_y10	174	AE	10101110	RW	4	Gamma Y10
443	BB	gm_y11	197	C5	11000101	RW	4	Gamma Y11
444	BC	gm_y12	218	DA	11011010	RW	4	Gamma Y12
445	BD	gm_y13	237	ED	11101101	RW	4	Gamma Y13
446	BE	gm_y14	255	FF	11111111	RW	4	Gamma Y14

Default : 00h, 0Ah, 17h, 24h, 2Fh, 41h, 50h, 67h, 77h, 95h, AEh, C5h, DAh, EDh, FFh

Description :

Gamma Correction is applied to RGB signal which ranges from 0 to 255 to compensate non-linear characteristics of display brightness vs input brightness.



GC : Gamma coefficient

< Group B >

(460-474) Lens Shading Compensation

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
460	CC	lens_gainr	0	00	00000000	RW	4	Red lens gain
461	CD	lens_gaing	0	00	00000000	RW	4	Green lens gain
463	CF	lens_gainb	0	00	00000000	RW	4	Blue lens gain
464	D0	lens_coffset_h	6	06	00000110	RW	4	lens column offset (H)
465	D1	lens_coffset_l	95	5F	01011111	RW	4	lens column offset (L)
466	D2	lens_rx	0	00	00000000	RW	4	red lens x origin
467	D3	lens_ry	0	00	00000000	RW	4	red lens y origin
468	D4	lens_gx	0	00	00000000	RW	4	green lens x origin
469	D5	lens_gy	0	00	00000000	RW	4	green lens y origin
472	D8	lens_bx	0	00	00000000	RW	4	blue lens x origin
473	D9	lens_by	0	00	00000000	RW	4	blue lens y origin
474	DA	lens_scale	81	51	01010001	RW	4	East/West/South/North lens scale factor

Default : CCh = 00h, CDh = 00h, CFh = 00h, D0h = 06h, D1h = 5Fh, D2h = 00h, D3h = 00h
D4h = 00h, D5h = 00h, D8h = 00h, D9h = 00h, DAh = 51h

Description :

Lens Gain R : CCh, Red Lens Shading Gain. 0x20 = x 1 gain.
Lens Gain G : CDh, Green Lens Shading Gain. 0x20 = x 1 gain.
Lens Gain B : CFh, Blue Lens Shading Gain. 0x20 = x 1 gain.
Lens Column Offset : D0h, D1h, Lens Shading Column Offset
Lens Red XY Origin : D2h, D3h, Window center origin Red XY value for Lens shading compensation
Lens Green XY Origin : D4h, D5h, Window center origin Green XY value for Lens shading compensation
Lens Blue XY Origin : D8h, D9h, Window center origin Blue XY value for Lens shading compensation
Lens Scale : DAh, East/West/South/North lens scale factor

< Group B >

(516) Auto control 1

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
516	04	auto_control_1	152	98	10011000	RW	2	auto control register 01

Default : 04h = 98h

Description :

register name : auto_control_01								
register #	bit#	name	default	152	default(h)	98	default(b)	10011000
516(d) 04(h)	7	Reserved	1					
	6	Reserved	0					
	5	Reserved	0					
	4	Reserved	1					
	3	Reserved	1					
	2	Auto White Balance Register Update	0	**Auto White Balance Register update** '0' : Update by internal function (default) '1' : Update by external interface				
	1	Auto Exposure Register Update	0	**Auto Exposure Register update** 00b : Update by Internal function. (default) 01b : Update by Exposure register 10b : Update by External_Inttime & Linear Gain 11b : Update by Inttime & Globalgain register				
	0		0					

< Group C >

(517) Auto control 2

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
517	05	auto_control_2	13	0D	00001101	RW	2	auto control register 02

Default : 05h = 0Dh

Description :

register name : auto_control_02								
register #	bit#	name	default	13	default(h)	0D	default(b)	00001101
517(d) 05(h)	7	x	0	x				
	6	x	0	x				
	5	Reserved	0					
	4	Reserved	0					
	3	Reserved	1					
	2	Digital gain Update	1	Digital gain Update '0' : Update by user '1' : Update by auto (default)				
	1	Reserved	0					
	0	Reserved	1					

< Group C >

(528-535) AE Window

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
528	10	ae_winx_h	0	00	00000000	RW	4	AE window X (H)
529	11	ae_winx_l	37	25	00100101	RW	4	AE window X (L)
530	12	ae_winy_h	0	00	00000000	RW	4	AE window Y (H)
531	13	ae_winy_l	28	1C	00011100	RW	4	AE window Y (L)
532	14	ae_width_h	2	02	00000010	RW	4	AE window Width (H)
533	15	ae_width_l	96	60	01100000	RW	4	AE window Width (L)
534	16	ae_height_h	1	01	00000001	RW	4	AE window Height (H)
535	17	ae_height_l	190	BE	10111110	RW	4	AE window Height (L)

Default : 10h = 00h, 11h = 25h, 12h = 00h, 13h = 1Ch, 14h = 02h, 15h = 60h, 16h = 01h, 17h = BEh

Description :

AE window X : 10h, 11h

AE window Y : 12h, 13h

AE window Width : 14h, 15h

AE window Height : 16h, 17h

(536-543) AE Center Window

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
536	18	ae_cwinx_h	0	00	00000000	RW	4	AE Center window X (H)
537	19	ae_cwinx_l	229	E5	11100101	RW	4	AE Center window X (L)
538	1A	ae_cwiny_h	0	00	00000000	RW	4	AE Center window Y (H)
539	1B	ae_cwiny_l	135	87	10000111	RW	4	AE Center window Y (L)
540	1C	ae_cwidth_h	0	00	00000000	RW	4	AE Center window Width (H)
541	1D	ae_cwidth_l	160	A0	10100000	RW	4	AE Center window Width (L)
542	1E	ae_cheight_h	0	00	00000000	RW	4	AE Center window Height (H)
543	1F	ae_cheight_l	160	A0	10100000	RW	4	AE Center window Height (L)

Default : 18h = 00h, 19h = E5h, 1Ah = 00h, 1Bh = 87h, 1Ch = 00h, 1Dh = A0h, 1Fh = A0h

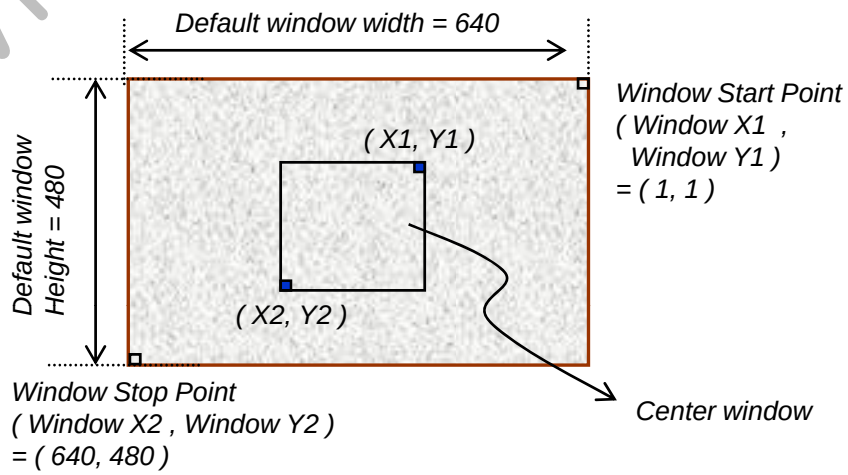
Description :

AE Center window X : 18h, 19h

AE Center window Y : 1Ah, 1Bh

AE Center Window Width : 1Ch, 1Dh

AE Center Window Height : 1Eh, 1Fh



(548-550) External Integration Time

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
548	24	ext_inttime_h	0	00	00000000	RW	2	External Integration Time (H)
549	25	ext_inttime_m	128	80	10000000	RW	2	External Integration Time (M)
550	26	ext_inttime_l	0	00	00000000	RW	2	External Integration Time (L)

Default : 24h = 00h, 25h = 80h, 26h = 00h

Description :

Manual external integration time

(552-553) External linear Globalgain

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
552	28	ext_glbg_h	1	01	00000001	RW	2	External Globalgain (H)
553	29	ext_glbg_l	0	00	00000000	RW	2	External Globalgain (L)

Default : 28h = 01h, 29h = 00h

Description :

Manual external Globalgain.

(556-559) Exposure Register

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
556	2C	exposure_t	0	00	00000000	RW	2	Current Exposure (T)
557	2D	exposure_h	0	00	00000000	RW	2	Current Exposure (H)
558	2E	exposure_m	128	80	10000000	RW	2	Current Exposure (M)
559	2F	exposure_l	0	00	00000000	RW	2	Current Exposure (L)

Default : 2Ch (Exposure Register - T) = 00h

2Dh (Exposure Register - H) = 00h

2Eh (Exposure Register - M) = 80h

2Fh (Exposure Register - L) = 00h

Description :

Exposure[31:0] : "*Exposure*" register means abstract exposure level of sensor. Larger the value of *Exposure*, effectively longer exposure time. LSB of *Exposure* corresponds to 1/256 line exposure time. User can write *Exposure* register only when AE function is disabled.

(564-567) Middle / Maximum FrameHeight

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
564	34	midfrmheight_h	3	03	00000011	RW	4	Middle FrameHeight (H)
565	35	midfrmheight_l	230	E6	11100110	RW	4	Middle FrameHeight (L)
566	36	maxfrmheight_h	7	07	00000111	RW	4	Max FrameHeight (H)
567	37	maxfrmheight_l	204	CC	11001100	RW	4	Max FrameHeight (L)

Default : 34h = 03h, 35h = E6h, 36h = 07h, 37h = CCh

Description :

FrameHeight middle value : 34h, 35h

FrameHeight maximum value : 36h, 37h

(572-582) Middle / Maximum / Minimum Exposure

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
572	3C	midexp_t	0	00	00000000	RW	4	Middle Exposure (T)
573	3D	midexp_h	31	1F	00011111	RW	4	Middle Exposure (H)
574	3E	midexp_m	48	30	00110000	RW	4	Middle Exposure (M)
576	40	maxexp_t	0	00	00000000	RW	4	Max Exposure (T)
577	41	maxexp_h	62	3E	00111110	RW	4	Max Exposure (H)
578	42	maxexp_m	96	60	01100000	RW	4	Max Exposure (M)
580	44	minexp_h	0	00	00000000	RW	4	Min Exposure (H)
581	45	minexp_m	0	00	00000000	RW	4	Min Exposure (M)
582	46	minexp_l	12	0C	00001100	RW	4	Min Exposure (L)

Default : 3Ch = 00h, 3Dh = 1Fh, 40h = 00h, 41h = 3Eh, 42h = 60h, 44h = 00h, 45h = 00h, 46h = 0Ch

Description :

Exposure middle value : 3Ch ~ 3Eh

Middle exposure time is decided by these registers.

Exposure maximum value : 40h ~ 42h

Maximum exposure time is decided by these registers. If user set these registers larger than default frameheight, frame rate is automatically varied.

Exposure minimum value : 44h ~ 46h

Under auto exposure mode, minimum exposure time of a pixel is set by MinExpTime register. LSB of MinExpTime corresponds to time for reading 1 / 64 line in each frame.

< Group C >

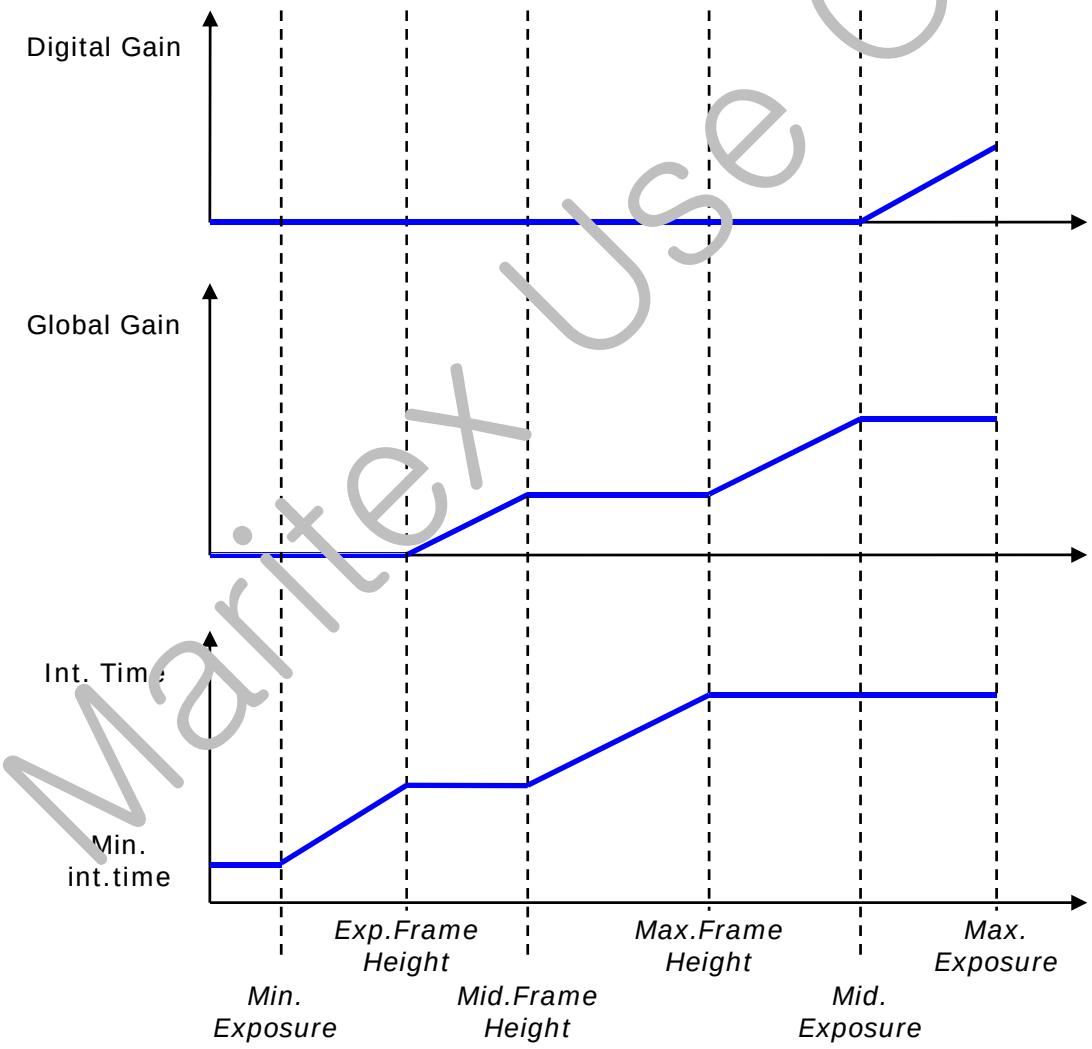
(584-585) Exposure FrameHeight

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
584	48	expFrmH_H	1	01	00000001	RW	4	Reference Exposure FrameHeight (H)
585	49	expFrmH_L	243	F3	11110011	RW	4	Reference Exposure FrameHeight (L)

Default : 48h = 01h, 49h = F3h

Description :

exposure FrameHeight value.



< Group C >

(588-590) Integration Time

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
588	4C	inttime_H	0	00	00000000	RW	2	Integration Time (H)
589	4D	inttime_M	128	80	100000000	RW	2	Integration Time (M)
590	4E	inttime_L	0	00	00000000	RW	2	Integration Time (L)

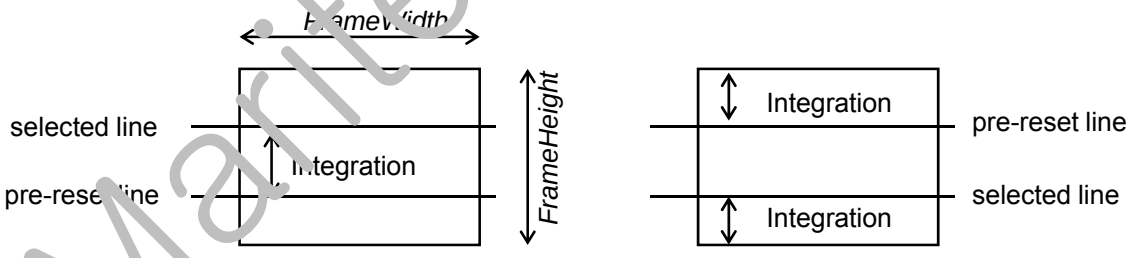
Default : 4Ch = 00h, 4Dh = 80h, 4Eh = 00h

Description :

There are 3 bytes of registers to control the photo-charge accumulation interval for each pixel. 4Ch and 4Dh registers indicate how many line times the integration will continue until they are all reset. 4Eh register further sub-divides one line time into 256 smaller intervals. Total integration time is the sum of the integral multiple and fractional parts of one line time.

As the row counter value is incremented from 0 to *FrameHeight*, each line relevant to the row count is selected and all pixel data of that line is read out all at once. The read- out operation involves pixel reset pulses, so all pixels that are selected and read out are reset to initial states.

To control exposure time, there runs another counter to select and reset a line other than the one that is selected to be read out. The space between the two lines is equal to the number of integration lines. There are two possible situations concerning the position of selected line and reset line. The 1st case is where the pre-reset counter runs ahead of read-out counter. And the other case Is just the reverse of the 1st one. The number of integration lines is different for the two cases as is shown in the left figures. Since the basic unit of integration time for PO60300K is 1/ 256 line time, it is easy to implement Auto Exposure algorithms without worrying about strong light environment where the image may change abruptly in brightness or it may even blink.



Case 1. Reset line preceding select line Case 2. Select line preceding reset line

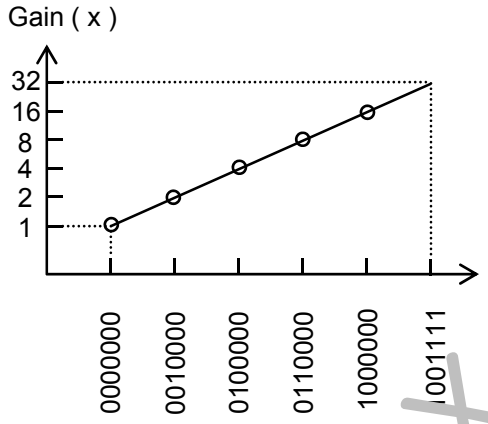
(592) Globalgain

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
592	50	globalgain	0	00	00000000	RW	2	Globalgain

Default : 50h = 00h

Description :

GlobalGain has effect on all of R, G, and B pixel outputs. Raw R, G, B data are amplified by a common factor of *GlobalGain*. The relation between *GlobalGain* and amplification factor is shown in the picture below.



Maximum value of *GlobalGain* is 1001111. Gain factors for *GlobalGain* larger than or equal to 1010000 are not defined.

(593) Digital Gain

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
593	51	digitalgain	64	40	01000000	RW	2	Digital Gain

Default : 51h = 40h

Description :

Digital Gain

(596) AE center Weight

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
596	54	ae_c_weight	3	03	00000011	RW	2	AE Center Weight

Default : 54h = 03h,

Description :

Center window weight (CW) for back light compensation.

$$\text{Bright mean} = \frac{(Yc \times CW) + (Yp \times (16 - CW))}{16}$$

Yc : Center window Y mean

Yp : Periphery Y mean

(597-598) Auto Exposure Speed

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
597	55	ae_up_speed	8	08	00001000	RW	2	AE upside Speed
598	56	ae_down_speed	12	0C	00001100	RW	2	AE downside Speed

Default : 55h = 08h, 56h = 0Ch

Description :

AE up Speed : AE speed applied when exposure is decreasing.

AE down Speed : AE speed applied when exposure is increasing

(599) Auto Exposure Lock

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
599	57	ae_lock	2	02	00000010	RW	2	AE lock range

Default : 57h = 02h,

Description :

set margin of Auto Exposure function.

(618-619) Y mean

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
618	6A	ymean_h	0	00	00000000	RO	4	Ymean (H)
619	6B	ymean_l	128	80	10000000	RO	4	Ymean (L)

Default : 6Ah = 00h, 6Bh = 80h

Description :

Brightness Mean

(623) User wYt

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
623	6F	user_wyt	128	80	10000000	RW	2	user Y target

Default : 6Fh = 80h

Description :

User weight Y target offset

< Group C >

(644-645) AWB R/B ratio

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
644	84	awb_rgratio	128	80	10000000	RW	4	AWB Red/Green Ratio
645	85	awb_bgratio	128	80	10000000	RW	4	AWB Blue/Green Ratio

Default : 84h (AWB R ratio) = 80h

85h (AWB B ratio) = 80h

Description :

Red mean target = Evaluate Green mean x R ratio / 128

Blue mean target = Evaluate Green mean x B ratio / 128

(646) Auto White Balance Lock

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
646	86	awb_lock	2	02	00000010	RW	4	AWB lock range

Default : 86h = 02h,

Description :

Set margin of Auto White Balance functions

(647) Auto White Balance Speed

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
647	87	awb_speed	8	08	00000000	RW	4	AWB speed (target AWB step numbers : 16 steps need to approach at One Time)

Default : 87h = 08h,

Description :

Auto White Balance evaluate speed.

(672- 675) White Balance RGB gain MIN/MAX

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
672	A0	wb_rgain_min	0	00	00000000	RW	2	min Red gain for white balance
673	A1	wb_rgain_max	255	FF	11111111	RW	2	max Red gain for white balance
674	A2	wb_bgain_min	0	00	00000000	RW	2	min Blue gain for white balance
675	A3	wb_bgain_max	255	FF	11111111	RW	2	max Blue gain for white balance

Default : A0h (Red_in_min) = 00h

A1h (Red_in_max) = FFh

A2h (Blue_in_min) = 00h

A3h (Blue_in_max) = FFh

Description :

RGB input data range for AWB compute

< Group C >

(676-678) White Balance R/G/B gain

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
676	A4	wb_rgain	64	40	01000000	RW	2	Red gain for white balance
677	A5	wb_ggain	64	40	01000000	RW	2	Green gain for white balance
678	A6	wb_bgain	64	40	01000000	RW	2	Blue gain for white balance

Default : A4h = 40h, A5h = 40h, A6h = 40h

Description :

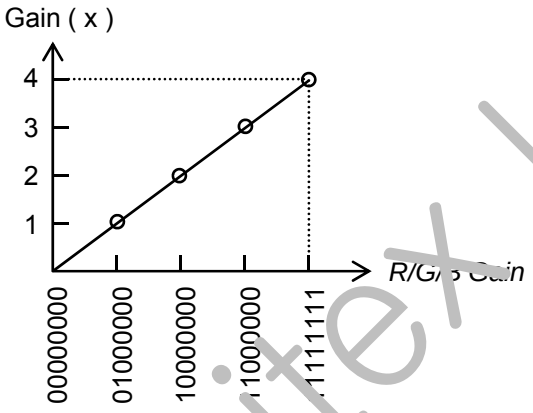
White Balance Red gain : A4h

RedGain is the multiplication factor for red pixel output. Total gain factor for red pixels is (gain from *GlobalGain*) * (gain from *RedGain*).

White Balance Green gain : A5h

G1/G2 pixels are those green pixels whose nearest neighbors are red pixels or blue pixels.

White Balance Blue gain : A6h



R / G / B gain can be used for white balance control. Bit7 of *R/G/B Gain* is weighted by 2, bit6 by 1 and the other consecutive bits are weighted by 1/2, 1/4, 1/8, … respectively. That is, *R/G/B gain* is a binary number with decimal point between bit6 and bit5.

(692) User color saturation

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
692	B4	user_cs	32	20	00100000	RW	2	User color saturation offset

Default : B4h = 20h

Description :

CS = CS x user_cs

(997-999) Average R/G/B

#		register name	default value			type	stage	Description
dec	hex		dec	hex	bin			
997	E5	avg_r	0	00		RO	0	Red average
998	E6	avg_g	0	00		RO	0	Green average
999	E7	avg_b	0	00		RO	0	Blue average

Description :

Monitoring R/G/B Average

< Group C >

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Electrical Characteristics

Absolute Maximum Ratings *

HVDD,AVDD Supply Voltage ---------- -0.3V to 4.5V
DVDD Supply Voltage ---------- -0.3V to 2.5V
DC Voltage at any input pin ---------- -0.3V to HVDD+0.3V
DC Voltage at any output pin ---------- -0.3V to HVDD+0.3V
Storage Temperature ---------- -40°C to + 125 °C

Table 4. DC Characteristics

Symbol	Descriptions	Min	Typ	Max	Unit
V_{DDD}	Digital VDD voltage relative to GND(DGND) level.	1.35	1.5 1.8	1.98	V
V_{DDA}	Analog voltage relative to GND(AGND) level.	2.52	2.8	3.08	V
HV_{DD}	High VDD(HVDD) voltage relative to GND(DGND) level	1.35	1.5 1.8 2.8 3.3	3.63	V
I_{DDD}	Supply current at 30 fps. Currents are programmable through 2-wire serial interface.				
	DVDD=1.5V(1.8V)		7.0(9.2)		mA
	AVDD=2.8V		16.0		mA
	HVDD=3.3V		3.5		mA
I_{DDS}	Standby supply current@ DVDD=1.5V(1.8V)/AVDD=2.8V/HVDD=3.3V		14.6(15.6)		uA
V_{IL1}	Input voltage LOW level			0.2*HVDD	V
V_{IH1}	Input voltage HIGH level	0.8*HVDD			V
V_{IL2}	Input voltage LOW level for rClk, rData.			0.2*HVDD	V
V_{IH2}	Input voltage HIGH level for rClk, rData	0.8*HVDD			V
C_{IN}	Input pin capacitance			10	pF
V_{OL1}	Output Voltage LOW			0.1*HVDD	V
V_{OH1}	Output Voltage HIGH	0.9*HVDD			V
V_{OL2}	Output Voltage LOW level for rClk, rData.			0.2	V
V_{OH2}	Output Voltage HIGH level for rData.	HVDD-0.2			V
I_{IN}	Input leakage current		0.005	1	uA
I_{OT}	Output leakage current		0.005	1	uA

* Excessive stresses may cause permanent damage to the device.

Table5. AC Characteristics (In case of HVDD=2.8V)

Cload=16pF

Symbol	Descriptions	Min	Typ	Max	Unit
f_{MCLK}	Master clock Frequency		24		MHz
duty	Master clock duty cycle		50		%
t1	Master clock rise/fall time		5		ns
t2	PCLK rise/fall time		9.67		ns
t3	PCLK rising edge to HSYNC		20.33		ns
t4	PCLK rising edge to digital output		21.3		ns
t5	MCLK rising edge to PCLK rising edge		15.2		ns
t6	PCLK rising edge to VSYNC		21		ns

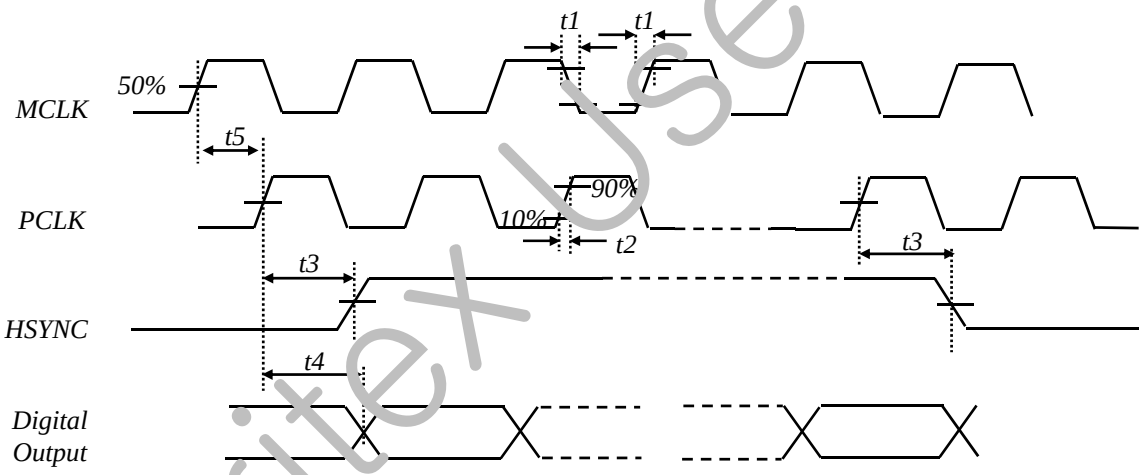


Fig. 12 Timing diagram of Clock, Data, and HSync

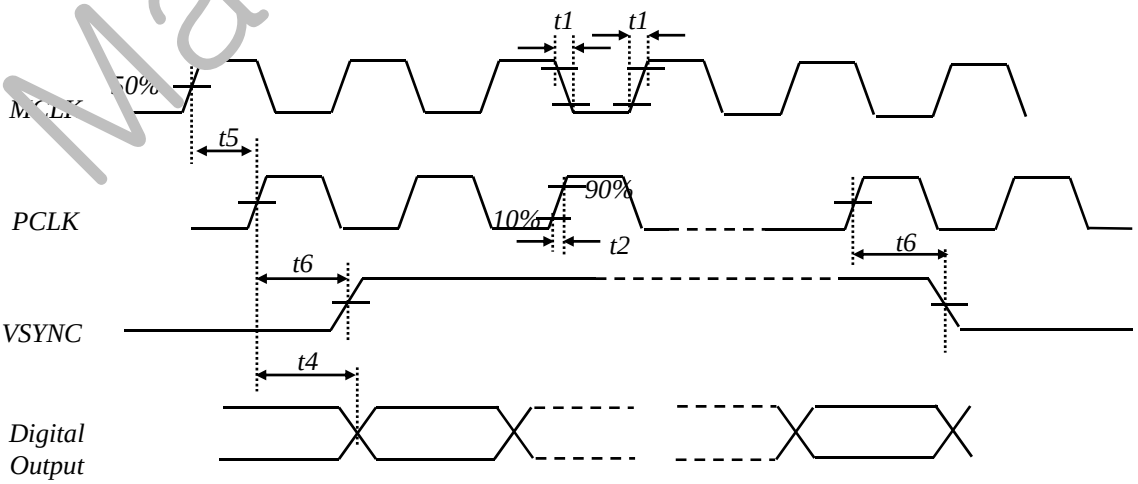


Fig. 13 Timing diagram of Clock, Data, and VSync

Table 6. Electro-Optical Characteristics (@ 60degree)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Sens	Sensitivity	1)		*1.46*		V/lux.sec
Vsat	Saturation Level	2)		1.2		V
Vdrk	Dark Signal	3)		*28.6*		mV/sec
DR	Dynamic range	4)		*50.3*		dB

Notes :

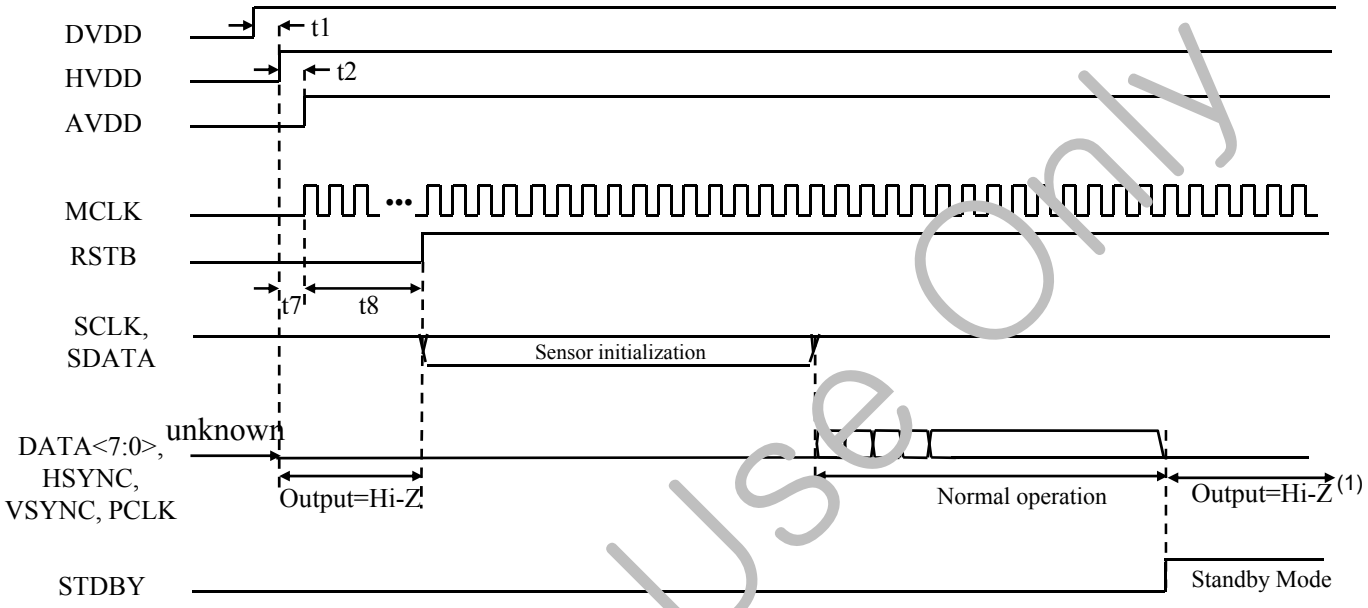
1) This value comes from the wafer test. The calculation sequence is as follows.
   (1) read the saturation level from evaluation pad
   (2) calculate One LSB.
   (3) Read output signal of Green pixels under illumination with output signal equal to 50% of saturation signal.
   (4) Read the Luminance and Integration Time when 50% of saturation signal.
   (5) Calculate the sensitivity using (1)~(4)
   = (the signal of Green pixels * one LSB) / (luminance * integration time)

2) Read the value of evaluation pad when all pixels are saturated in condition

3) Measured at the zero illumination
   (1) read the dark signal average of all pixels for minimum integration time
   (2) read the dark signal average of all pixels for maximum integration time
   (3) [Dark signal @ maximum integration time] – [Dark signal @ minimum integration time]
   (4) convert to mV/sec unit

4) For frame rate=7.5 fps
   20*Log [Saturation Signal /Dark signal] [dB]

Power-On Sequence



(1) To make output Hi-Z state in power-down mode, set Reg.B-69h[1] to '1' before starting power-down mode

Power-Off Sequence

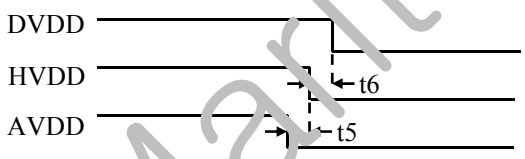


Table Recommended Power-On/Off sequence

Symbol	Descriptions	Min	Typ	Max	Unit
t1	From DVDD rising to HVDD rising	0			ns
t2	From HVDD rising to AVDD rising	0			ns
t5	From AVDD falling to HVDD falling	0			ns
t6	From HVDD falling to DVDD falling	0			ns
t7	From HVDD rising to initial mclk rising	0			ns
t8	Minimum reset time	16 x MCLK period			

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

▶ Application Note

- Revision Number

Reg. Addr. (Hex)	Read Value (Hex)	Register Name	Descriptions
02	01	*RevNum*	Revision Number of PO6030K

- Register Groups

PO6030K has four Register Groups (Register A, B, C & D). So, you must be careful and make sure that the correct register group is firstly selected before you access registers .

Register Group can be selected by Setting Reg.03h.

Address (Hex)	Write Value (Hex)	Register Name	Descriptions
03	**00**	*RegisterSet*	Select Register Group A
	01		Select Register Group B
	02		Select Register Group C
	03		Select Register Group D

Ex) When you want to write (or read) the value to Reg.04h in the Register Group A,

=> 1st > Write 0x00 to Reg.03h

2nd >Write (or Read) the value to Reg.04h

When you want to write (or read) the value to Reg.04h and 05h in the Register Group B,

=> 1st > Write 0x01 to Reg.03h

2nd >Write (or Read) the values of Reg.04h and 05h

< Notation >

We will use the following notation in this application note to separate registers according to the Register Group which they belong to.

Register Group	Notation	Example
A	A-	A-10 : Reg.10h in Register Group A
B	B-	B-4C : Reg.4Ch in Register Group B
C	C-	
D	D-	

- Image Output Size

PO6030K support VGA, QVGA, QQVGA, CIF, QCIF

- VGA mode (640x480)

Address (Hex)	Setting value (Hex)	Register Name	Default Vale (Hex)	Description
B-51	**07**	*WindowX1 (L)*	07	Window Position
B-53	**07**	*WindowY1 (L)*	07	
B-54	**02**	*WindowX2 (H)*	02	
B-55	**86**	*WindowX2 (L)*	86	
B-56	**01**	*WindowY2 (H)*	01	
B-57	**E6**	*WindowY2 (L)*	E6	
B-61	**0C**	*VsyncStartRow(L)*	0C	
B-63	**EC**	*VsyncStopRow(L)*	EC	
B-80	**20**	*ScaleX*	20	
B-81	**20**	*ScaleY*	20	
B-82	**01**	*Reserved*	04	
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	
C-11	**25**	*AEWinX (L)*	25	AE Window Position
C-13	**1C**	*AEWinY (L)*	1C	
C-14	**02**	*AEWinWidth (H)*	02	
C-15	**60**	*AEWinWidth (L)*	60	
C-16	**01**	*AEWinHeight (H)*	01	
C-17	**BE**	*AEWinHeight (L)*	BE	
C-19	**E5**	*AECenterWinX (L)*	E5	AE Center Window Position
C-1B	**87**	*AECenterWinY (L)*	87	
C-1D	**A0**	*AECenterWidth (L)*	A0	
C-1F	**A0**	*AECenterHeight (L)*	A0	

- QVGA mode (320x240)

Address (Hex)	Setting value (Hex)	Register Name	Default Vale (Hex)	Description
B-51	**04**	*WindowX1 (L)*	07	Window Position
B-53	**04**	*WindowY1 (L)*	07	
B-54	**01**	*WindowX2 (H)*	02	
B-55	**43**	*WindowX2 (L)*	86	
B-56	**00**	*WindowY2 (H)*	01	
B-57	**F3**	*WindowY2 (L)*	E6	
B-61	**0C**	*VsyncStartRow(L)*	0C	
B-63	**EC**	*VsyncStopRow(L)*	EC	
B-80	**40**	*ScaleX*	20	
B-81	**40**	*ScaleY*	20	
B-82	**01**	*Reserved*	04	
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	
C-11	**12**	*AEWinX (H)*	25	AE Window Position
C-13	**0E**	*AEWinY (L)*	1C	
C-14	**01**	*AEWinWidth (H)*	02	
C-15	**60**	*AEWinWidth (L)*	60	
C-16	**00**	*AEWinHeight (H)*	01	
C-17	**BE**	*AEWinHeight (L)*	BE	
C-19	**72**	*AECenterWinX (L)*	E5	AE Center Window Position
C-1B	**43**	*AECenterWinY (L)*	87	
C-1D	**50**	*AECenterWidth (L)*	A0	
C-1F	**50**	*AECenterHeight (L)*	A0	

- QQVGA mode (160x120)

Address (Hex)	Setting value (Hex)	Register Name	Default Vale (Hex)	Description
B-51	**03**	*WindowX1 (L)*	07	Window Position
B-53	**02**	*WindowY1 (L)*	07	
B-54	**00**	*WindowX2 (H)*	02	
B-55	**A2**	*WindowX2 (L)*	86	
B-56	**00**	*WindowY2 (H)*	01	
B-57	**79**	*WindowY2 (L)*	E6	
B-61	**0C**	*VsyncStartRow(L)*	0C	
B-63	**EC**	*VsyncStopRow(L)*	EC	
B-80	**80**	*ScaleX*	20	
B-81	**80**	*ScaleY*	20	
B-82	**01**	*Reserved*	04	
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	
C-11	**09**	*AEWinX (H)*	25	AE Window Position
C-13	**07**	*AEWinY (L)*	1C	
C-14	**00**	*AEWinWidth (H)*	02	
C-15	**80**	*AEWinWidth (L)*	60	
C-16	**00**	*AEWinHeight (H)*	01	
C-17	**6F**	*AEWinHeight (L)*	BE	
C-19	**39**	*AECenterWinX (L)*	E5	AE Center Window Position
C-1B	**21**	*AECenterWinY (L)*	87	
C-1D	**28**	*AECenterWidth (L)*	A0	
C-1F	**28**	*AECenterHeight (L)*	A0	

- CIF mode (352x288)

Address (Hex)	Setting value (Hex)	Register Name	Default Vale (Hex)	Description
B-51	**16**	*WindowX1 (L)*	07	Window Position
B-53	**05**	*WindowY1 (L)*	07	
B-54	**01**	*WindowX2 (H)*	02	
B-55	**75**	*WindowX2 (L)*	86	
B-56	**01**	*WindowY2 (H)*	01	
B-57	**24**	*WindowY2 (L)*	E6	
B-61	**0E**	*VsyncStartRow(L)*	0C	
B-63	**EB**	*VsyncStopRow(L)*	E	
B-80	**35**	*ScaleX*	2	
B-81	**35**	*ScaleY*	20	
B-82	**01**	*Reserved*	04	
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	
C-11	**16**	*AEWinX (L)*	25	AE Window Position
C-13	**10**	*AEWinY (L)*	1C	
C-14	**01**	*AEWinWidth (H)*	02	
C-15	**6F**	*AEWinWidth (L)*	60	
C-16	**01**	*AEWinHeight (H)*	01	
C-17	**0B**	*AEWinHeight (L)*	BE	
C-19	**8A**	*AECenterWinX (L)*	E5	AE Center Window Position
C-1B	**51**	*AECenterWinY (L)*	87	
C-1D	**60**	*AECenterWidth (L)*	A0	
C-1F	**60**	*AECenterHeight (L)*	A0	

- QCIF mode (176x144)

Address (Hex)	Setting value (Hex)	Register Name	Default Vale (Hex)	Description
B-51	**0C**	*WindowX1 (L)*	07	Window Position
B-53	**03**	*WindowY1 (L)*	07	
B-54	**00**	*WindowX2 (H)*	02	
B-55	**BB**	*WindowX2 (L)*	86	
B-56	**00**	*WindowY2 (H)*	01	
B-57	**92**	*WindowY2 (L)*	E6	
B-61	**0D**	*VsyncStartRow(L)*	0C	
B-63	**EC**	*VsyncStopRow(L)*	EC	
B-80	**6A**	*ScaleX*	2	
B-81	**6A**	*ScaleY*	20	
B-82	**3E**	*Reserved*	04	
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	
C-11	**0B**	*AEWinX (H)*	25	AE Window Position
C-13	**08**	*AEWinY (L)*	1C	
C-14	**00**	*AEWinWidth (H)*	02	
C-15	**87**	*AEWinWidth (L)*	60	
C-16	**00**	*AEWinHeight (H)*	01	
C-17	**8E**	*AEWinHeight (L)*	BE	
C-19	**45**	*AECenterWinX (L)*	E5	AE Center Window Position
C-1B	**28**	*AECenterWinY (L)*	87	
C-1D	**30**	*AECenterWidth (L)*	A0	
C-1F	**30**	*AECenterHeight (L)*	A0	

- Flicker Free Mode

(1) Manual Flicker Free Mode

-Related Registers : Reg.B-11h, Reg.C-04h, Reg.B-21h ~ A-26h

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Setting value	Descriptions
B-21	*fd_period60 (H)*	00	$256 * \frac{\text{MCLK Freq.}/(\text{Frame Width} * 2)}{120}$	60Hz flicker period
B-22	*fd_pediod60 (M)*	50		
B-23	*fd_pediod60 (L)*	C0		
B-24	*fd_period50 (H)*	00	$256 * \frac{\text{MCLK Freq.}/(\text{Frame Width} * 2)}{100}$	50Hz flicker period
B-25	*fd_period50 (M)*	43		
B-26	*fd_period50 (L)*	4A		

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Setting Value	Descriptions
B-11	*FdControl2*	00	**00**	Normal mode (flicker free disable)
			08	60Hz manual flicker free enable
			04	50Hz manual flicker Free enable

- Flicker Period Control Register Setting

ex) 60Hz flicker, MCLK = 24MHz

Frame Width = *Frame Width (Reg B-48h,B-49h) + 1 = 800d.*

→ *Period60 = 256*(24000000 / (800 * 2)) / (60*2) = 32000d = 7D00h.*

→ *fd_period60 (H) = 00h, fd_period60 (M) = 7Dh, fd_period60 (L) = 00h.*

ex) 50Hz flicker, MCLK = 24MHz

Frame Width = *Frame Width (Reg B-48h,B-49h) + 1 = 800d..*

→ *Period50 = 256*(24000000 / (800 * 2)) / (50*2) = 38400d = 9600h.*

→ *fd_period50 (H) = 00h, fd_period50 (M) = 96h, fd_period50 (L) = 00h.*

(2) Auto Flicker Detection Mode

PO6030K support auto flicker detection mode.

Reg. Addr. (Hex)	Appropriate value	Register Name	Default Value (Hex)	Descriptions
B-19	$\frac{256*256*4}{60\text{Hz flicker period (line)}}$	*Reserved*	0C	
B-1A		*Reserved*	CC	
B-1B	$\frac{256*256*4}{50\text{Hz flicker period (line)}}$	*Reserved*	0E	
B-1C		*Reserved*	37	
B-20	*Appropriate Value*	*fd_th*	10	licker Detection Threshold
B-21	$256*\frac{\text{MCLK Freq.}/(\text{Frame Width}*2)}{120}$	*fd_period60 (H)*	50	Flicker Period for 60Hz flicker
B-22		*fd_period60 (M)*	C0	
B-23		*fd_period60 (L)*	00	
B-24	$256*\frac{\text{MCLK Freq.}/(\text{Frame Width}*2)}{100}$	*fd_period50 (H)*	00	Flicker Period for 50Hz flicker
B-25		*fd_period50 (M)*	43	
B-26		*fd_period50 (L)*	4A	
B-27	$\frac{\text{MCLK Freq.}/(\text{Frame Width}*2)}{20}$	*fd_periodC (H)*	01	Period (line) for CASE C
B-28		*fd_periodC (L)*	93	

Reg. Addr. (Hex)	Setting Value (Hex)	Register Name	Default Value (Hex)	Descriptions
B-11	**32**	*FdControl2*	00	50Hz / 60Hz flicker Auto Detection

- Flicker Detection Control Registers Setting

ex) Frame Width = *Frame Width (Reg A-48h,A-49h) + 1 = 800d, MCLK = 24MHz*

(1) Period60 (60Hz flicker) = 256(24000000 / (800 * 2)) / (60*2) = 32000d = 7D00h.*

→ fd_period60 (H) = 00h, fd_period60 (M) = 7Dh, fd_period60 (L) = 00h.

(2) Period50 (50Hz flicker) = 256(24000000 / (800 * 2)) / (50*2) = 38400d = 9600h.*

→ fd_period50 (H) = 00h, fd_period50 (M) = 96h, fd_period50 (L) = 00h

*(3) PeriodC = (24000000 / (800 * 2)) / 20 = 750d = 2EEh.*

→ fd_periodC (H) = 02h, fd_periodC (L) = EEh

*(4) Reg.B-19h ~ 1Ah = 256*256*4 / (Period60 / 256) = 256*256*4 / 125 = 2097d = 831h*

→ Reg.B-19h = 08h, Reg.B-1Ah = 31h

*(5) Reg.B-1Bh ~ 1Ch = 256*256*4 / (Period50 / 256) = 256*256*4 / 150 = 1748d = 6D4h*

→ Reg.B-1Bh = 06h, Reg.B-1Ch = D4h

- Output Format

1) YCbCr422 (8 Bit, Y range : 16 ~ 235, Cb & Cr range : 16 ~ 240) – CCIR.601

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
B-38	**xxxx0000**	*Format*	00	Cb Y Cr Y…
	xxxx0001			Cr Y Cb Y…
	xxxx0010			Y Cb Y Cr…
	xxxx0011			Y Cr Y Cb…

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
B-90	**E0**	*CS Max*	FF	CbCr range
B-91	**37**	*Y Contrast*	40	Y range
B-92	**10**	*Brightness*	01	..
B-93	**EB**	*Y Max*	FE	..
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	

2) YUV422 (8 Bit, Y range : 1 ~ 254 , U & V range : 1 ~ 254)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
B-38	**xxxx0000**	*Formar*	00	U Y V Y…
	xxxx0001			V Y U Y…
	xxxx0010			Y U Y V…
	xxxx0011			Y V Y U…

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
B-90	**FF**	*CS Max*	FF	CbCr range
B-91	**40**	*Y Contrast*	40	Y range
B-92	**01**	*Brightness*	01	..
B-93	**FE**	*Y Max*	FE	..
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	

3) RGB565 (8 Bit)

Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Hex)	Descriptions
B-38	**xxxx1000**	*Format*	00	R5G3, G3B5…
	xxxx1001			B5G3, G3[illegible]5…
B-90	**FF**	*CS Max*	FF	C[illegible]Cr rang[illegible]
B-91	**40**	*Y Contrast*	40	[illegible] range
B-92	**01**	*Brightness*	01	..
B-93	**FE**	*Y Max*	FE	..
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	[illegible]0	

4) Raw RGB Bayer (8 Bit)

Reg. Addr. (Hex)	Setting value	Register Name	Default Value (Hex)	Descriptions
B-38	**xxxx0100(b)**	*Format*	00	RGRG…GBGB…
	xxxx0101(b)			GBGB…RGRG…
	xxxx0110(b)			GRGR…BGBG…
	xxxx0111(b)			BGBG…GRGR…
B-30	**03(h)**	*ISPControl0*	FF	Color Correction / Edge Enhancement Off
B-31	**xxxxxx[illegible](b)**	*ISPControl1*	FF	
B-32	**xxx[illegible]xx0[illegible]**	*ISPControl2*	01	Lens shading Off
B-33	**xx[illegible]x0xx[illegible](b)**	*ISPControl3*	D8	Gamma Off
B-90	**FF**	*CS Max*	FF	CbCr range
B-91	**40**	*Y Contrast*	40	Y range
B-92	**01**	*Brightness*	01	..
B-[illegible]	**FE**	*Y Max*	FE	..
B-6[illegible]	*Refer to PCLK rate in page 70*	*SyncControl0*	00	

5) Mono (8 Bit)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
B-38	**0D**	*Format*	00	YYYY…
B-91	**40**	*Y Contrast*	40	Y range
B-92	**01**	*Brightness*	01	..
B-93	**FE**	*Y Max*	FE	..
B-68	*Refer to PCLK rate in page 70*	*SyncControl0*	00	

- PCLK rate

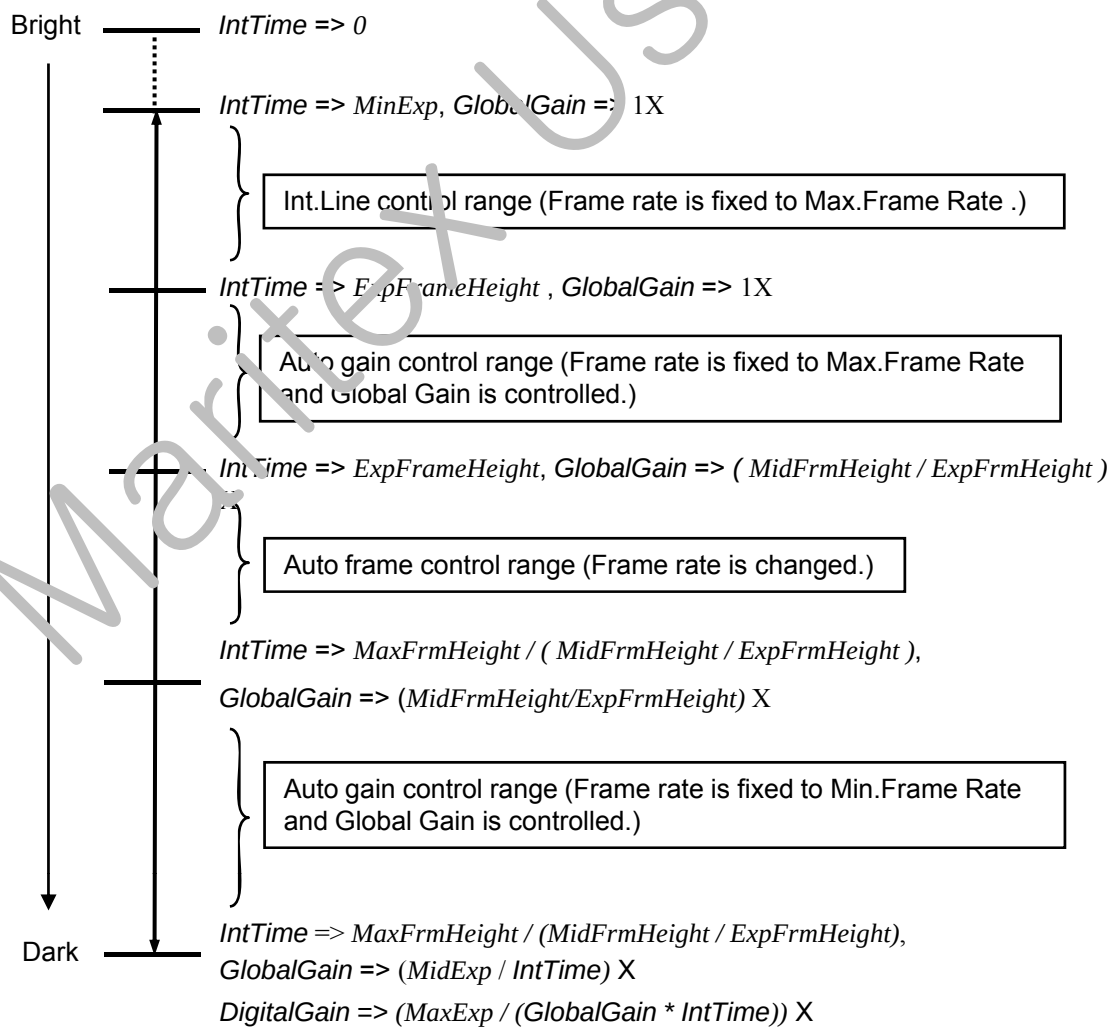
Reg. Addr. (Hex)	Setting value (Bin)	Register Name	Default Value (Bin)	Descriptions	
B-68	**xxxx0001**	*SyncControl0*	xxxx0000	RGB Bayer, Mono	VGA
	xxxx0011				CIF
	xxxx0011				QVGA
	xxxx0100				QCIF
	xxxx0111				QQVGA
	xxxx0000			YUV422, YCbCr422, RGB565	VGA
	xxxx0001				CIF
	xxxx0001				QVGA
	xxxx0010				QCIF
	xxxx0011				QQVGA

- AE Control

(1) Internal AE Control

Related Registers : Int.Time(Reg.C-4Ch ~ C-4Eh), GlobalGain(Reg.C-50h), AutoControl1(Reg.C-04h), MidFrmHeight(Reg.C-34h, C-35h), MaxFrmHeight(Reg.C-36h, C-37h), MidExp(Reg.C-3Ch ~ C-3Eh), MaxExp (Reg.C-40h ~ C-42h), MinExp(Reg.C-44 ~ C-46h), ExpFrmHeight(Reg.C-48 ~49h), AELock(Reg.C-57h)

If bit[1..0] of *AutoControl1(Reg.C-04h*) register is set to "00", *IntTime(Reg.C-4Ch ~ C-4Eh)*, *GlbGain(Reg.C-50h)* registers are automatically controlled by ISP to adjust overall brightness of sensor image. During auto exposure process, the average brightness of image is adjusted to get close to Target Exp. value with the margin set by *AELock*(*Reg.C-57h*) register. *IntTime* registers are controlled, at first. If Integration Line is limited to the *MaxFrmHeight*(*Reg.C-36h, C-37h*), then Global Gain is controlled. Variation of *GlbGain* and *IntTime* registers are limited by *MaxExp, MidExp*, *MinExp and MaxFrameHeight* registers described in the figure below.



Auto Frame Control Method can be used to get brighter image in dark condition. Frame rate is automatically controlled by ISP between Max.Frame Rate and Min.Frame Rate.

Max. Frame Rate = (MCLK frequency) / (Frame Height * Frame Width * 2)
Min. Frame Rate
= (MCLK frequency) / ((*MaxFrmHeight / Mid. Global Gain)** Frame Width * 2)
Max. Int. Time = *MaxFrmHeight / Mid. Global Gain* ------ (1)
Min. Int. Time = *MinExposure* ------ (2)
(Frame Height = *FrameHeight* + 1, Frame Width = *FrameWidth* + 1)

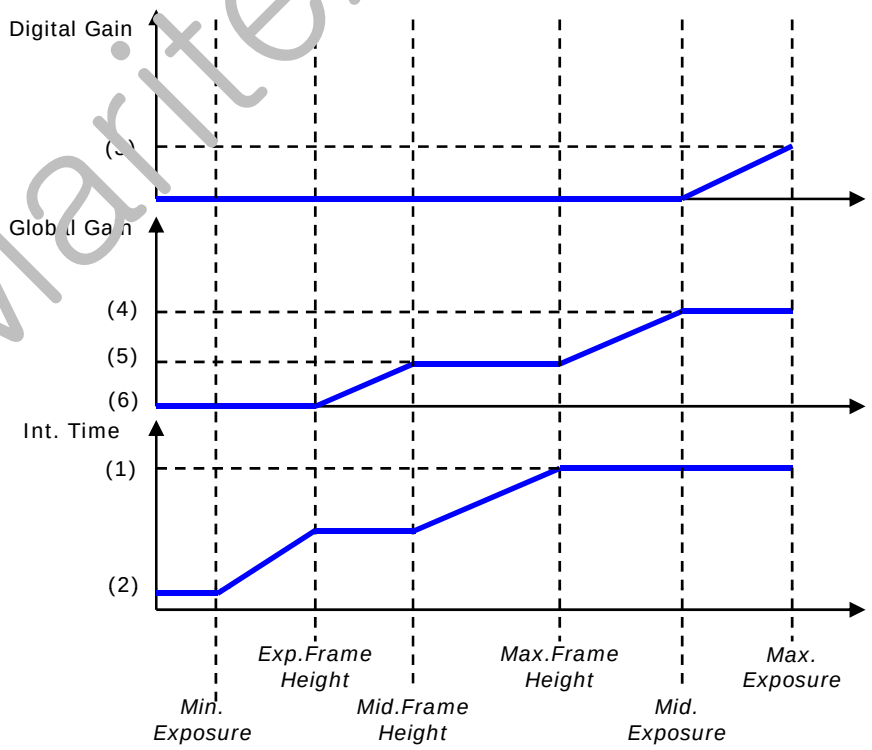
Min. Frame Rate is controlled by *MaxFrmHeight* register. *MaxFrmHeight* must be bigger than *ExpFrmHeight* and *MidFrmHeight*.(*MaxFrmHeight* >= *MidFrmHeight* >= *ExpFrmHeight*)

2) Auto Gain Control

Auto Gain Control Method can be used to get brighter image in dark condition. Global gain is controlled automatically by ISP between Max.Global Gain and Min.Global Gain.

Max. Gain = Max. Global Gain * Max. Digital Gain
Max. Digital Gain = *(MaxExp / (*Max. Global Gain * Max. Int. Time*))* X ------ (3)
Max. Global Gain = (*MidExp* / Max. Int. Time) X ------ (4)
Mid. Global Gain = (*MidFrmHeight* / *ExpFrmHeight*) X ------ (5)
Min. Global Gain = 1X ------ (6)

MaxExp must be bigger than *MaxFrmHeight* (*MaxExp >= MaxFrmHeight)* and *MidFrmHeight* must be bigger than *MaxFrmHeight* (*MidFrmHeight >= MaxFrmHeight*).



(2) External AE Control

1) Exposure Control Mode

Related Registers : AutoControl1 (Reg.C-04h), Exposure (Reg.C-2Ch ~ C-2Fh)

If you turn off internal AE function of PO6030K, you can control Integration line and Global gain through *Exposure (Reg.C-2Ch ~ C-2Fh)* registers for implementing external Auto Exposure function. *IntTime* (*Reg.C-4Ch ~ C-4Eh*) and *GlobalGain* (*Reg.C-50h*) registers aren't accessible by user. *Exposure* (*Reg.C-2Ch ~ C-2Fh*) registers aren't controllable while internal AE is working.

- Disable Internal AE Function for This Mode

Reg. Addr. (Hex)	Register Name	Descriptions
C-04	*AutoControl1*	Set bit [1..0] to "01" to turn off internal AE function and control it by Exposure registers.
C-55	*AEUpSpeed*	Set this register to 00h
C-56	*AEDownSpeed*	Set this register to 00h

- Registers for External AE Control

Reg. Addr. (Hex)	Register Name	Descriptions
C-2C	*Exposure(T)*	Exposure register
C-2D	*Exposure(M)*	
C-2E	*Exposure(M)*	
C-2F	*Exposure(L)*	

(1) *MinExp* < *Exposure* ≤ *FrameHeight* (Int.Line Control Range)

(2) *FrmHeight* < *Exposure* ≤ *MidExp* (Global Gain Control Range)

(2) *FrameHeight* < *Exposure* ≤ *MaxFrmHeight* (Frame Rate Control Range)

Current Frame Rate = (MCLK freq.) / (*Exposure – (MidExp + FrameHeight)*) * Frame Width * 2)
Min. Frame Rate is limited by *MaxFrmHeight*.

(3) *MaxFrmHeight* < *Exposure* ≤ *MaxExp* (Global Gain Control Range)

Current Global Gain = (*MidExp* / *FrameHeight*) * (*Exposure* / *MaxFrmHeight*) X
Max.Gain is limited by *MaxExp*.

2) Manual External IntTime and Global Gain Control Mode

Related Registers : AutoControl1 (Reg.C-04h), ExtIntTime (Reg.C-24h ~ 26h), ExtLGlbG (Reg.C-28h, C-29h)

If you turn off internal AE function of PO6030K, you can control Integration line and Global gain through ExtIntTime *(Reg.C-24h ~ C-26h)* and ExtGlbG *(Reg.C-28h, C-29h)* registers for implementing external Auto Exposure function. *IntTime* (*Reg.C-4Ch ~ C-4Eh*) and *GlobalGain* (*Reg.C-50h*) registers aren't accessible by user. ExtIntTime and ExtGlbG registers aren't controllable while internal AE is working.

- Disable Internal AE Function for This Mode

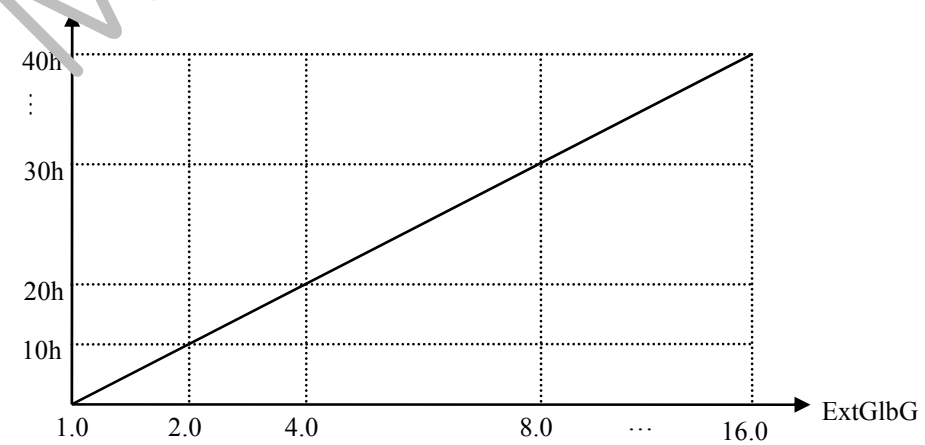
Reg. Addr. (Hex)	Register Name	Descriptions
C-04	*AutoControl1*	Set bit 1& 0 (AEr) to "10" to turn off internal AE function & control it by External Int.Time & External Global Gain.
C-55	*AEUpSpeed*	Set this register to 00h
C-56	*AEDownSpeed*	Set this register to 00h

- Registers for External AE Control

Reg. Addr. (Hex)	Register Name	Descriptions
C-24	*ExtIntTime(H)*	External Integration Time
C-25	*ExtIntTime(M)*	
C-26	*ExtIntTime(L)*	
C-28	*ExtLGlbG(H)*	External Global Gain (1X : Reg.C-28h = 01h, Reg.C-29h = 00h (Min.) 16X : Reg.C-28h =10h, Reg.C-29h = 00h (Max.))
C-29	*ExtLGlbG(L)*	

(1) *IntTime = ExtIntTime*

(2) *ExtLGlbG*



- AWB Control

(1) Internal AWB Control

Related Registers : RGain(Reg.C-A4h), GGain(Reg.C-A5h), BGain(Reg.C-A6h), AWBRratio(Reg.C-84h), AWBBratio(Reg.C-85h),

If bit[2] of *AutoControl1(Reg.C-04*h) register is set to '1', *RGain*(*Reg.C-A4h*) and *BGain*(*Reg.C-A6h*) registers are automatically controlled by ISP to control the RGB ratio of sensor image. The ratio of average of R, G, B components can be controlled by *AWBRratio and AWBBratio* registers. Those ratios are defined according to the following relation,

$$\overline{B} = \frac{AWBBratio}{128} \times \overline{G} \qquad \overline{R} = \frac{AWBRratio}{128} \times \overline{G}$$

(2) External AWB Control

If you turn off internal AWB function of PO6030K, you can control R, G and B gains through *R, G* and *B Gain* (*Reg.C-A4h ~ C-A6h*) registers for implementing external Auto White Balance function. *R* and *B gain* registers aren't controllable while internal AWB is working.

- Disable Internal AWB Function

Reg. Addr. (Hex)	Register Name	Descriptions
C-04	*AutoControl1*	Set bit [2] to '0' to turn off internal AWB function.

- Registers for external AWB control

Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Descriptions
C-A4	*R Gain*	40	1X R Gain = 0x40 (2X = 0x80)
C-A5	*G Gain*	40	1X G1 Gain = 0x40
C-A6	*B Gain*	40	1X B Gain = 0x40

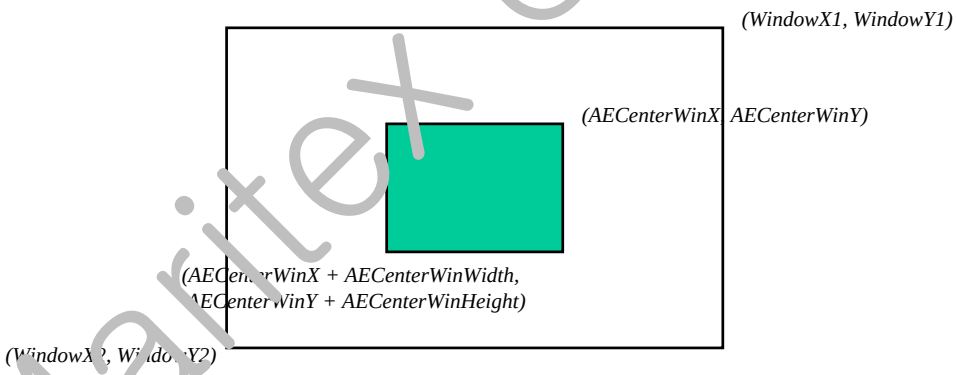
- Backlight Compensation

Related Registers : AECenterWinX (Reg.C-18h, 19h), AECenterWinY (Reg.C-1Ah, 1Bh),

AECenterWinWidth (Reg.C-1Ch, 1Dh), AECenterWinHeight (Reg.C-1Eh, 1Fh), AECenterWeight (Reg.C-54h)

1) Weight Window

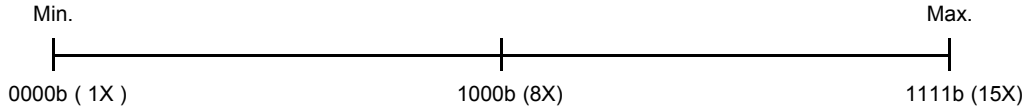
Reg. Addr. (Hex)	Register Name	Default Value (Hex)	Description
C-18	*AECenterWinX (H)*	00	**Minimum** : *WindowX1(Reg.B-50h, 51h)*
C-19	*AECenterWinX (L)*	E5	
C-1A	*AECenterWinY (H)*	00	**Maximum** : *WindowX2(Reg.B-54h, 55h)*
C-1B	*AECenterWinY (L)*	87	
C-1C	*AECenterWinWidth (H)*	00	**Minimum** : *WindowY1(Reg.B-52h, 53h)*
C-1D	*AECenterWinWidth(L)*	A0	
C-1E	*AECenterWinHeight (H)*	00	**Maximum**: *WindowY2(Reg.B-56h, 57h)*
C-1F	*AECenterWinHeight (L)*	A0	



2) Weight Factor

Weight Factor is controlled by AECenterWeight register (*Reg.C-54h*).

0000b ≤ Weight Factor ≤ 1111b



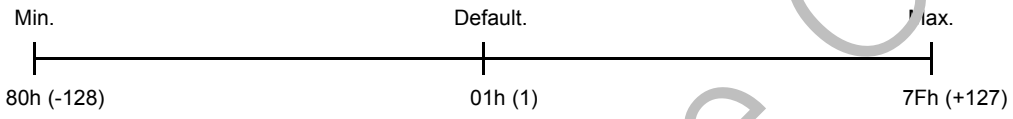
- Brightness / Y Contrast

-Related Registers : Brightness (Reg.B-92h), YContrast (Reg.B-91h)

Y *reault* = Y * (Ycontrast / 64) + Brightness

(1) Brightness

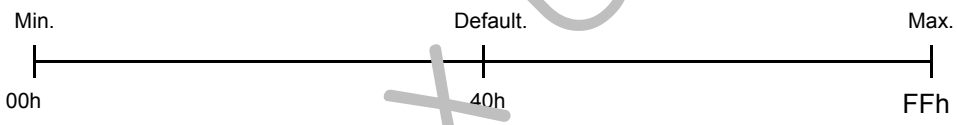
Brightness is controlled by *Brightness* register (*Reg.B-92h*). The default value of this register is 01h.



* Brightness : 2's compliment

(2) Y Contrast

Contrast is controlled by Y *Contrast* register (*Reg.B-91h*). The default value of this register is 40h.



- Color Correction Matrix

Related Registers : ColorMatrix11 (Reg.B-A4h) ~ ColorMatrix33 (Reg.B-ACh)

Color correction can be accomplished by color transform registers (*Reg.B-A4h ~ B-ACh*) by means of the following equation, where ***CC*** is 3x3 color correction matrix.

$$\begin{pmatrix} CT0 & CT1 & CT2 \\ CT3 & CT4 & CT5 \\ CT6 & CT7 & CT8 \end{pmatrix} = \begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * CC$$

* m00 ~ m22 : (bit7) | (bit6 ~ bit0) = sign digit | magnitude

<Ex.>

$$\begin{pmatrix} m00 & m01 & m02 \\ m10 & m11 & m12 \\ m20 & m21 & m22 \end{pmatrix} = 32 * \begin{pmatrix} 1.7396 & -1.1444 & 0.4048 \\ -0.6039 & 1.4137 & 0.1902 \\ -0.1225 & -1.1094 & 2.4119 \end{pmatrix}$$

$$= \begin{pmatrix} 55.6672 & -36.6208 & 12.9536 \\ -19.3248 & 45.2384 & 6.0864 \\ -3.28 & -41.9008 & 77.1808 \end{pmatrix} = \begin{pmatrix} 38h & A5h & 0Dh \\ 93h & 2Dh & 06h \\ 83h & AAh & 4Dh \end{pmatrix}$$

- Sharpness Control

Related Registers : EdgeGain (Reg.B-9Ch), EdgeThreshold (Reg.B-9Dh)

Sharpness is controlled by *EdgeGain (Reg.B-9Ch)* and *EdgeThreshold* register *(Reg.B-9Dh).* All three values have the following Min. and Max. value.

00h ≤ *EdgeGain* ≤ 3Fh
00h ≤ *EdgeThreshold* ≤ FFh

The lowest sharpness level can be gotten by setting registers as follows.

EdgeGain = 00h, *EdgeThreshold* = FFh

And, the highest sharpness level can be gotten by setting registers as follows.

EdgeGain = 3Fh, *EdgeThreshold* = 00h

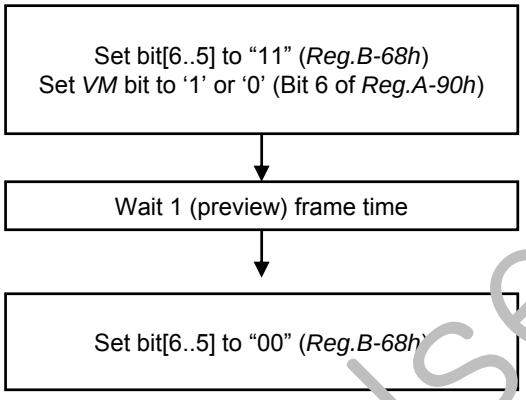
But, we recommend to set *EdgeThreshold* register value greater than 01h.

- Vertical / Horizontal Mirror

Related Registers : BayerControl01(Reg.A-90h), SyncControl0(Reg.B-68h)

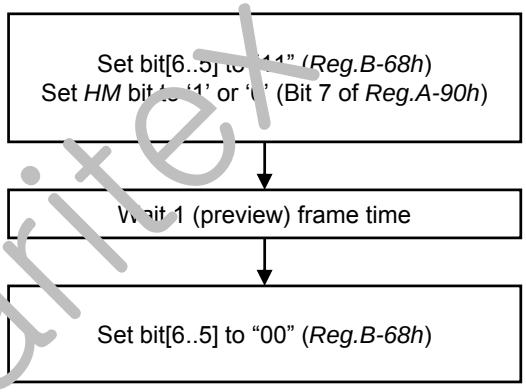
(1) Vertical Mirror

Vertical Mirror is controlled by *VM* bit (Bit 7 of *Reg.A-90h*).



(2) Horizontal Mirror

Horizontal Mirror is controlled by *HM* bit (Bit 6 of *Reg.A-90h*).



- Special Effect

(1) Color Effect

Related Registers : ISPFunc2 (Reg.B-32), CbTone (Reg.B-84h), CrTone (Reg.B-85h)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
B-32	**81**	*ISPFunc2*	01	
B-84	***Appropriate Value***	*CbTone*	80	
B-85	***Appropriate Value***	*CrTone*	80	

Sepia (Reg.B-84h : A0h, Reg.B-85h : 20h)

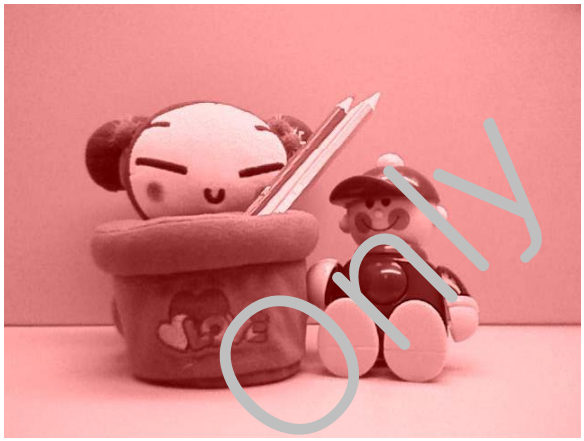
Green (Reg.B-84h : C0h, Reg.B-85h : C0h)

Aqua (Reg.B-84h : 20h, Reg.B-85h : C0h)

Red (Reg.B-84h : 00h, Reg.B-85h : 50h)

1/6.2 inch VGA Single Chip CMOS Image Sensor with 640 X 480 Pixel Array

Cool (Reg.B-84h : 50h, Reg.B-85h : C0h)



Warm (Reg.B-84h : 90h, Reg.B-85h : 30h)

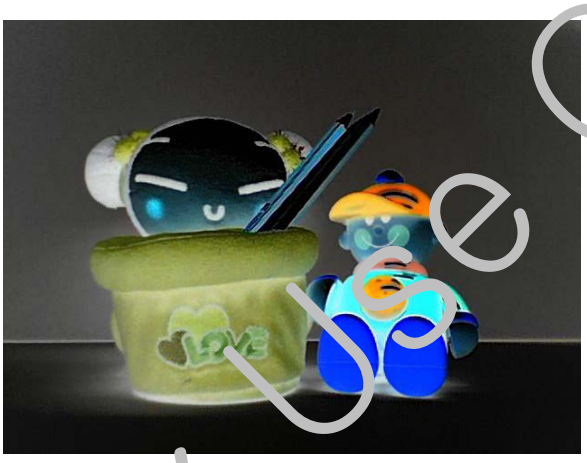
BW (Reg.B-84h : 00h, Reg.B-85h : 00h)

Antique (Reg.B-84h : 90h, Reg.B-85h : 10h)

(2) Negative Effect

Related Registers : ISPFunc2 (Reg.B-32h), Reserved (Reg.C-5Ah)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
C-5A	**02**	*Reserved*	03	
B-32	**09**	*ISPFunc2*	01	

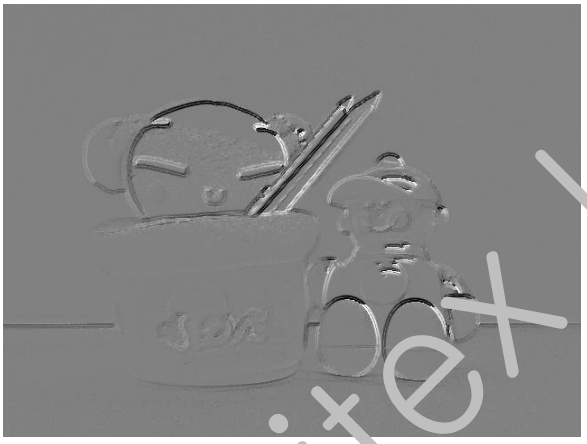


Negative

(3) Embossing Effect

Related Registers : SketchOffset2 (Reg.B-89h), ISPFunc2 (Reg.B-32h), Reserved (Reg.C-5Ah)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
C-5A	**01**	*Reserved*	03	
B-89	**80**	*SketchOffset2*	C8	
B-32	**21**	*ISPFunc2*	01	Embossing mode 0
B-32	**31**	*ISPFunc2*	01	Embossing mode 1



Embossing mode 0

Embossing mode 1

(4) Sketch Effect

Related Registers : ISPFunc2 (Reg.B-32h), SketchOffset1 (Reg.B-88h), SketchOffset2 (Reg.B-89h), SketchOffset3 (Reg.B-8Ah), SketchOffset4 (Reg.B-8Bh), Reserved (Reg.C-5Ah)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
C-5A	**01**	*Reserved*	03	
B-32	**41**	*ISPFunc2*	01	
B-88	***Appropriate Value***	*SketchOffset1*	20	
B-89	***Appropriate Value***	*SketchOffset2*	C8	
B-8A	***Appropriate Value***	*SketchOffset3*	1	
B-8B	***Appropriate Value***	*SketchOffset4*	80	

Sketch image 1

SketchOffset1 : FFh

SketchOffset2 : FFh

SketchOffset3 : 08h

SketchOffset4 : FFh

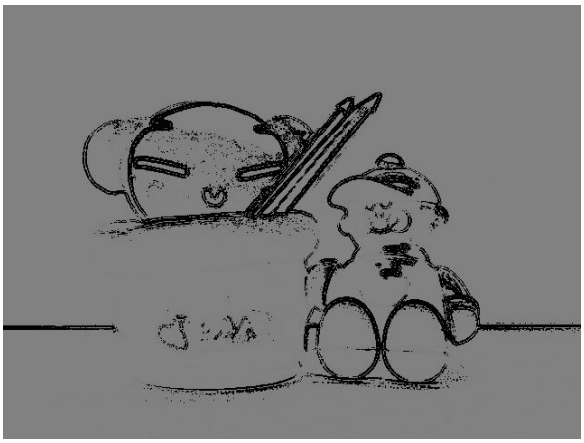
Sketch image 2

SketchOffset1 : FFh

SketchOffset2 : FFh

SketchOffset3 : 08h

SketchOffset4 : 80h



Sketch image 3

SketchOffset1 : FFh

SketchOffset2 : 80h

SketchOffset3 : 08h

SketchOffset4 : FFh

Sketch image 4

SketchOffset1 : 20h

SketchOffset2 : 80h

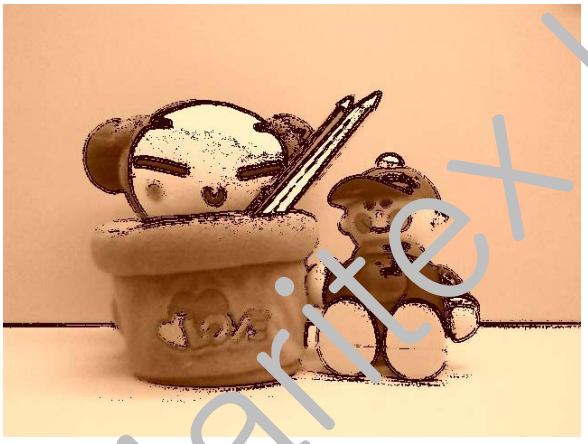
SketchOffset3 : 08h

SketchOffset4 : FFh

(5) Sketch Effect with Color Effect

Related Registers : ISPFunc2 (Reg.B-32h), CbTone (Reg.B-84h), CrTone (Reg.B-85h), SketchOffset (Reg.B-88h ~ 8Bh), Reserved (Reg.C-5Ah)

Reg. Addr. (Hex)	Setting value (Hex)	Register Name	Default Value (Hex)	Descriptions
C-5A	**01**	*Reserved*	03	
B-32	**C1**	*ISPFunc2*	01	
B-84	***Appropriate Value***	*CbTone*	C0	
B-85	***Appropriate Value***	*CrTone*	40	
B-88	**00**	*SketchOffset1*	20	
B-89	**00**	*SketchOffset2*	C8	
B-8A	**08**	*SketchOffset3*	10	
B-8B	**FF**	*SketchOffset4*	80	



Sketch with Sepia tone

(Reg.B-84 : A0h, Reg.B-85 : 20h)

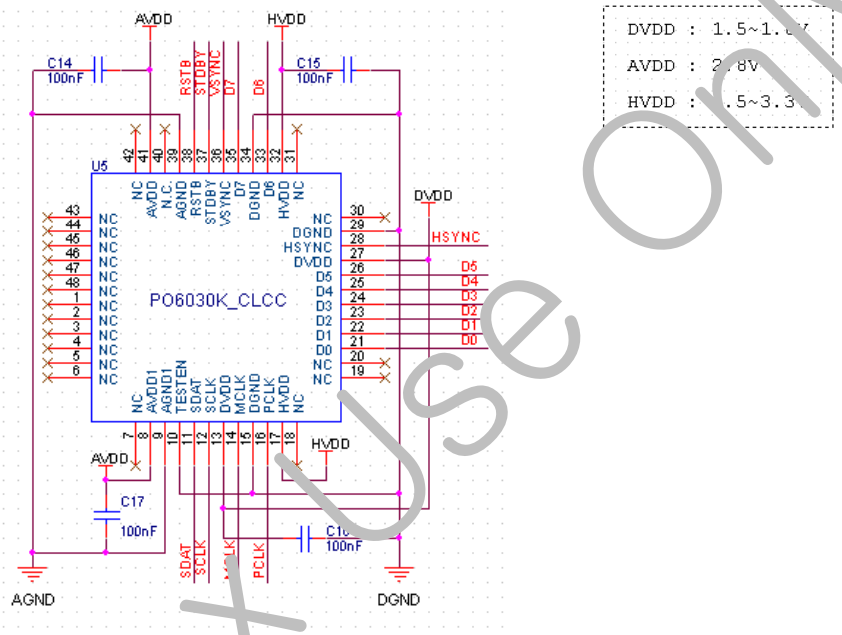
Sketch with Green tone

(Reg.B-84h : C0h, Reg.B-85h : C0h)

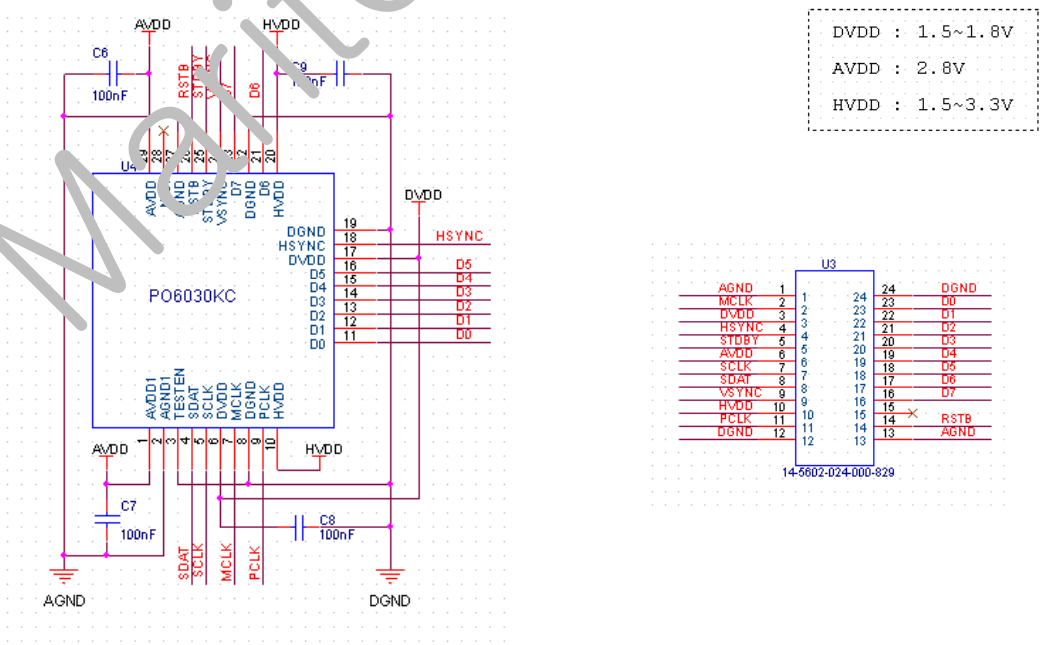
Please refer to the color effect chapter to use more variety color effect.

- PC Board Layout Considerations

It is important that care be given to the PC board layout to reduce power noise. <Fig.A-1> & <Fig.A-2> show the recommended connection diagram for the PO6030K.



< Fig.A-1 > PO6030K typical connection diagram (CLCC)



< Fig. A-2 > PO6030K module typical connection diagram (COB)

Ground Planes

The ground plain should connect to the regular PCB ground plane at a single point This ground plane also has two distinct power planes, one for analog pins and one for digital pins. The analog ground plane should encompass AGND pin, and the digital ground plane should encompass DGND & HGND pin.

Power Planes

The PC board layout should have the distinct power plane for PO6030K. This power plane should have the separate regulator or be connected to the regular PCB power plane(VCC) at a single point. This power plane also has four distinct power planes, two for analog pins, one for digital pins and one for I/O pins. The analog power planes should encompass each AVDD pins, the digital power plane should encompass DVDD pin and IO power plane should encompass HVDD pin.

Supply Decoupling

Noise on the PO6030K power plane can be reduced by the use of multiple decoupling capacitors. Optimum performance is achieved by the use of 0.1uF ceramic capacitors for HVDD, DVDD & AVDD. Each of the power pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to power pins with the capacitor leads as short as possible, thus minimizing lead inductance.

- Stand-by method

1. Standby pin (Hardware Method)

⇒ You can control stand-by mode by using STDBY pin.

LOW : normal mode
HIGH : stand-by (power-down) mode

2. 2-wire serial interface Stand-by (Software Method)

⇒ You can control stand-by mode by setting *STDBY* bit (bit 1) of *Reg.B-34h.*

⇒ ***STDBY pin must be connected to DGND***

'0' : normal mode
'1' : stand-by (power-down) mode