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PS171 DisplayPort™ to HDMI/DVI Converter with HDMI 1.4a 3.0 Gbps Support

Version 0.9

Jan. 31, 2012

REVISION HISTORY

Preliminary, 05/15/2011

1. Initial Preliminary release.

Version 0.8, 11/01/2011

1. Updated characterization data
2. Updated the display timing list

Version 0.9, 1/31/2011

1. Updated the thermal data
2. Updated characterization data
3. Updated the packing information

KEY FEATURES

- Supports DisplayPort™ 1, 2, and 4 lanes
- Supports full link training, fast link training and no link training
- Supports multiple color format: RGB 6/8/10/12-bit per component (bpc) and YCbCr4:4:4, YCbCr4:2:2 8/10/12 bpc
- HDMI 1.4a compliant with maximum data rate 3.0Gbps
- Supports 10/12-bit deep color 1080p up to 2.25Gbps and 3D video formats (720p@50/59.94/60Hz, 1080i@50/59.94/60Hz, 1080p@23.98/24Hz, 1080p@50/59.94/60Hz) up to 2.97Gbps
- DVI 1.0 transmitter support
- Supports up to 8 channel LPCM, compressed audio (AC-3, DTS) and HBR audio format
- Supports up to 192kHz audio frame rate and up to 24-bit audio sample size
- Content protection of HDCP 1.3 for DisplayPort™ and HDMI/DVI
- Integrated both HDCP Rx and Tx keys to support HDCP repeater
- On-chip microprocessor with SPI ROM interface
- I2C slave interface for chip control
- I2C master for external EDID and expansion function
- Supports Interrupt request output for expansion function
- ESD: HBM 8kV
- 1.2V Core Power Supply & 3.3V I/O Power Supply
- 0°C to 70°C Operating Temperature Range
- 56-pin QFN Halogen free RoHS package

APPLICATIONS

- Docking Station
- Monitor and TV
- Thunderbolt Format Conversion
- DP to HDMI/DVI Format Converting Dongle

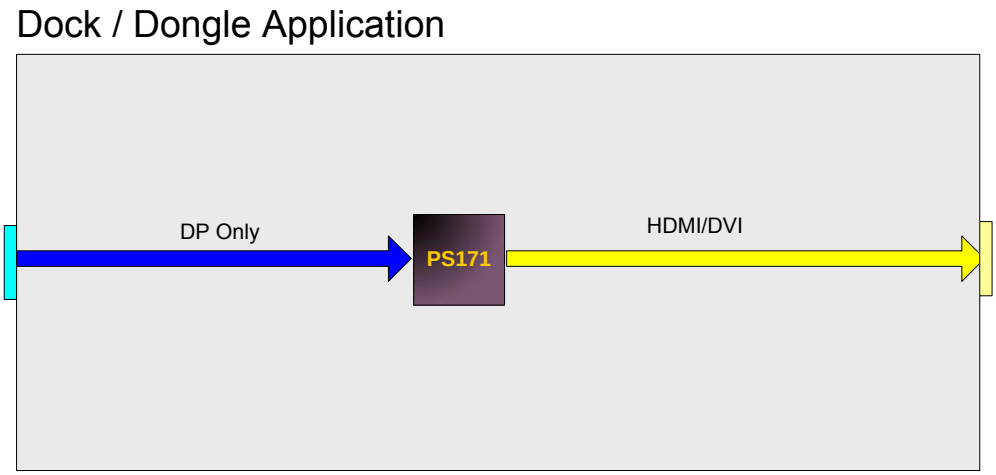


Figure1. Typical Application

DESCRIPTION

PS171 is a new generation DisplayPort™ to HDMI/DVI converter which receives both video and audio streams from DisplayPort™ link and converts to HDMI/DVI output. The HDMI transmitter is compliant to HDMI 1.4a specification and supports 3D video formats up to 2.97Gbps.

PS171 integrates both HDCP Rx & Tx keys for repeater application such as DP to HDMI/DVI format converting dongle etc.

The system level block diagram of PS171 is described in Figure 2. Detailed descriptions of each functional block are given in the following sections.

FUNCTIONAL BLOCK DIAGRAM

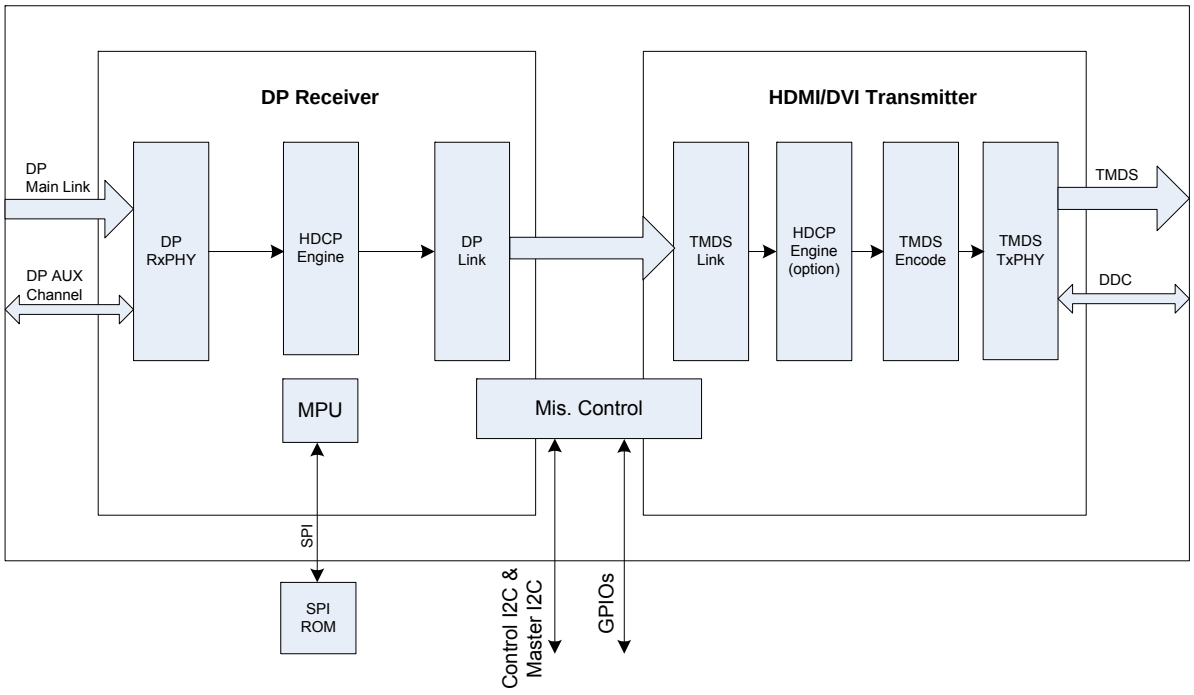


Figure2. PS171 Functional Block Diagram

DISPLAYPORT™ RECEIVER

The DisplayPort™ Receiver interface implemented in the PS171 is fully compliant to the *VESA DisplayPort Standard, Version 1.1a, for both 1.62Gbps and 2.7Gbps.*

Physical Layer (PHY)

The DisplayPort™ main link operates at a data rate of 2.7Gbps (High Bit Rate - HBR) or 1.62Gbps (Reduced Bit Rate - RBR). DisplayPort™ Receiver receives serial data stream, de-serializes it, and decodes it in ANSI 8B/10B format. Subsequently, the receiver unscrambles and de-skews the decoded data.

The DisplayPort™ AUX channel is a half-duplex, bi-directional channel which supports bit rate at 1 Mbps. The logical sub-block of AUX channel generates and detects Start/Stop condition and locks to Sync pattern, encodes or decodes of data using Manchester-II coding. The electrical sub-block of AUX channel consists of one differential pair which operates as a half-duplex bi-directional channel. The AUX channel provides Link Configuration, Link maintenance and EDID access.

The DisplayPort™ Hot Plug/Unplug detection is indicated by HPD signal. The HPD signal is asserted whenever the sink device is connected to its main power supply and the source (DP Tx) is detected. The pulsed HPD signal is also used as an Interrupt Request (IRQ) by sink device. The low-going pulse width within 0.5ms to 1.0ms is asserted as Interrupt Request (IRQ) from sink device to source device and source device shall read link status field of DisplayPort™ Configuration Data (DPCD) and take proper action.

Link Layer

The DisplayPort™ receiver Link Layer services reconstruct original video and audio data and timing base through isochronous transport services over main link. It also handles AUX Channel link service and device service. The main link supports 4-lane, 2-lane and 1-lane at 2.7Gbps or 1.62 Gbps data rate. The optimal lane count and data rate shall be negotiated through capability discovery and link training between source and sink devices. The isochronous transport services of Link Layer provide packing/unpacking, stuffing/un-stuffing, framing/un-framing, inter-lane skewing/de-skewing, stream clock recovery, insertion/extraction of Main Stream Attributes data and/or inserting/extracting of secondary-data packet with ECC (Error Control Code) for audio stream packet & CEA861-D InfoFrame packet.

PS171 DisplayPort™ receiver supports RGB444 (6/8/10/12-bit), YCbCr444 (8/10/12-bit) and YCbCr422 (8/10/12-bit) video input formats and supports up to 8 channels LPCM, compressed audio format (AC-3, DTS) and HBR audio format. Support audio frame rate of 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz and audio sample size of 16, 20 and 24 bits per sample.

HDMI TRANSMITTER

The High Definition Multimedia Interface (HDMI) implemented in the PS171 is fully compliant to the *High-Definition Multimedia Interface Specification, Version 1.4a, March 4, 2010.*

Compliance includes the capability to deliver audio and video content from the decoded DisplayPort™ audio and video streams onto an HDMI or DVI output. The HDMI interface provides support for up to 3.0Gbps data rate, allowing display up to 1080p at 60Hz refresh rate with 12-bit deep color and 3D video formats up to 1080p at 60Hz. Audio output support consists of up to 8 channels of LPCM at 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz and 192kHz sample rate and audio sample size of 16, 20 and 24-bits per sample, decoded by DisplayPort™ receiver. The PS171 also supports compressed audio formats (AC-3, DTS) and HBR audio format.

The HDMI interface provides support for a DDC channel for retrieval of the monitor EDID information and a monitor hot plug detect signal HPD to detect the attachment and presence of a sink device.

DVI TRANSMITTER

The Digital Visual Interface (DVI) implemented in the PS171 is compliant to the *Digital Visual Interface, Revision 1.0, April 2, 1999.*

PS171 supports single link (4 TMDS channels) connection to a DVI enabled monitor. The display supports up to a 1920x1200 resolution at 60Hz refresh rate (using standard VESA CVT timing), with 8-bit color mode.

The DVI interface provides support for a monitor hot plug detection signal, to detect the attachment and presence of a monitor, as well as a DDC channel for retrieval of the EDID information from the monitor.

Support of HDCP 1.3 specification and compliant with earlier versions of HDCP 1.0, 1.1 and 1.2.

HDCP REPEATER

The High-bandwidth Digital Content Protection (HDCP) provides a secure audio and video content on DisplayPort™ receiver and HDMI/DVI transmitter interfaces as well as appropriate security measures to prevent discovery and nullification of the HDCP keys stored within the PS171. PS171 is compliant with HDCP version 1.3 specification for DisplayPort™ receiver and compliant with HDCP version 1.0, 1.1, 1.2 and 1.3 specification for HDMI/DVI transmitter. The features of HDCP are summarized as below:

- The DisplayPort™ receiver side performs upstream HDCP function including HDCP authentication and HDCP decryption.
- The HDMI/DVI transmitter side performs downstream HDCP function including HDCP authentication and HDCP encryption.
- Software will interface with both upstream and downstream HDCP authentication engine to implement the HDCP repeater functions.

- HDCP repeater support up to 16 downstream devices
- Integrated both HDCP receiver and transmitter Key ROMs

HOT PLUG DETECTION (HPD)

PS171 is a DisplayPort™ to HDMI/DVI converter and it has two hot plug detection signals.

- HDMI_HPD: downstream port hot plug detection input
- DP_HPD: upstream port hot plug detection output

HDMI_HPD

HDMI_HPD is an input. A HIGH on this signal indicates that a HDMI or DVI sink is connected. Detecting the state change on this pin is the hardware responsibility. The interpretation of this signal and hence the actions taken after the HDMI_HPD state change is the firmware's responsibility.

HDMI_HPD state changes are mainly used in the PS171 operation and power state machine maintained by PS171 firmware.

DP_HPD

DP_HPD is an output signal. A high on this signal indicates that PS171 is ready to take DisplayPort™ input. Firmware will control this signal according to PS171 operation and power state machine.

After power on, DP_HPD signal will stay at low, once PS171 is ready to take DisplayPort™ input, this signal will be asserted HIGH.

Besides hot plug detection, DP_HPD signal is also used for the following:

- DisplayPort™ IRQ, including Link Status change, AUTOMATED_TEST_REQUEST and CP_IRQ. In these events, hardware will generate short low-going pulse (0.5ms ~ 1ms) on DP_HPD pin
- DisplayPort™ MCCS_IRQ and SINK_SPECIFIC_IRQ. Firmware will generate short low-going pulse (0.5ms ~ 1ms) in the two events

AUX TO I2C BRIDGE

AUX to I2C bridge acts as a bidirectional repeater function from DisplayPort™ AUX CH interface to HDMI/DVI DDC interface. It monitors DisplayPort™ AUX CH traffic and converts only those I2C-over-AUX CH transactions targeted to the HDMI sink device, as described below, into HDMI/DVI DDC interface.

- EDID access, I2C slave address of 60h, 61h, A0h and A1h
- MCCS communication: I2C slave address of 6Eh and 6Fh
- VESA DisplayID standard (proposed and legacy): I2C slave address of A0h through A7h

All other I2C-over-AUX transactions are blocked and assumed to be accessing functions within the PS171.

The AUX to I2C bridge provides an interface for PS171 firmware to interface AUX CH directly. This is to provide hardware support for firmware to handle all possible native AUX transactions and I2C-over-AUX transactions, including those targeted to the HDMI/DVI sink device.

The AUX to I2C bridge also provides an interface for PS171 to directly access HDMI/DVI DDC port. This function will be used when firmware needs to read EDID from downstream device, or to read downstream HDCP port directly.

ON-CHIP MICROPROCESSOR (MPU)

PS171 integrates a micro-processor unit (MPU) on-chip. The MPU core is an 8-bit processor which executes 8031/8051 type instructions. The instructions are stored in an external flash ROM with Serial Peripheral Interface (SPI) and can be accessed through the internal ROM bus. 512 bytes internal RAM and 128 bytes SFR (special function register) provide the temporal data storage space. The MPU accesses the internal registers through a memory bus.

There is total 512K bytes SPI ROM space available for the MPU in PS171. PS171 firmware is stored in this ROM. There are three ways to update the SPI ROM. One is to use offline SPI ROM programmer, one is through PS171 control I2C port and another one is through AUX CH.

EDID

There are two EDID operation cases for PS171.

EDID Relay: In this case, EDID can be relayed from DDC bus in HDMI transmitter interface to the AUX CH of DisplayPort™ receiver interface. When relaying the EDID from HDMI to DisplayPort™, PS171 does not do any modifications. DisplayPort™ source will know the type of downstream port through DPCD capability registers (DPCD 0x005, 0x008, and 0x080-08F).

EDID Store: In some special cases, EDID data can be fixed and does not need relay from sink side, then the EDID can be stored in SPI ROM. DisplayPort™ source will read the EDID from SPI ROM through AUX CH.

GENERIC I/O INTERFACES

There are 1 dedicated General Purpose Input/Output pin (GPIO) and 4 shared GPIO pins in PS171. Those GPIO pins have internal pull-down resistors.

CONTROL I2C SLAVE

Control I2C slave is the programming interface for external device to access internal registers, including DPCD registers. This bus is used to configure, control or debug PS171 internal functions.

In real application, this I2C bus may also be used as the interface for handshaking with external micro-controller.

I2C MASTER

PS171 has an I2C master. This I2C master can be used for three possible applications:

- Access external HDCP key ROM for DisplayPort™ receiver HDCP function. This is the back up, or debugging option, to replace internal OTP ROM.
- Access external HDCP key ROM for HDMI/DVI transmitter HDCP function. This is the back up, or debugging option, to replace internal OTP ROM.
- Control possible external expansion modules

If PS171 is configured as a HDCP repeater, optionally the downstream port HDCP key can be stored in the external EEPROM. In this case, I2C master will be used to read the HDCP key.

If PS171 is not configured as a HDCP repeater, this master I2C bus can be used to interface with external expansion modules.

DISPLAY RESOLUTIONS

Following tables provide the popular video modes that PS171 may support. PS171 will also support other video modes as long as they are within available DisplayPort™ bandwidth and TMDS clock frequency range of 25MHz to 300MHz.

Table 1. Video clock table for monitors

Resolution	Refresh Rate	Horizontal Frequency	Pixel Frequency	Standard Type	Original Document	Date
640 x 350	85 Hz	37.9 kHz	31.500 MHz	VESA Standard	VDMTPROP	3/1/96
640 x 400	85 Hz	37.9 kHz	31.500 MHz	VESA Standard	VDMTPROP	3/1/96
720 x 400	85 Hz	37.9 kHz	35.500 MHz	VESA Standard	VDMTPROP	3/1/96
640 x 480	60 Hz	31.5 kHz	25.175 MHz	Industry Standard	n/a	n/a
	72 Hz	37.9 kHz	31.500 MHz	VESA Standard	VS901101	12/2/92
	75 Hz	37.5 kHz	31.500 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	43.3 kHz	36.000 MHz	VESA Standard	VDMTPROP	3/1/96
800 x 600	56 Hz	35.1 kHz	36.000 MHz	VESA Guidelines	VG900601	8/6/90
	60 Hz	37.9 kHz	40.000 MHz	VESA Guidelines	VG900602	8/6/90
	72 Hz	48.1 kHz	50.000 MHz	VESA Standard	VS900603A	8/6/90
	75 Hz	46.9 kHz	49.500 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	53.7 kHz	56.250 MHz	VESA Standard	VDMTPROP	3/1/96
848 x 480	60 Hz	31.0 kHz	33.750 MHz	VESA Standard	AddDMT	3/4/03
1024 x 768	43 Hz Interlaced	35.5 kHz	44.900 MHz	Industry Standard	n/a	n/a
	60 Hz	48.4 kHz	65.000 MHz	VESA Guidelines	VG901101A	9/10/91
	70 Hz	56.5 kHz	75.000 MHz	VESA Standard	VS910801-2	8/9/91

	75 Hz	60.0 kHz	78.750 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	68.7 kHz	94.500 MHz	VESA Standard	VDMTPROP	3/1/96
1152 x 864	75 Hz	67.5 kHz	108.000 MHz	VESA Standard	VDMTPROP	3/1/96
1280 x 768	60 Hz	47.4 kHz	68.250 MHz	CVT Red. Blanking	AddDMT	3/4/03
	60 Hz	47.8 kHz	79.500 MHz	CVT	AddDMT	3/4/03
	75 Hz	60.3 kHz	102.250 MHz	CVT	AddDMT	3/4/03
	85 Hz	68.6 kHz	117.500 MHz	CVT	AddDMT	3/4/03
1280 x 960	60 Hz	60.0 kHz	108.000 MHz	VESA Standard	VDMTPROP	3/1/96
	85 Hz	85.9 kHz	148.500 MHz	VESA Standard	VDMTPROP	3/1/96
1280 x 1024	60 Hz	64.0 kHz	108.000 MHz	VESA Standard	VDMTREV	12/18/96
	75 Hz	80.0 kHz	135.000 MHz	VESA Standard	VDMT75HZ	10/4/93
	85 Hz	91.1 kHz	157.500 MHz	VESA Standard	VDMTPROP	3/1/96
1360 x 768	60 Hz	47.7 kHz	85.500 MHz	VESA Standard	AddDMT	3/4/03
1400 x 1050	60 Hz	64.7 kHz	101.000 MHz	CVT Red. Blanking	AddDMT	5/13/03
	60 Hz	65.3 kHz	121.750 MHz	CVT	AddDMT	3/4/03
	75 Hz	82.3 kHz	156.000 MHz	CVT	AddDMT	3/4/03
	85 Hz	85.0 kHz	179.500 MHz	CVT	AddDMT	3/4/03
1440 x 900	60 Hz	55.5 kHz	88.750 MHz	CVT Red. Blanking	CVT 1.30MA	7/14/04
	60 Hz	59.9 kHz	106.500 MHz	CVT	CVT 1.30MA	7/14/04
	75 Hz	75.0 kHz	136.750 MHz	CVT	CVT 1.30MA	7/14/04
	85 Hz	84.8 kHz	157.000 MHz	CVT	CVT 1.30MA	7/14/04
1600 x 1200	60 Hz	75.0 kHz	162.000 MHz	VESA Standard	VDMTREV	12/18/96
	65 Hz	81.3 kHz	175.500 MHz	VESA Standard	VDMTREV	12/18/96
	70 Hz	87.5 kHz	189.000 MHz	VESA Standard	VDMTREV	12/18/96
	75 Hz	93.8 kHz	202.500 MHz	VESA Standard	VDMTREV	12/18/96
	85 Hz	106.3 kHz	229.500 MHz	VESA Standard	VDMTREV	12/18/96
1680 x 1050	60 Hz	64.7 kHz	119.000 MHz	CVT Red. Blanking	CVT 1.76MA	7/14/04
	60 Hz	65.3 kHz	146.250 MHz	CVT	CVT 1.76MA	7/14/04
	75 Hz	74.9 kHz	187.000 MHz	CVT	CVT 1.76MA	7/14/04
	85 Hz	93.9 kHz	214.75 MHz	CVT	CVT 1.76MA	7/14/04
1792 x 1344	60 Hz	83.64 kHz	204.750 MHz	VESA Standard	VDMTREV	9/17/98
1856 x 1392	60 Hz	86.33 kHz	218.250 MHz	VESA Standard	VDMTREV	9/17/98
1920 x 1200	60 Hz	74.0 kHz	154.000 MHz	CVT Red. Blanking	AddDMT	3/4/03
	60 Hz	74.6 kHz	193.250 MHz	CVT	AddDMT	3/4/03
	75 Hz	94.0 kHz	245.250 MHz	CVT	AddDMT	3/4/03
1920 x 1440	60 Hz	90.000 kHz	234.000 MHz	VESA Standard	VDMTREV	9/17/98

Table 2. Video clock table for TV devices

Field Rate	VIC	Hactive	Vactive	I/P	Htotal	Hblank	Vtotal	Vblank	H Freq (kHz)	V Freq (Hz)	Pixel Freq (MHz)
Low	60	1280	720	Prog	3300	2020	750	30	18.000	24.000	59.400
	61	1280	720	Prog	3960	2680	750	30	18.750	25.000	74.250
	62	1280	720	Prog	3300	2020	750	30	22.500	30.000	74.250
	32	1920	1080	Prog	2750	830	1125	45	27.000	24.000	74.250
	33	1920	1080	Prog	2640	720	1125	45	28.125	25.000	74.250
	34	1920	1080	Prog	2200	280	1125	45	33.750	30.000	74.250
50Hz	17,18	720	576	Prog	864	144	625	49	31.250	50.000	27.000
	19	1280	720	Prog	1980	700	750	30	37.500	50.000	74.250

	20	1920	1080	Int	2640	720	1125	22.5	28.125	50.000	74.250
	21,22	1440	576	Int	1728	288	625	24.5	15.625	50.000	27.000
	23,24	1440	288	Prog	1728	288	312	24	15.625	50.080	27.000
	23,24	1440	288	Prog	1728	288	313	25	15.625	49.920	27.000
	23,24	1440	288	Prog	1728	288	314	26	15.625	49.761	27.000
	25,26	2880	576	Int	3456	576	625	24.5	15.625	50.000	54.000
	27,28	2880	288	Prog	3456	576	312	24	15.625	50.080	54.000
	27,28	2880	288	Prog	3456	576	313	25	15.625	49.920	54.000
	27,28	2880	288	Prog	3456	576	314	26	15.625	49.761	54.000
	29,30	1440	576	Prog	1728	288	625	49	31.250	50.000	54.000
	31	1920	1080	Prog	2640	720	1125	45	56.250	50.000	148.500
	37,38	2880	576	Prog	3456	576	625	49	31.250	50.000	108.000
	39	1920	1080	Int	2304	384	1250	85	31.250	50.000	72.000
60Hz	1	640	480	Prog	800	160	525	45	31.469	59.940	25.175
	2,3	720	480	Prog	858	138	525	45	31.469	59.940	27.000
	4	1280	720	Prog	1650	370	750	30	45.000	60.000	74.250
	5	1920	1080	Int	2200	280	1125	22.5	33.750	60.000	74.250
	6,7	1440	480	Int	1716	276	525	22.5	15.734	59.940	27.000
	8,9	1440	240	Prog	1716	276	262	22	15.734	60.054	27.000
	8,9	1440	240	Prog	1716	276	263	23	15.734	59.826	27.000
	10,11	2880	480	Int	3432	552	525	22.51	15.734	59.940	54.000
	12,13	2880	240	Prog	3432	552	262	22	15.734	60.054	54.000
	12,13	2880	240	Prog	3432	552	263	23	15.734	59.826	54.000
	14,15	1440	480	Prog	1716	276	525	45	31.469	59.940	54.000
	16	1920	1080	Prog	2200	280	1125	45	67.500	60.000	148.500
	35,36	2880	480	Prog	3432	552	525	45	31.469	59.940	108.000
100Hz	40	1920	1080	Int	2640	720	1125	22.51	56.250	100.00	148.500
	41	1280	720	Prog	1980	700	750	30	75.000	100.00	148.500
	42,43	720	576	Prog	864	144	625	49	62.500	100.00	54.000
	44,45	1440	576	Int	1728	288	625	24.5	31.250	100.00	54.000
	64	1920	1080	Prog	2640	720	1125	45	112.500	100.00	297.000
120Hz	46	1920	1080	Int	2200	280	1125	22.5	67.500	120.00	148.500
	47	1280	720	Prog	1650	370	750	30	90.000	120.00	148.500
	48,49	720	480	Prog	858	138	525	45	62.937	119.88	54.000
	50,51	1440	480	Int	1716	276	525	22.5	31.469	119.88	54.000
	63	1920	1080	Prog	2200	280	1125	45	135.000	120.00	297.000
200Hz	52,53	720	576	Prog	864	144	625	49	125.000	200.00	108.00
	54,55	1440	576	Int	1728	288	625	24.5	62.500	200.00	108.00
240Hz	56,57	720	480	Prog	858	138	525	45	125.874	239.76	108.000
	58,59	1440	480	Int	1716	276	525	22.5	62.937	239.76	108.000

(CEC-861-E, March 2008)

Table 3. 4K x 2K video formats

HDMI_VIC	Description	Pixel Freq (MHz)	Hactive	Hblank	Vfreq (Hz)	Vactive	Vblank
0x01	4K x 2K 29.97, 30Hz	297.000 296.703	3840	560	30.000 29.970	2160	90
0x02	4K x 2K 25Hz	297.000	3840	1440	25.000	2160	90
0x03	4K x 2K 23.98, 24Hz	297.000 296.703	3840	1660	24.000 23.976	2160	90

0x04	4K x 2K 24Hz (SMPTE)	297.000	4096	1404	24.000	2160	90

(HDMI Specification Version 1.4a, March 4, 2010)

Table 4. DisplayPort to HDMI 3D video formats mapping and list

DisplayPort 3D Video Formats	HDMI 3D Video Formats
Stacked Frame	Framing packing
Frame Sequential	Framing packing
Pixel Interleaved (Line interleave only)	Line alternative
Side-by-Side (Full mode)	Side-by-Side (Full)

3D Structure	VIC	Description	Hactive	Hblank	Vactive	Vact_space	Vblank	Pixel freq (MHz)	V freq (Hz)
0000 Frame Packing	32	1080p, 23.98/24Hz	1920	830	1080	45	45	148.35/148.50	23.976/24.000
	4	720p, 59.94/60Hz	1280	370	720	30	30	148.35/148.50	59.940/60.000
	19	720p, 50Hz	1280	700	720	30	30	148.50	50.000
0010 Line alternative	16	1080p 60Hz	1920	280	1080	n.a.	45	297.00	60.000
	31	1080p 50Hz	1920	720	1080	n.a.	45	297.00	50.000
0011 Side-by-Side(Full)	16	1080p 60Hz	1920	280	1080	n.a.	45	297.00	60.000
	31	1080p 50Hz	1920	720	1080	n.a.	45	297.00	50.000

(HDMI Specification Version 1.4a, March 4, 2010)

Note: *All the supported 3D video formats in the mapping table can support all the timing data rates less than 3.0Gbps, and the timing list table only show some examples.*

POWER ON HARDWARE CONFIGURATION

The first configuration mechanism is through configuration pins as shown in Table 4.

Table 5. Power On Configuration

Configuration Signal	Purpose	Definition
GPIO0	Control I2C address selection	'0': 0x10h - 0x2Fh (default) '1': 0x90h – 0x9Fh, 0xD0h ~ 0xDFh
GPIO1	MPU / I2C select	'0': Use MPU to control PS171 (default) '1': Use control I2C to control PS171
IROMD	Firmware initial address	'0': Start from Bank 3 '1': Start from Bank 7

Another mechanism to achieve configuration is through external ROM. The master I2C has the option to load configuration data from external ROM after power up.

PIN ASSIGNMENT & DESCRIPTION

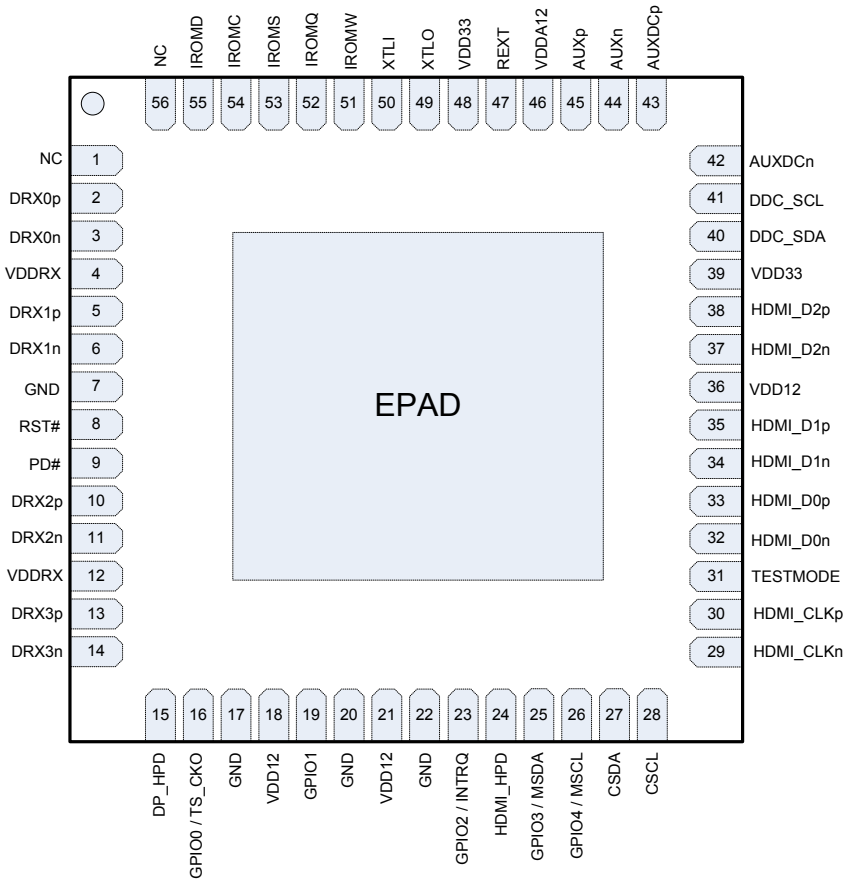


Figure3. PS171 Pin Assignment

Table 6. PS171 Pin Descriptions

Pin #	Pad Name	I/O Type	I/O Dir	Description
1	NC			Reserved
2	DRX0p	Analog	I	DP RX lane 0 positive
3	DRX0n	Analog	I	DP RX lane 0 negative
4	**VDDRX**			**DP power supply at 1.2V**
5	DRX1p	Analog	I	DP RX lane 1 positive
6	DRX1n	Analog	I	DP RX lane 1 negative
7	**GND**			**Ground**
8	RST#	Schmitt	I	Reset, active low, 3.3V input Internal pull-up at ~100kΩ
9	PD#	Schmitt	I	Power down, active low, 3.3V input Internal pull-up at ~100kΩ
10	DRX2p	Analog	I	DP RX lane 2 positive
11	DRX2n	Analog	I	DP RX lane 2 negative
12	**VDDRX**			**DP power supply at 1.2V**
13	DRX3p	Analog	I	DP RX lane 3 positive
14	DRX3n	Analog	I	DP RX lane 3 negative
15	DP_HPD	LVTTL	O	DP Rx hot plug detection output
16	GPIO0 / TS_CKO	LVTTL	I/O	General purpose I/O 0 Internal pull-down at ~80kΩ
		CMOS	O	DP test Clock output
17	**GND**			**Ground**
18	**VDD12**			**Core power supply at 1.2V**
19	GPIO1	LVTTL	I/O	General purpose I/O Internal pull-down at ~80kΩ
20	**GND**			**Ground**
21	**VDD12**			**Core power supply at 1.2V**
22	**GND**			**Ground**
23	GPIO2 / INTRQ	LVTTL	I/O	General purpose I/O Internal pull-down at ~80kΩ
		Schmitt, OD		Interrupt request
24	HDMI_HPD	LVTTL	I	HDMI Tx hot plug detection input 5V tolerant
25	GPIO3 / MSDA	LVTTL	I/O	General purpose I/O Internal pull-down at ~80kΩ
		Schmitt, OD		Master I2C data
26	GPIO4 / MSCL	LVTTL	I/O	General purpose I/O Internal pull-down at ~80kΩ

		Schmitt, OD		Master I2C clock
27	CSDA	Schmitt, OD	I/O	Control I2C slave data
28	CSCL	Schmitt, OD	I/O	Control I2C slave clock
29	HDMI_CLKn	Analog	O	HDMI Tx clock channel negative
30	HDMI_CLKp	Analog	O	HDMI Tx clock channel positive
31	TESTMODE	Schmitt	I	Test mode control, NC for normal operation
32	HDMI_D0n	Analog	O	HDMI Tx data channel 0 negative
33	HDMI_D0p	Analog	O	HDMI Tx data channel 0 positive
34	HDMI_D1n	Analog	O	HDMI Tx data channel 1 negative
35	HDMI_D1p	Analog	O	HDMI Tx data channel 1 positive
36	**VDD12**			**Core power supply at 1.2V**
37	HDMI_D2n	Analog	O	HDMI Tx data channel 2 negative
38	HDMI_D2p	Analog	O	HDMI Tx data channel 2 positive
39	**VDD33**			**I/O power supply at 3.3V**
40	DDC_SDA	Schmitt, OD	I/O	HDMI/DVI DDC data, 5V tolerant
41	DDC_SCL	Schmitt, OD	I/O	HDMI/DVI DDC clock, 5V tolerant
42	AUXDCn	Analog	I	DP source detection
43	AUXDCp	Analog	I	DP source detection
44	AUXn	Analog	I/O	DP AUX CH differential negative
45	AUXp	Analog	I/O	DP AUX CH differential positive
46	**VDDA12**			**Analog power supply at 1.2V**
47	REXT	Analog	I/O	Connect to a 4.99kΩ, 1% precision resistor to ground.
48	**VDD33**			**I/O power supply at 3.3V**
49	XTLO	Analog	O	Crystal out
50	XTLI	Analog	I	Crystal input or reference clock input.
51	IROMW	LVTTL	O	Firmware write protection Internal pull-down at ~80kΩ
52	IROMQ	LVTTL	I	Firmware ROM data input Internal pull-down at ~80kΩ
53	IROMS	LVTTL	O	Firmware ROM chip select Internal pull-up at ~100kΩ
54	IROMC	LVTTL	O	Firmware ROM clock output Internal pull-down at ~80kΩ
55	IROMD	LVTTL	O	Firmware ROM data output Internal pull-down at ~80kΩ
56	NC			Reserved
	EPAD			Connected to Ground

ABSOLUTE MAXIMUM RATINGS

Parameters	Comments	Min	Typ	Max	Unit
Supply Voltage Range:					
VDD33		-0.5		4	V
VDD12, VDDA12, VDDRX		-0.5		1.45	V
Normal I/O Voltage Range		-0.5		4	V
5V Safe I/O Voltage Range	DDC_SCL, DDC_SDA, HDMI_HPD	-0.5		6	V
T_J	Junction temperature			125	°C
T_S	Storage temperature	-40		150	°C
ESD	Human Body Model		+/- 8000		V
	Machine Model		+/- 400		V
	Charged Device Model		+/- 2000		V

ESD Standard:

Human Body Mode: JESD22-A114-D

Machine Mode: JESD22-A115-A

Charged Device Mode: JESD22-C101-A

Latch-up Standard: JESD78; I-Test: +/- 200 mA; V-Test: 1.5X of Vcc

NORMAL OPERATING CONDITIONS AND POWER CONSUMPTIONS

Parameter	Min	Typ	Max	Unit
Supply Voltage:				
VDD33	3.0	3.3	3.6	V
VDD12, VDDA12, VDDRX	1.14	1.2	1.26	V
Operation Temperature:				
Ta - Ambient Temperature	0		70	°C
Tc - Case Temperature	0		85	°C
Supply Current				
I_{DD33} (current @ 3.3V)		5	7	mA
I_{DD12} (current @ 1.2V) at 1080p & 8-bit color depth				
2-lane 2.7Gbps receiving, HDMI output 1.485Gbps		264	330	mA
I_{DD12} (current @ 1.2V) at 1080p & 12-bit color depth				
4-lane 2.7Gbps receiving, HDMI output 2.25Gbps		328	410	mA
I_{DD12} (current @ 1.2V) at 1080p@60Hz 3D format, 2.97Gbps				
4-lane 2.7Gbps receiving, HDMI output 2.97Gbps		374	468	mA
Power Consumption				
1080p with 8-bit color depth, 1.485Gbps		333	441	mW
1080p with 12-bit color depth, 2.25Gbps		410	542	mW
1080p@60Hz 3D format, 2.97Gbps		465	615	mW
Standby Power Consumption AUX channel is active for Link handshaking communication Cable connected, DPCD 600h=02h or RESET asserted			73	mW
Power Down Power Consumption Pin PD# is asserted			5	mW

PACKAGE DISSIPATION RATINGS

56-pin QFN	Still air, 4-layer PCB
θ_{JA} - Junction to Ambient Thermal Resistance	25.5 °C/W
θ_{JC} - Junction to Case Thermal Resistance	11.6 °C/W
Maximum Power Dissipation Rating, Ta = 70 °C	2157 mW

I/O DC CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
I2C pins:						
CSCL/CSDA, MSCL/MSDA						
V_{OH}	High-level output voltage	External 1.5 kΩ pull-up to		VDD33		V
V_{OL}	Low-level output voltage	VDD33, I_{OL} = 8 mA			0.4	V
SPI pins:						
IROMD, IROMC, IROMS, IROMQ, IROMW						
V_{IH}	LVCMOS input High-level voltage		0.7VDD33			V
V_{IL}	LVCMOS input Low-level voltage				0.25VDD33	V
V_{OH}	High-level output voltage	I_{OL} = 4 mA, I_{OH} = -4 mA	0.8VDD33			V
V_{OL}	Low-level output voltage				0.15VDD33	V
Control input pin: RST#, PD#						
V_{IH}	Input High-level voltage		0.7VDD33			V
V_{IL}	Input Low-level voltage				0.25VDD33	V
Status I/O pins: GPIOx (x= 0~4)						
V_{OH}	High-level output voltage		0.8VDD33			V
V_{OL}	Low-level output voltage				0.15VDD33	V

I/O AC CHARACTERISTICS

Parameter		Test Conditions	Min	Typ[2]	Max	Unit
Supply ramp up time:						
(both supplies ramp at the same starting point)						
$t_{3.3}$	3.3V supply ramp up time	10% to 90% of the 3.3V supply voltage			+10	ms
$t_{1.2}$	1.2V supply ramp up time	10% to 90% of the 1.2V supply voltage			+10	ms
dt	VDD33 and VDD12 power ramp up separation	Time difference between the mid points of VDD33 and VDD12	-10		+10	ms
Status output pins: GPIOx (x=0~4)						
t_r	Output rise time	CL = 10 pF			6	ns
t_f	Output fall time				6	ns
SPI pins: IROMx						
t_{HI}	Clock high time		9			ns
t_{LO}	Clock low time		9			ns
t_{SETUP}	Data in setup time reference to clock rising edge		5			ns
t_{HOLD}	Data in hold time reference to clock rising edge		5			ns
t_V	Data out valid time reference to clock falling edge				9	ns
t_{HO}	Data out hold time reference to clock falling edge		0			ns
t_{CSS}	Chip select setup time reference to clock rising edge		25			ns
t_{CSH}	Chip select hold time reference to clock falling edge		10			ns
Hot plug detection pin: DP_HPD						
	IRQ HPD pulse width (driven by sink device)		0.5		1.0	ms

POWER UP AND RESET TIMING SEQUENCE

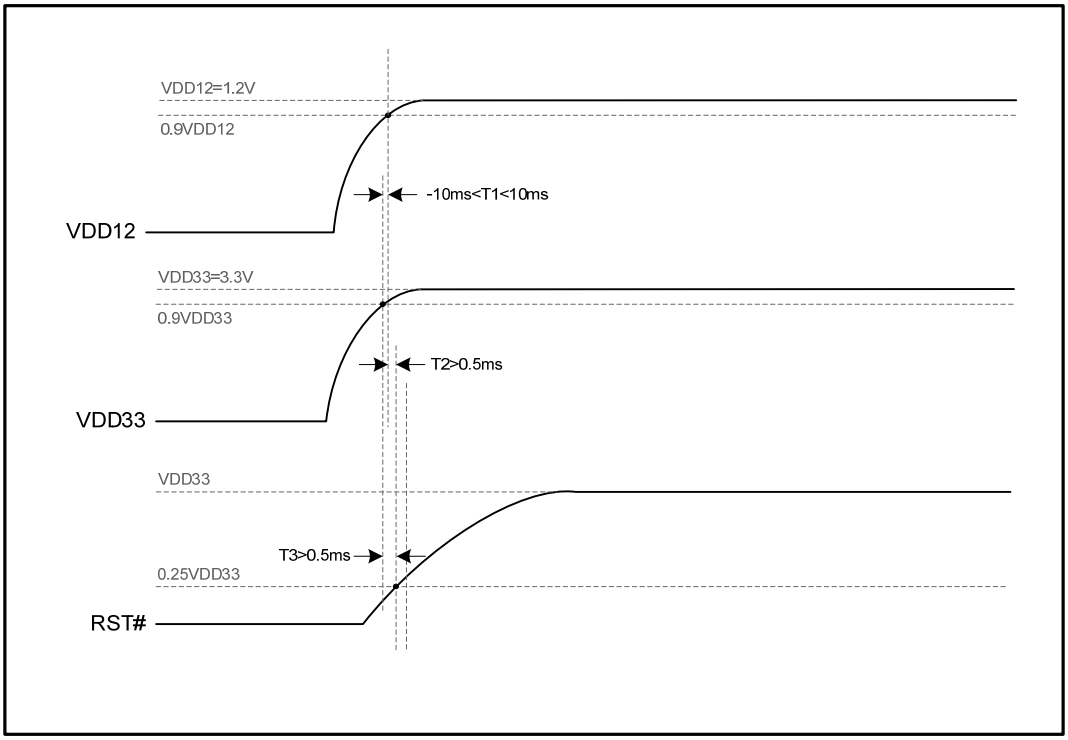


Figure4. Power Up and Reset Timing Sequence

Note: The de-assertion of the RST# shall follow by the timing sequence as given in the above diagram.

DISPLAYPORT™ AUX CHANNEL CHARACTERISTICS

Symbol and Parameter	Test Conditions	Min	Typ	Max	Unit
UI: Unit Interval for AUX channel		0.4	0.5	0.6	µs
$V_{AUX-DIFF-p-p}$: AUX differential peak-to-peak voltage at TP1 When AUX CH is driving the bus		400		900	mV
$V_{AUX-DIFF-p-p}$: AUX differential peak-to-peak voltage at TP2 When AUX CH is receiving the bus		320		1360	mV
$V_{AUX-DC-CM-RX}$: AUX common mode voltage when receiving			VDD12		V
$V_{AUX-DC-CM-TX}$: AUX common mode voltage when transmitting			VDD12-0.3		V
$I_{AUX-SHORT}$: AUX channel short circuit current				20	mA
C_{AUX}: AUX AC coupling capacitor		75		200	nF

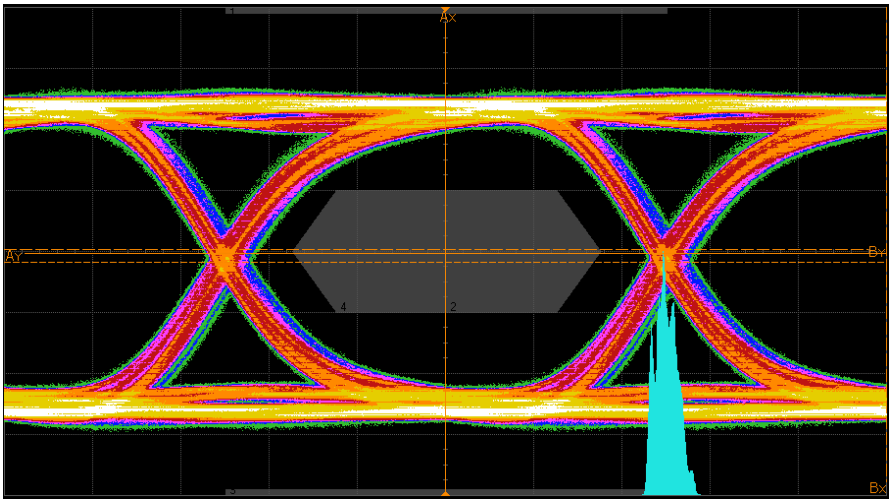
DISPLAYPORT™ MAIN LINK RECEIVER CHARACTERISTICS

Symbol and Parameter	Test Conditions	Min	Typ	Max	Unit
Spread spectrum clock, down-spreading by SOURCE			0.5		%
Modulation frequency		30		33	kHz
$V_{RX\text{-}DIFFp\text{-}p}$: Differential peak-to-peak input voltage at package pins		100		1360	mV
Maximum adaptive RX equalization level at 1.35GHz			9		dB
$V_{RX\_DC\_CM}$: RX input DC common mode voltage			GND		V
$R_{RX\text{-}DIFF}$: Differential termination resistance		80	100	120	Ω
$R_{RX\text{-}SE}$: Single-ended termination resistance		40	50	60	Ω
I_{RX_SHORT}: Rx short circuit current limit				20	mA
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (HBR)				150	ps
RX intra-pair skew tolerance at HBR					
$L_{RX\_SKEW\_INTRA\_PAIR}$: Intra-pair skew at Rx package pins (RBR)				300	ps
RX intra-pair skew tolerance at RBR					
Receiver Jitter Tolerance for High Bit Rate (HBR)					
Total jitter tolerance at 2MHz		1227			mUI
Total jitter tolerance at 10MHz		548			mUI
Total jitter tolerance at 20MHz		505			mUI
Total jitter tolerance at 100MHz		491			mUI
Receiver Jitter Tolerance for Reduced Bit Rate (RBR)					
Total jitter tolerance at 2MHz		1648			mUI
Total jitter tolerance at 10MHz		778			mUI
Total jitter tolerance at 20MHz		747			mUI
Note: Jitter Tolerance Testing follows *VESA DisplayPort™ PHY Compliance Testing Standard, Version 1.1a.*					

HDMI/DVI TRANSMITTER CHARACTERISTICS

Symbol and Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OD}	Peak-to-peak differential output swing	AVcc = 3.3V, RT = 50 Ω	800	1000	1200	mV
V_{OH}	Single end high-level output voltage	Clock > 165MHz	AVcc-200		AVcc+10	mV
V_{OL}	Single end low-level output voltage		AVcc-700		AVcc-400	mV
t_r	differential output rise time	AVcc = 3.3V, RT = 50 Ω	90		166	ps
t_f	differential output fall time		90		166	ps
t_{sk_intra}	intra-pair differential skew				0.15	T_{bit}
t_{sk_inter}	inter-pair differential skew				0.50	T_{bit}
$t_{CK\text{-}jitter}$	output clock jitter	With 4MHz clock recovery bandwidth defined in HDMI CTS			0.25	T_{bit}
$t_{DATA\text{-}jitter}$	output data jitter				0.30	T_{bit}

Typical 3Gbps HDMI Output Eye Diagram



MEASUREMENT INFORMATION

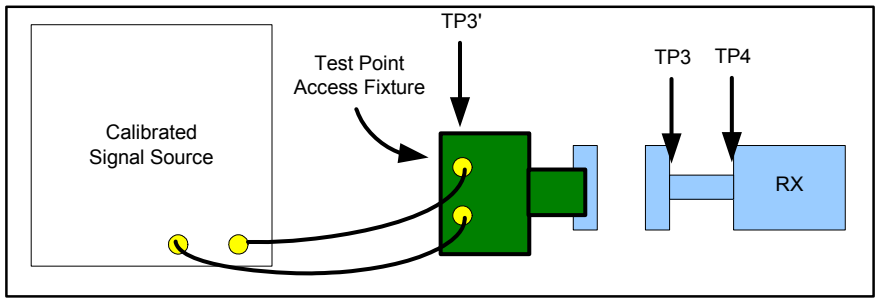


Figure5. Measurement Setup for DisplayPort Sink Device

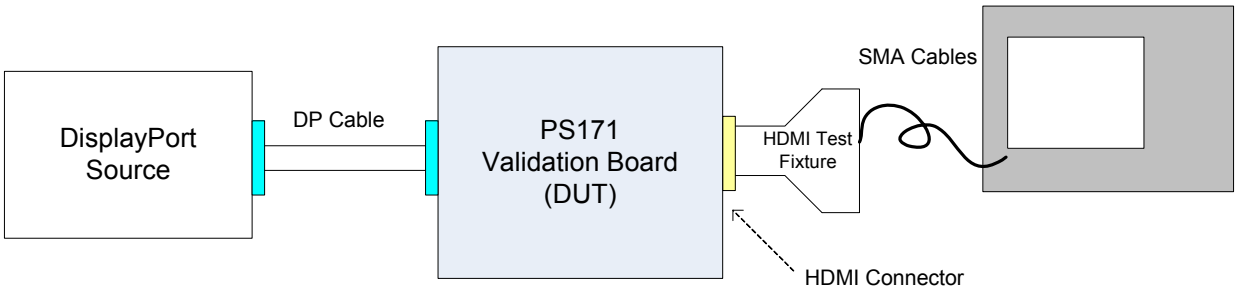


Figure6. Measurement Setup for HDMI Source Device

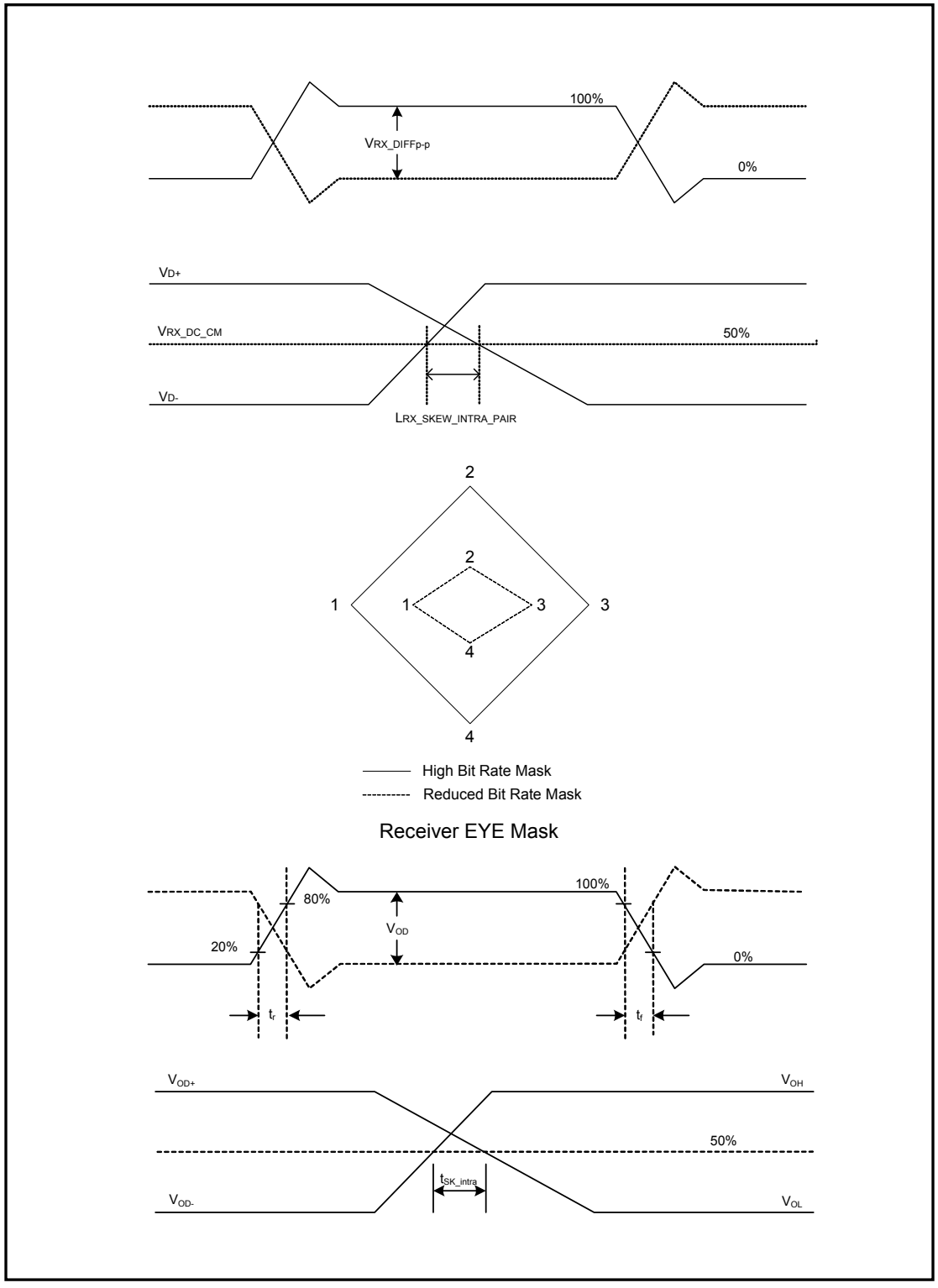


Figure7. Definition of Key Parameters

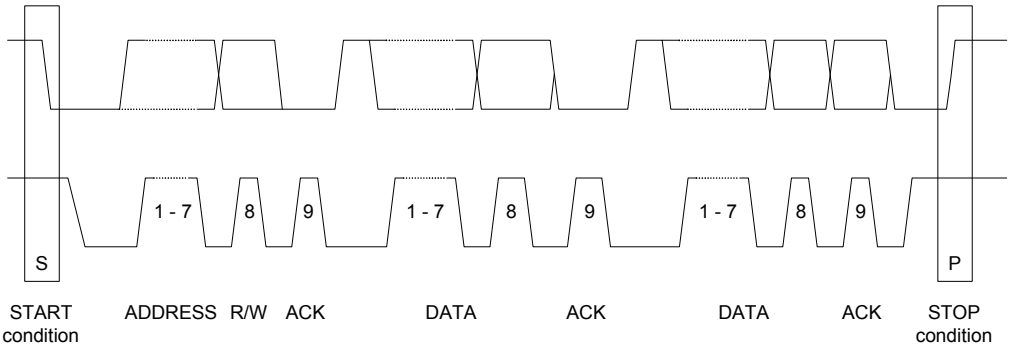


Figure8. I2C Complete Data Transfer

S	SLAVE ADDRESS	W#	A	INDEX ADDRESS (n)	A	S	SLAVE ADDRESS	R	A	DATA(n)	A/A#	P

I2C Read Command

S	SLAVE ADDRESS	W#	A	INDEX ADDRESS (n)	A	DATA(n)	A	DATA(n+1)	A/A#	P

I2C Write Command

From Master to Slave

From Slave to Master

S: START condition
P: STOP condition
A: Acknowlegde (SDA Low)
A#: not acknowledge (SDA High)
W#: Write command (SDA Low)
R: Read command (SDA High)
Slave Address: 7 bits
Index Address: 8 bits, index n
Data: 8 bits, reference to index n

Figure9. I2C Read and Write Command

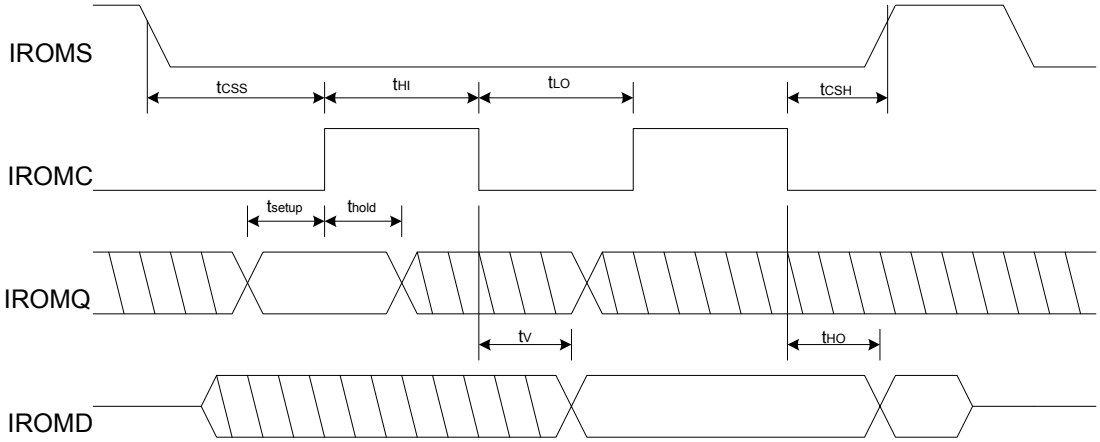


Figure10. SPI Interface Timing

LAYOUT GUIDELINES

High Speed Interfaces

- Select proper PCB stack up and trace width for 100 ohm differential transmission line impedance for high speed DisplayPort™ main link and AUX channels
- Avoid tight bend for differential signals
- Match intra-pair and inter-pair traces length within each differential pair
- Keep uninterrupted ground plane beneath differential signals
- Keep wide and shortest traces for both power and ground path to PS171

Filtering Capacitors

- Place 0.1uF capacitors on all VDD33, VDD12, VDDA12 and VDDRX power pins. These capacitors shall be placed as close as possible to the chip package pins
- Place additional 0.01uF capacitor on the VDD12, VDDA12 and VDDRX pins. These capacitors shall be placed as close as possible to the chip package pins

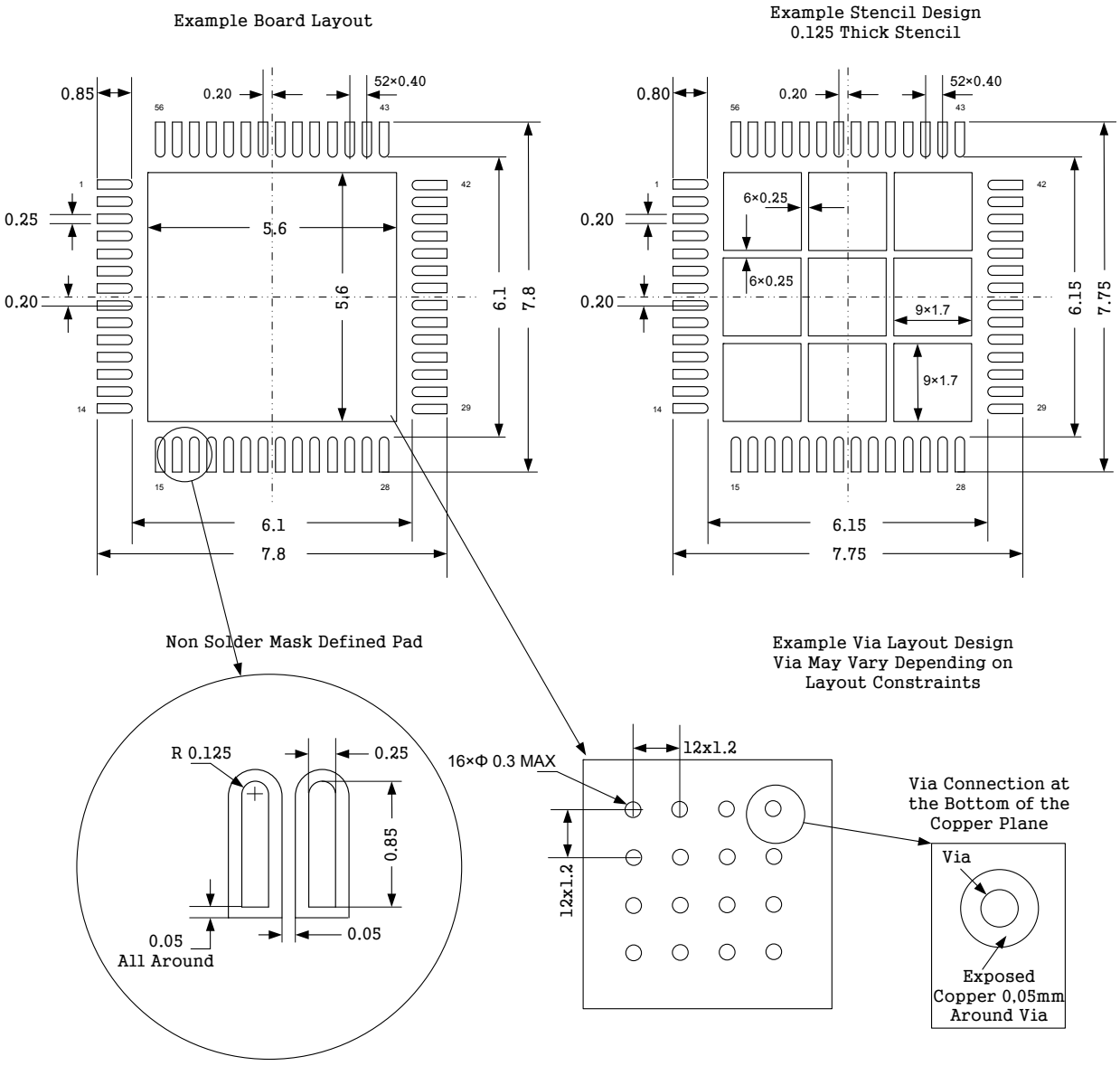


Figure11. The Exposed Thermal Pad Layout Guidelines

NOTES:

1. All dimensions are in millimeters.
2. The drawing is subject to change without notice.
3. Customers should contact their board fabrication site for recommend solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

ORDER & PACKAGING INFORMATION

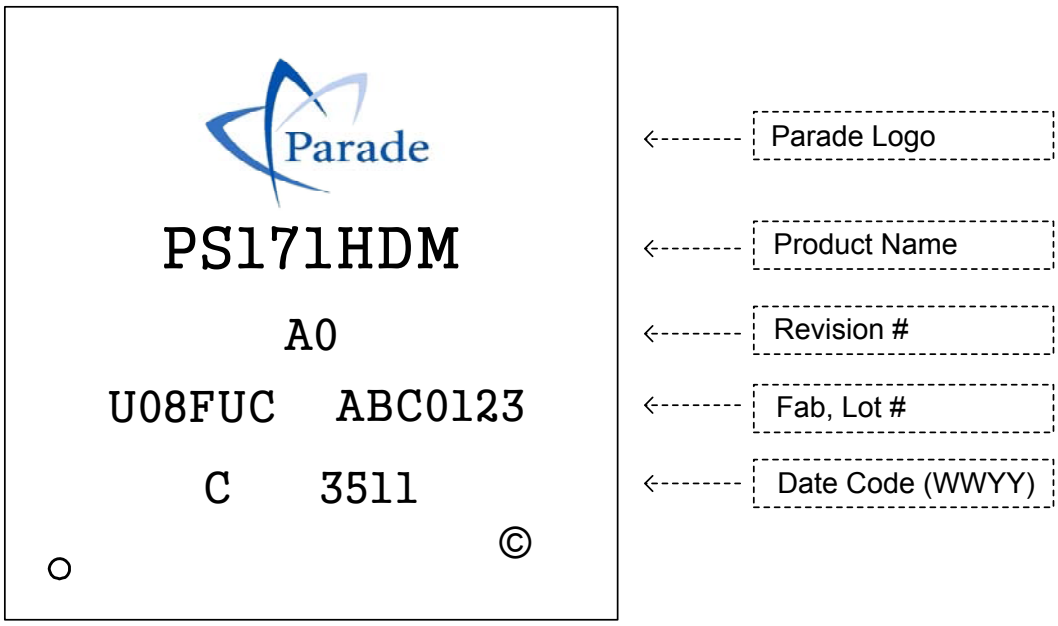
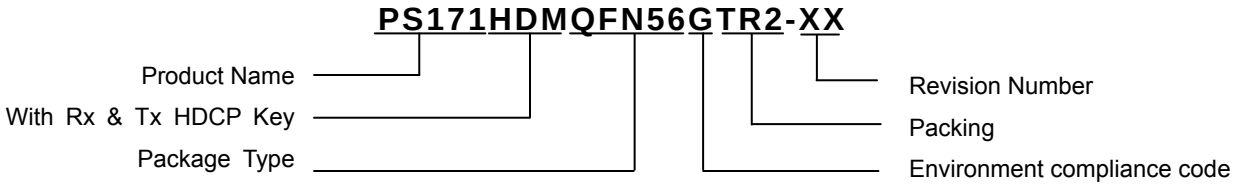


Figure12. Top Side Marking

Order Information:

Part number:

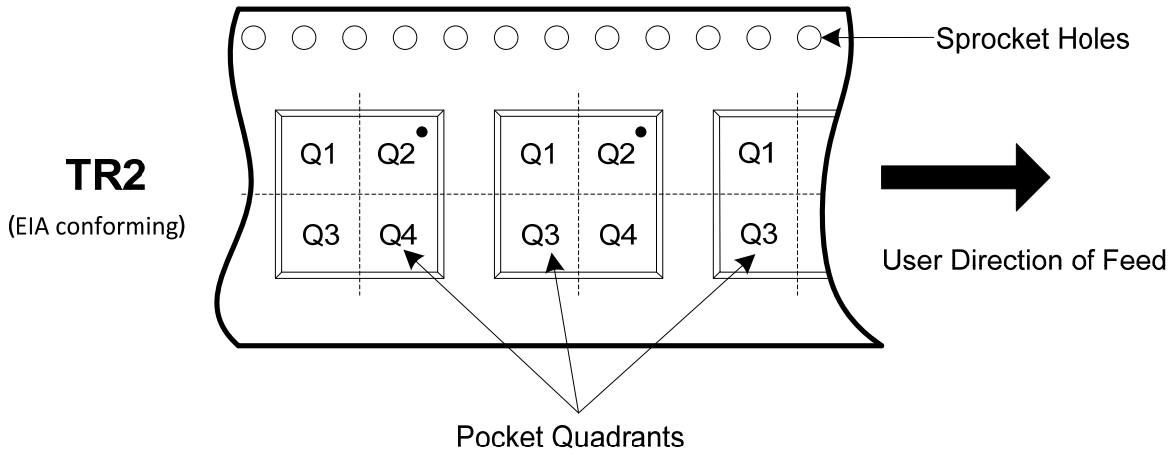


Part Number		Packing
PS171HDMQFN56G-XX	(Rx & Tx key)	Tray
PS171HDMQFN56GTR2-XX	(Rx & Tx key)	Tape and Reel (EIA conforming)

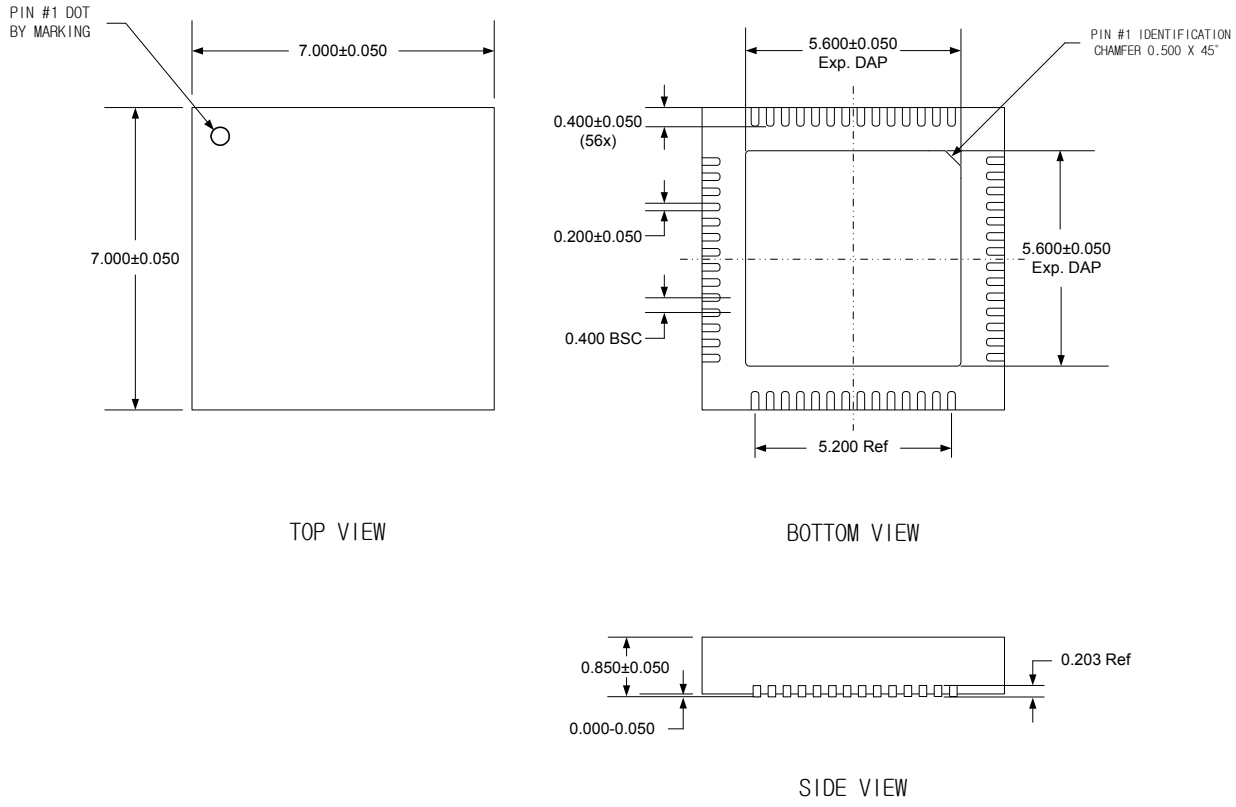
Lead Finish: 100% Sn

TAPE AND REEL PACKING PIN1 ORIENTATION

QUADRANT ASSIGNMENT FOR PIN1 ORIENTATION IN TAPE



PHYSICAL DIMENSIONS



NOTES:

1. All dimensions are in mm. Angles in degrees.
2. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
3. Refer JEDEC M0-220 modified.