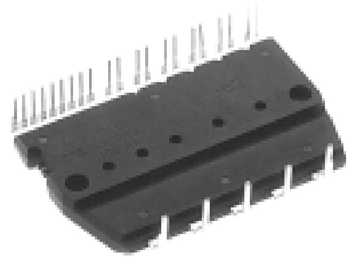
PS21343-N

TRANSFER-MOLD TYPE
INSULATED TYPE

PS21343-N



INTEGRATED POWER FUNCTIONS

600V/10A low-loss 4th generation (planar) IGBT inverter bridge for 3 phase DC-to-AC power conversion.

INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

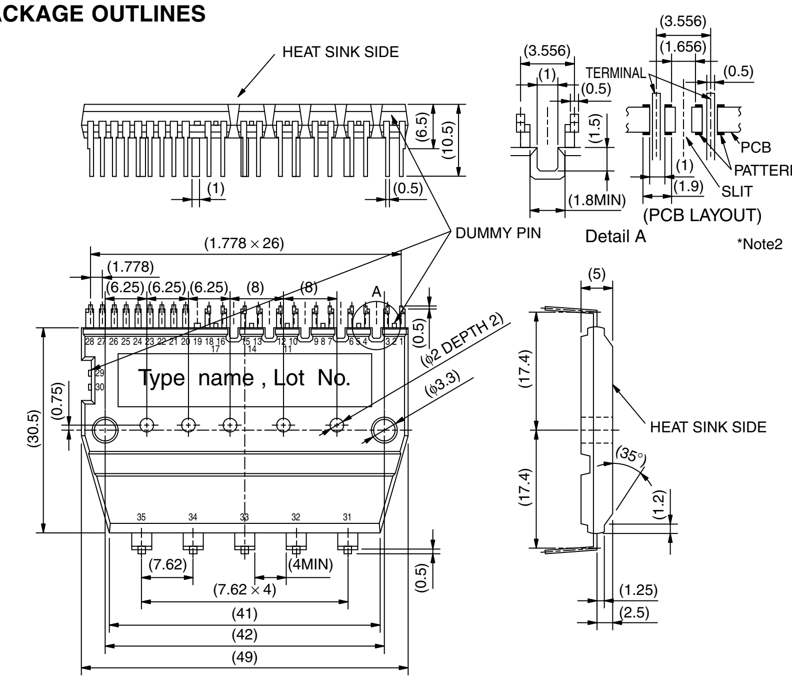
- For upper-leg IGBTs : Drive circuit, High voltage isolated high-speed level shifting, Control circuit under-voltage (UV) protection.
  Note : Bootstrap supply scheme can be applied.
- For lower-leg IGBTs : Drive circuit, Control circuit under-voltage protection (UV), Short-circuit protection (SC).
- Fault signaling : Corresponding to a SC fault (Low-side IGBT) or a UV fault (Low-side IGBT).
- Input interface : 5V line CMOS/TTL compatible, Schmitt Trigger receiver circuit.

APPLICATION

AC100V~200V inverter drive for motor control.

Fig. 1 PACKAGE OUTLINES

Dimensions in mm



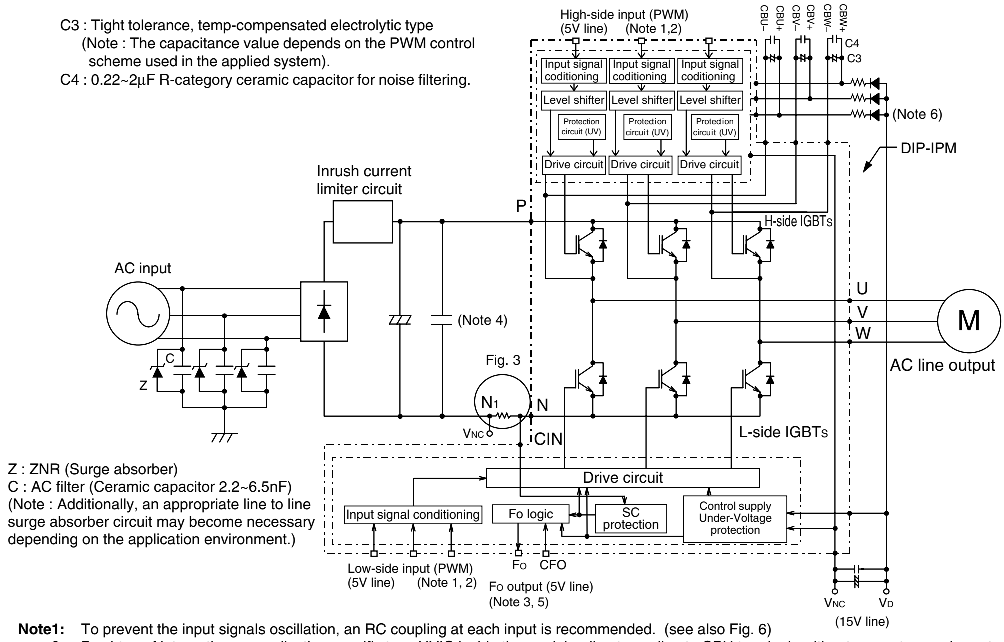
TERMINAL CODE

1	VUFS
2	(UPG)
3	VUFB
4	VP1
5	(COM)
6	UP
7	VVFS
8	(VPG)
9	VVFB
10	VP1
11	(COM)
12	VP
13	VWFS
14	(WPG)
15	VWFB
16	VP1
17	(COM)
18	WP
19	(UNG)
20	VNO(NC)
21	UN
22	VN
23	WN
24	FO
25	CFO
26	CIN
27	VNC
28	VN1
29	(WNG)
30	(VNG)
31	P
32	U
33	V
34	W
35	N

*Note1:(***) = Dummy Pin.

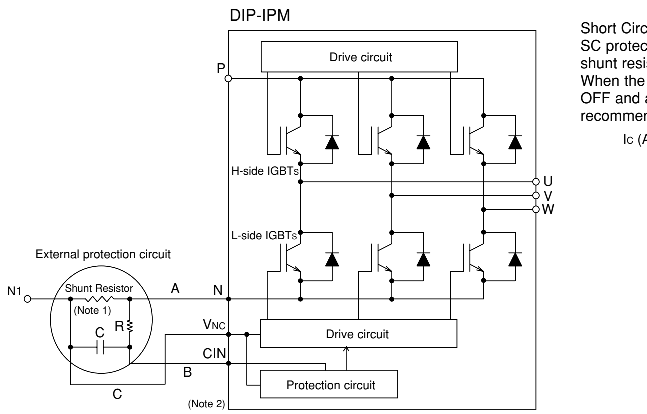
*Note 2: In order to increase the surface distance between terminals, cut a slit, etc. on the PCB surface when mounting a module.

Fig. 2 INTERNAL FUNCTIONS BLOCK DIAGRAM (TYPICAL APPLICATION EXAMPLE)

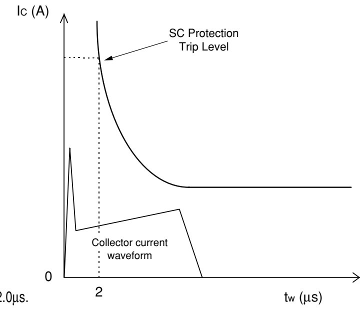


Note1: To prevent the input signals oscillation, an RC coupling at each input is recommended. (see also Fig. 6)
2: By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible. (see also Fig. 6)
3: This output is open collector type. The signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1kΩ resistance. (see also Fig. 6)
4: The wiring between the power DC link capacitor and the P/N1 terminals should be as short as possible to protect the DIP-IPM against catastrophic high surge voltages. For extra precaution, a small film type snubber capacitor (0.1~0.22µF, high voltage type) is recommended to be mounted close to these P and N1 DC power input terminals.
5: Fo output pulse width should be decided by connecting external capacitor between CFO and VNC terminals. (Example : C_{FO}=22nF → t_{FO}=1.8ms (Typ.))
6: High voltage (600V or more) and fast recovery type (less than 100ns) diodes should be used in the bootstrap circuit.

Fig. 3 EXTERNAL PART OF THE DIP-IPM PROTECTION CIRCUIT



Short Circuit Protective Function (SC) :
SC protection is achieved by sensing the L-side DC-Bus current (through the external shunt resistor) after allowing a suitable filtering time (defined by the RC circuit).
When the sensed shunt voltage exceeds the SC trip-level, all the L-side IGBTs are turned OFF and a fault signal (Fo) is output. Since the SC fault may be repetitive, it is recommended to stop the system when the Fo signal is received and check the fault.



Note1: In the recommended external protection circuit, please select the RC time constant in the range 1.5~2.0µs.
2: To prevent erroneous protection operation, the wiring of A, B, C should be as short as possible.

MAXIMUM RATINGS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V_{CC}	Supply voltage	Applied between P-N	450	V
$V_{CC(surge)}$	Supply voltage (surge)	Applied between P-N	500	V
V_{CES}	Collector-emitter voltage		600	V
$\pm I_C$	Each IGBT collector current	T_f = 25°C	10	A
$\pm I_{CP}$	Each IGBT collector current (peak)	T_f = 25°C, instantaneous value (pulse)	20	A
P_C	Collector dissipation	T_f = 25°C, per 1 chip	25	W
T_j	Junction temperature	(Note 1)	–20~+150	°C

Note 1 : The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150°C (@ $T_f \le$ 100°C). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \le$ 125°C (@ $T_f \le$ 100°C).

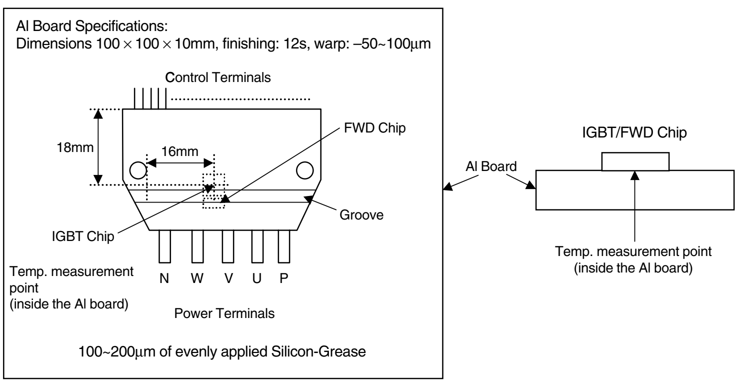
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	20	V
V_{CIN}	Input voltage	Applied between U_P, V_P, W_P-V_{NC}, U_N, V_N, W_N-V_{NC}	–0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	–0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	15	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	–0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
$V_{CC(PROT)}$	Self protection supply voltage limit (short-circuit protection capability)	V_D = V_{DB} = 13.5~16.5V, Inverter part T_j = 125°C, non-repetitive, less than 2 μs	400	V
T_f	Heat-fin operation temperature	(Note 2)	–20~+100	°C
T_{stg}	Storage temperature		–40~+125	°C
V_{iso}	Isolation voltage	60Hz, Sinusoidal, 1 minute, connection pins to heat-sink plate	1500	V_{rms}

Note 2 : T_f MEASUREMENT POINT



THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits Min.	Typ.	Max.	Unit
$R_{th(j-f)Q}$	Junction-to-heat sink thermal resistance	Inverter IGBT part (per 1/6 module) (Note 3)	—	—	5.0	°C/W
$R_{th(j-f)F}$		Inverter FWD part (per 1/6 module) (Note 3)	—	—	6.5	°C/W

Note 3 : Grease with good thermal conductivity should be applied evenly about +100µm~+200µm on the contact surface of a DIP-IPM and a heat sink.

ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition		Limits Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_D = V_{DB}$ = 15V	I_C = 10A, T_j = 25°C	—	1.55	2.15	V
		V_{CIN} = 0V	I_C = 10A, T_j = 125°C	—	1.65	2.25	V
V_{EC}	FWD forward voltage	T_j = 25°C, $-I_C$ = 10A, V_{CIN} = 5V		—	2.1	2.85	V
t_{on}	Switching times	V_{CC} = 300V, $V_D = V_{DB}$ =15V I_C = 10A, T_j = 125°C Inductive load (upper-lower arm) $V_{CIN} = 5 \leftrightarrow 0V$		0.40	0.90	1.35	µs
t_{rr}				—	0.20	—	µs
$t_{c(on)}$				—	0.40	0.65	µs
t_{off}				—	1.2	1.65	µs
$t_{c(off)}$				—	0.6	1.3	µs
I_{CES}	Collector-emitter cut-off current	$V_{CE} = V_{CES}$	T_j = 25°C	—	—	1	mA
			T_j = 125°C	—	—	10	mA

CONTROL (PROTECTION) PART

Symbol	Parameter	Condition		Limits Min.	Typ.	Max.	Unit
I_D	Circuit current	$V_D = V_{DB}$ =15V V_{CIN} = 5V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	8.5	mA
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	—	—	1.0	mA
		$V_D = V_{DB}$ =15V V_{CIN} = 0V	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	—	—	9.7	mA
			V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	—	—	1.0	mA
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O = 10kΩ 5V pull-up		4.9	—	—	V
V_{FOL}		V_{SC} = 0V, I_{FO} = 1.5mA		—	0.6	0.9	V
V_{FOsat}		V_{SC} = 1V, I_{FO} = 15mA		0.8	1.2	1.8	V
$V_{SC(ref)}$	Short-circuit trip level	T_j = 25°C, V_D = 15V (Note 4)		0.43	0.48	0.53	V
UV_{DBt}	Supply circuit under-voltage protection	$T_j \leq$ 125°C	Trip level	10.0	—	12.0	V
UV_{DBr}			Reset level	10.5	—	12.5	V
UV_{Dt}			Trip level	10.3	—	12.5	V
UV_{Dr}			Reset level	10.8	—	13.0	V
t_{FO}	Fault output pulse width	C_{FO} = 22nF (Note 5)		1.0	1.8	—	ms
$V_{th(on)}$	ON threshold voltage	Applied between: U_P, V_P, W_P-V_{NC}, U_N, V_N, W_N-V_{NC}		0.8	1.4	2.0	V
$V_{th(off)}$	OFF threshold voltage			2.5	3.0	4.0	V

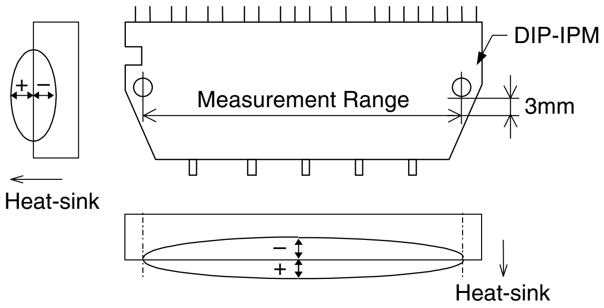
Note 4 : Short-circuit protection operates only at the low-arms. Please select the value of the external shunt resistor such that the SC trip level is less than 17A

5 : Fault signal is outputted when the low-arm short-circuit or control supply under-voltage protective functions operate. The fault output pulse-width t_{FO} depends on the capacitance value of C_{FO} according to the following approximate equation. : $C_{FO} = (12.2 \times 10^{-6}) \times t_{FO}$ [F]

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw : M3	—	0.59	0.78	0.98	N·m
Terminal pulling strength	Weight 9.8N	EIAJ-ED-4701	10	—	—	s
Bending strength	Weight 4.9N. 90deg bend	EIAJ-ED-4701	2	—	—	times
Weight		—	—	20	—	g
Heat-sink flatness	(Note 6)	—	–50	—	100	µm

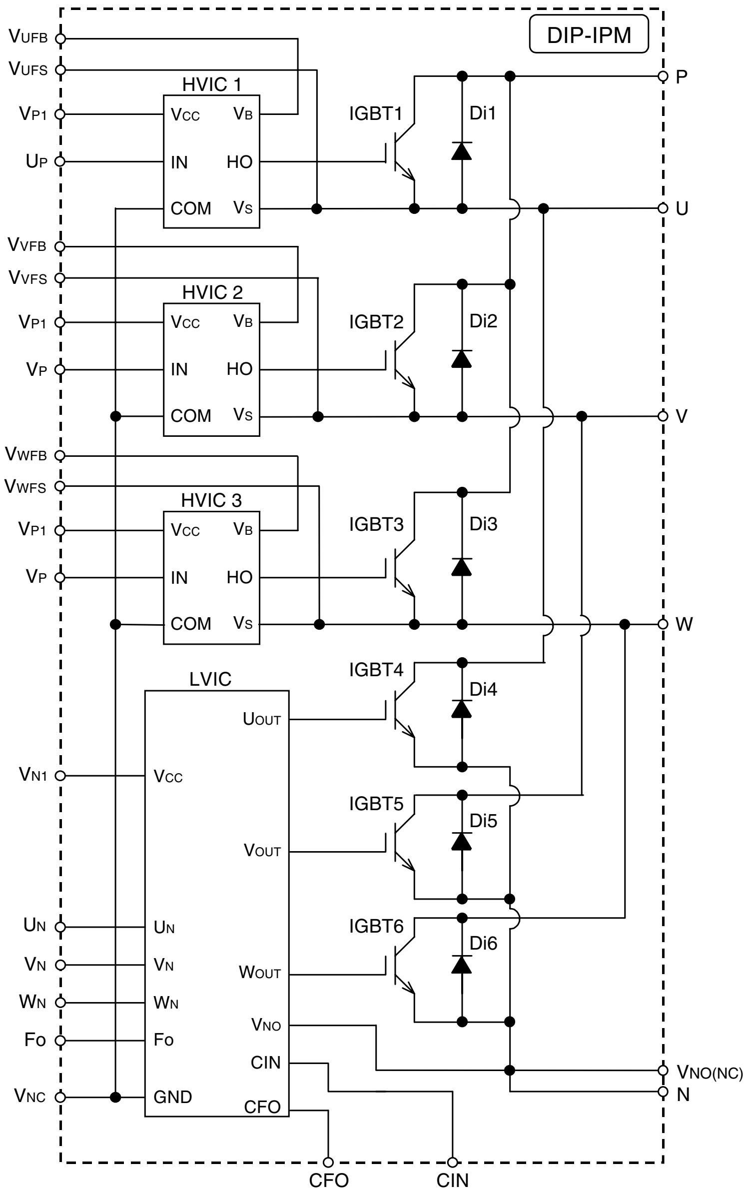
Note 6: Measurement point of heat-sink flatness



RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition	Limits Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	Applied between P-N	0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-V_{UFS}, V_{VFB}-V_{VFS}, V_{WFB}-V_{WFS}	13.5	15.0	16.5	V
ΔV_D, ΔV_{DB}	Control supply variation		–1	—	1	V/µs
t_{dead}	Arm shoot-through blocking time	For each input signal	1.5	—	—	µs
f_{PWM}	PWM input frequency	$T_j \leq 125°C$, $T_f \leq 100°C$	—	5	—	kHz
$V_{CIN(ON)}$	Input ON voltage	Applied between U_P, V_P, W_P-V_{NC}, U_N, V_N, W_N-V_{NC}	0~0.65			V
$V_{CIN(OFF)}$	Input OFF voltage		4.0~5.5			V

Fig. 4 THE DIP-IPM INTERNAL CIRCUIT

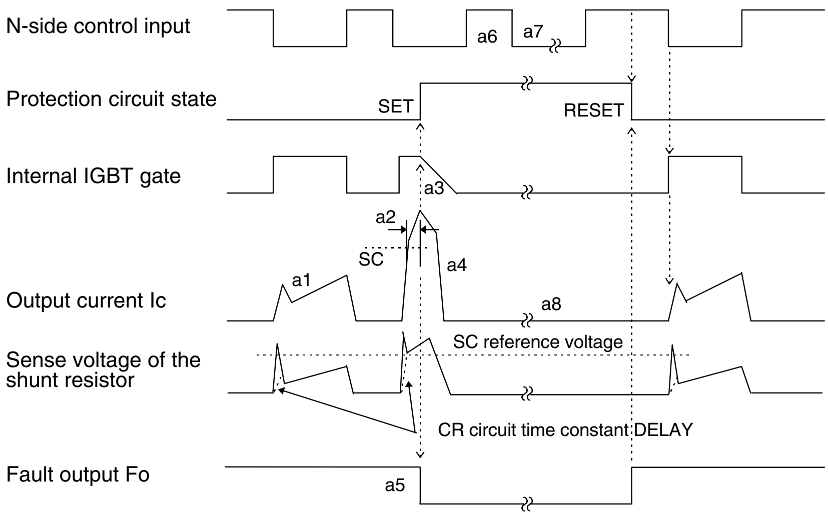


Note: The IGBTs gates and the HVICs COM terminals are connected to the dummy pins.

Fig. 5 TIMING CHARTS OF THE DIP-IPM PROTECTIVE FUNCTIONS

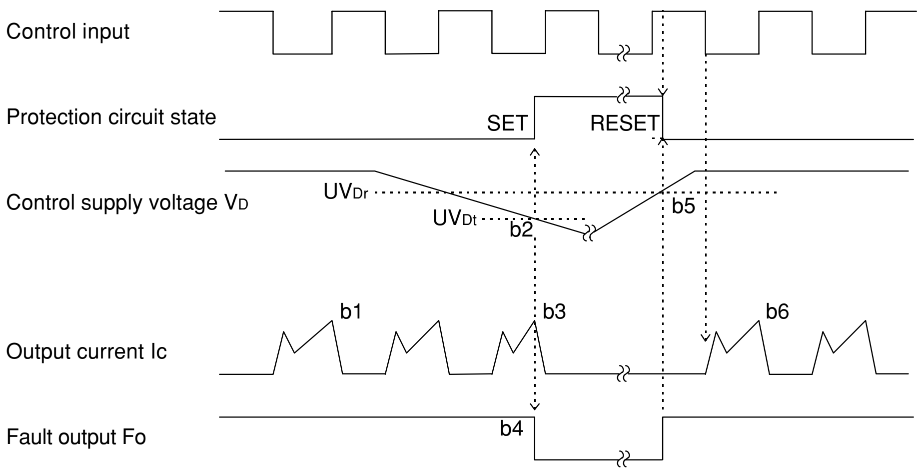
[A] Short-Circuit Protection (N-side only)

(For the external shunt resistor and CR connection, please refer to Fig. 3.)
a1. Normal operation : IGBT ON and carrying current.
a2. Short-circuit current detection (SC trigger).
a3. IGBT gate interrupt.
a4. IGBT turns OFF.
a5. FO timer operation starts : The pulse width of the FO signal is set by the external capacitor CFO.
a6. Input “H” : IGBT OFF state.
a7. Input “L” : IGBT ON state.
a8. IGBT OFF state.



[B] Under-Voltage Protection (N-side, UVD)

b1. Normal operation : IGBT ON and carrying current.
b2. Under-voltage trip (UVDt).
b3. IGBT OFF in spite of control input condition.
b4. FO timer operation starts.
b5. Under-voltage reset (UVDr).
b6. Normal operation : IGBT ON and carrying current.



[C] Under-Voltage Protection (P-side, UV_{DB})

c1. Control supply voltage rises : After the voltage level reachs UV_{DBr}, the circuits start to operate when the next input is applied.
c2. Normal operation : IGBT ON and carrying current.
c3. Under-voltage trip (UV_{DBt}).
c4. IGBT OFF in spite of control input condition (there is no F_O signal output).
c5. Under-voltage reset (UV_{DBr}).
c6. Normal operation : IGBT ON and carrying current.

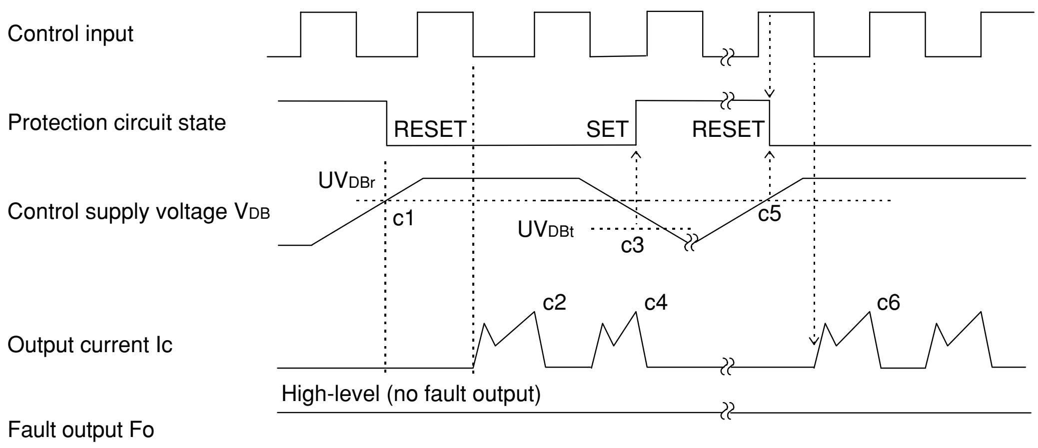
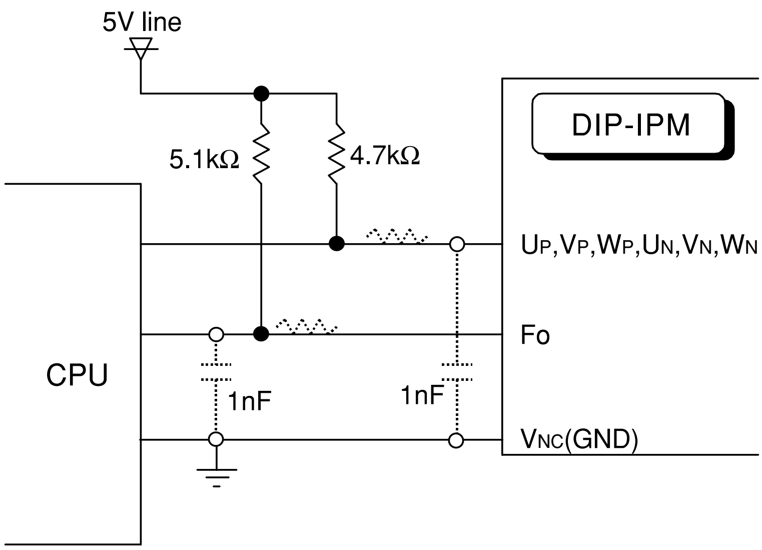


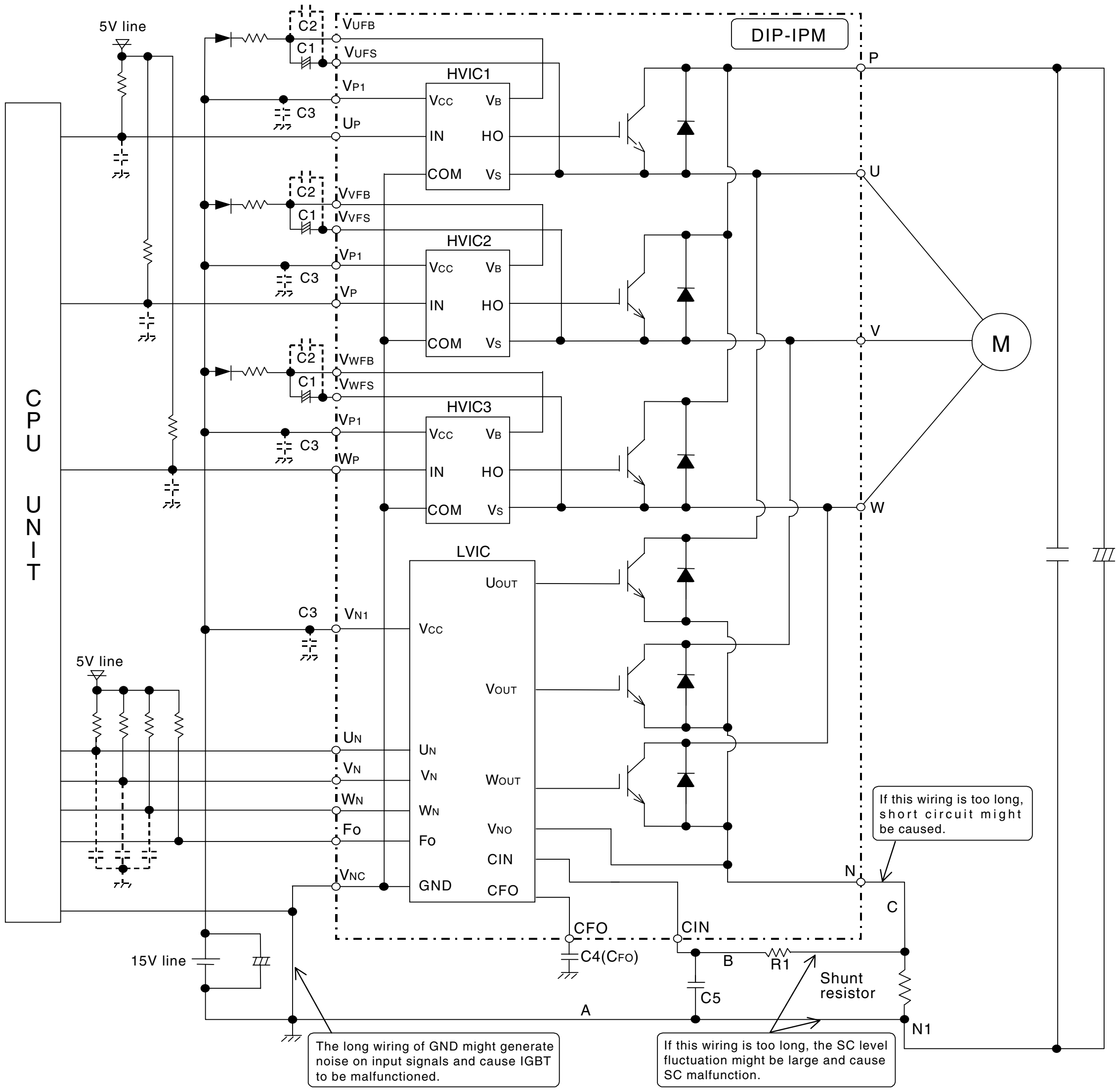
Fig. 6 RECOMMENDED CPU I/O INTERFACE CIRCUIT



Note : RC coupling at each input (parts shown dotted) may change depending on the PWM control scheme used in the application and on the wiring impedance of the application's printed circuit board.

Fig. 7 TYPICAL DIP-IPM APPLICATION CIRCUIT EXAMPLE

C1: Tight tolerance temp-compensated electrolytic type; C2,C3: 0.22~2 µ F R-category ceramic capacitor for noise filtering



Note 1 : To prevent the input signals oscillation, an RC coupling at each input is recommended, and the wiring of each input should be as short as possible (less than 2cm).

2 : By virtue of integrating an application specific type HVIC inside the module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3 : F_O output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 5.1kΩ resistance.

4 : F_O output pulse width should be decided by connecting an external capacitor between CFO and V_{NC} terminals (C_{FO}). (Example : C_{FO} = 22 nF → t_{FO} = 1.8 ms (typ.))

5 : Each input signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedances of the system's printed circuit board). Approximately a 0.22~2µF by-pass capacitor should be used across each power supply connection terminals.

6 : To prevent errors of the protection function, the wiring of A, B, C should be as short as possible.

7 : In the recommended protection circuit, please select the R_1C_5 time constant in the range of 1.5~2µs.

8 : Each capacitor should be put as nearby the terminals of the DIP-IPM as possible.

9 : To prevent surge destruction, the wiring between the smoothing capacitor and the P&N1 terminals should be as short as possible. Approximately a 0.1~0.22µF snubber capacitor between the P&N1 terminals is recommended.