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Phison Electronics Corporation

USB 2.0 Flash Controller Specification **PS2136**

version 1.2

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Revision History

Revision	History	Draft Date	Author
1.0	First Release.	25-Jul-06	Hughman
1.1	Modify typing error in Block Diagram, change ROM size from 48K to 64K.	11-Aug-06	David
1.2	Modify Electrical Specification.	26-Oct-07	David

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A. General Description

The PHISON's PS2136 micro-controller is the best choice for USB 2.0 & 1.1 Interface to NAND Flash Memory. This chip is specially designed for portable storage device or build-in to the PC / Notebook / IA system. It is pin compatible to PS2136.

By using this single chip solution, it will reduce a lot of efforts which was needed from R/D to production, as well as simplifying the RMA problems. With the USB plug & play function and driver-less solution with most of the operating systems, this solution provides not only easy to install, but also fast, easy to use and low cost way for user.

B. Controller Features

www.DataSheet4U.com **Ø Support Host Interfaces : USB 2.0 & 1.1 Interface**

Ø Support Flash Memory Interfaces : Build-in NAND Flash Memory

Ø USB Interface :

- Fully compatible with USB Specification Version 2.0 & 1.1
- High speed 480Mbit/second supporting
- Full speed 12Mbit/second supporting
- Support one CONTROL transfer, one INTERRUPT transfer and two BULK transfer
- Support four Endpoints :
 - u** Endpoint 0 : 64 Bytes CONTROL transfer
 - u** Endpoint 1 : 512*2 Bytes BULK transfer for IN transaction
 - u** Endpoint 2 : 512*2 Bytes BULK transfer for OUT transaction
 - u** Endpoint 3 : 64 Bytes INTERRUPT transfer for IN transaction

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- Support Data Payload
 - ⌋ Endpoint 0 : max 64 bytes
 - ⌋ Endpoint 1 : max 512 bytes
 - ⌋ Endpoint 2 : max 512 bytes
 - ⌋ Endpoint 3 : max 64 bytes
- Support USB power saving mode

Ø Build-In NAND Flash Memory Interface

- Build-in hardware ECC circuit (Hamming & Reed-Solomon).
- Support SLC (Single level cell) Small Block NAND Flash Memory.
- Support SLC (Single level cell) Large Block (2K+64 Bytes per page) NAND Flash Memory.
- Support MLC (Multi level cell) Small Block NAND flash.
- Support MLC (Multi level cell) Large Block NAND flash.

Main Feature		
SLC NAND Flash	Small Block	128Mb ~ 1Gb
	Large Block	1Gb ~ 16Gb
MLC NAND Flash	Small Block	512Mb ~ 4Gb
	Large Block	2Gb~32Gb
Toshiba NAND Flash support		Yes
Samsung NAND Flash support		Yes
Renesas NAND Flash support		Yes
ST NAND Flash support		Yes
Micron NAND Flash support		Yes
Hynix NAND Flash support		Yes
Infineon NAND Flash support		Yes
Number of NAND Flash support		4
High-speed 25MHz NAND Flash support		Yes
Flash IO mode support		1x8 / 2x8
Flash I/O voltage support		3.3v/1.8v

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Ø **Support External Flash ROM (EEPROM) for In-System Programming through**

USB Port : 0x0000h~0xFFFFh: 64KB

Ø **Transfer Rate for USB Interface:**

- “High speed” Up to 480Mbits/sec for USB 2.0
- “Full speed” Up to 12Mbits/sec for USB 1.1

Ø **Support 3.3V Flash I/O:**

Internal 3.3V regulator can supply current for controller analog circuit, controller I/O and Flash.

Ø **Support 1.8V Flash I/O:**

Internal 1.8V regulator can supply the current for controller core, controller I/O and Flash.

Ø **64-Pin QFP Package**

Ø **Operating Voltage: 2.7~3.6V.**

Ø **USB bus-powered capability.**

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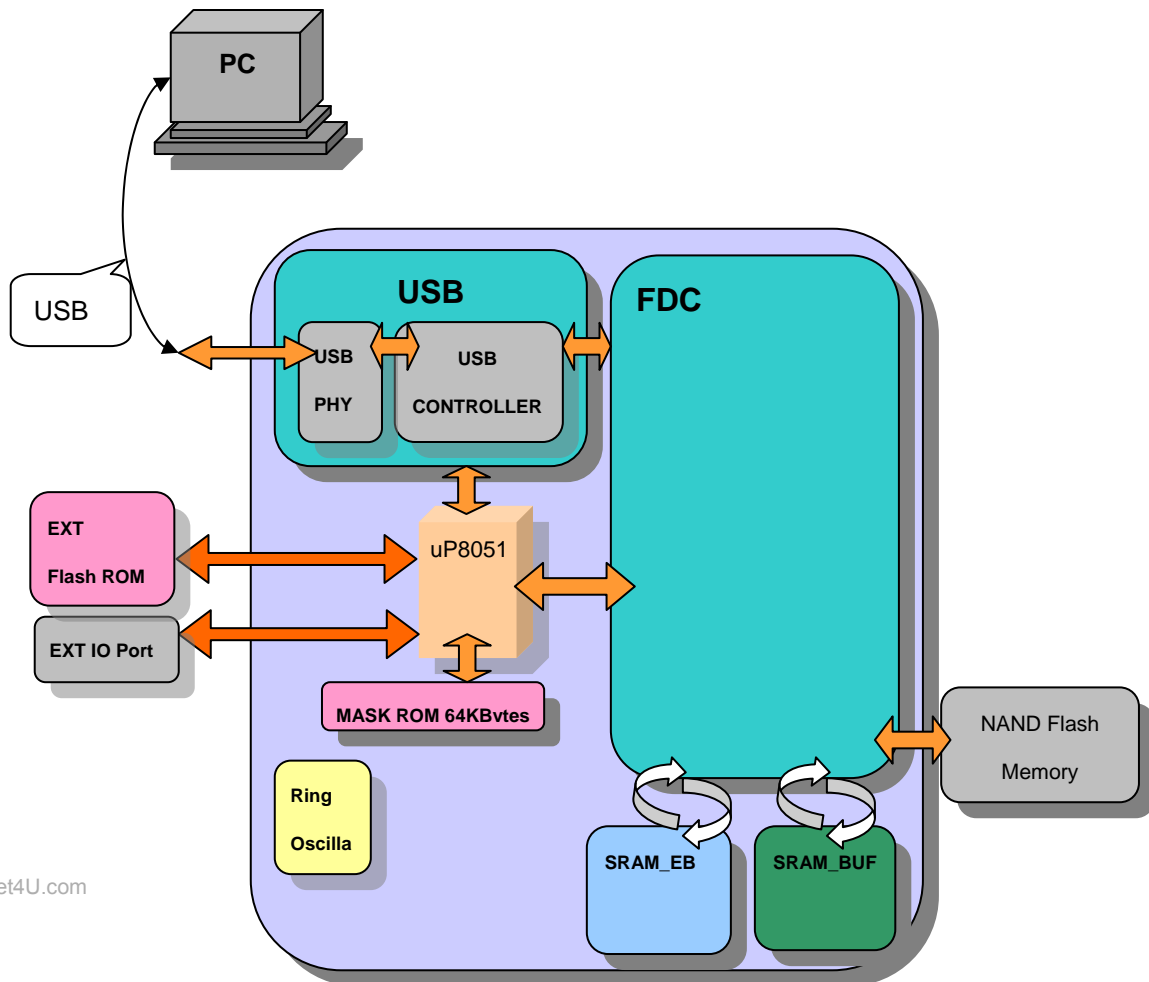
Ø **Power Saving implemented.**

Ø **Working Frequency: 12MHz.**

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C. BLOCK DIAGRAM

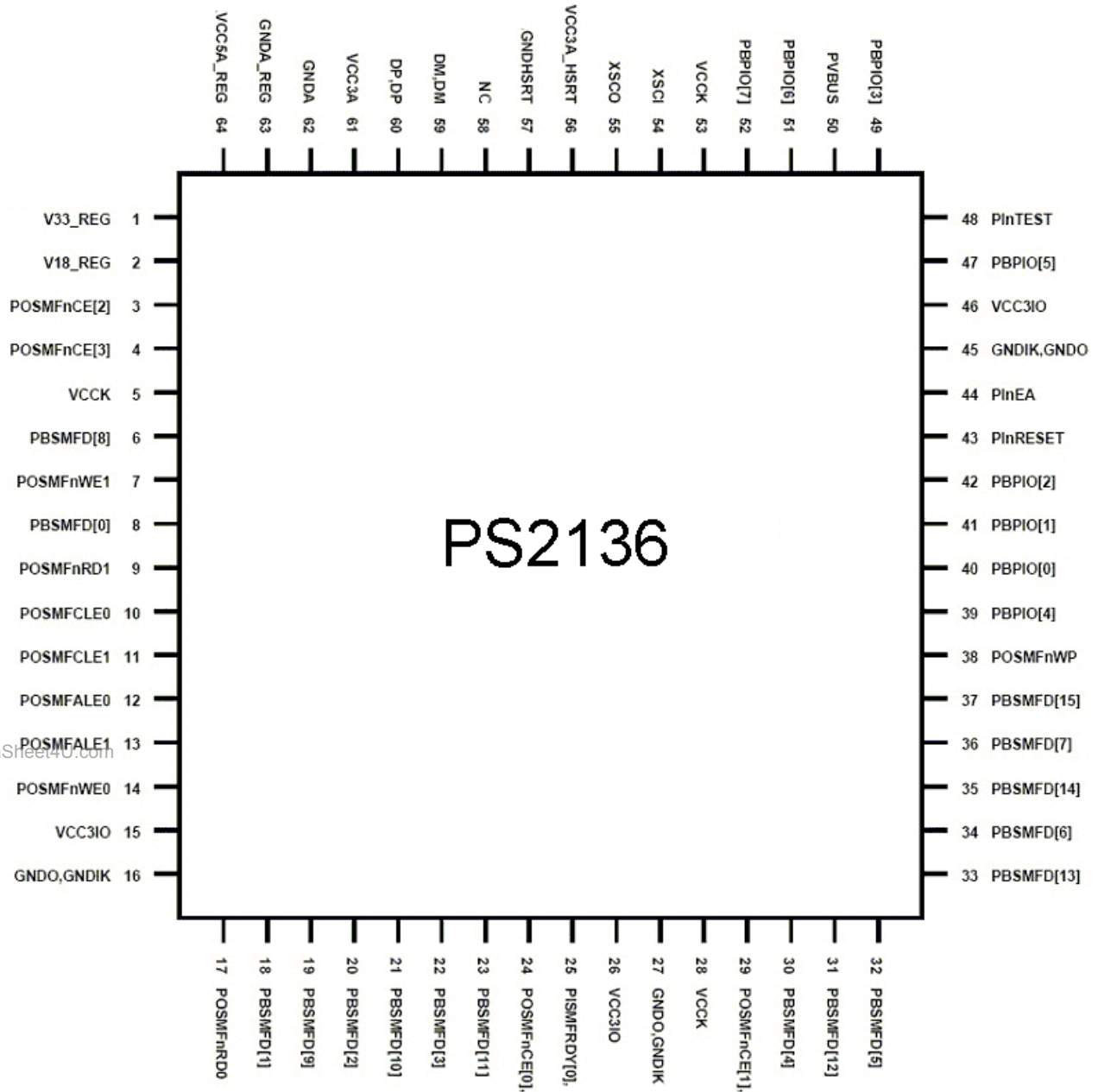


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D. Pin Assignment and Description

D1. Pin Assignment



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D2. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal
1	V33_REG	23	PBSMFD[11]	45	GNDIK
2	V18_REG	24	POSMFnCE[0]	46	VCC3IO
3	POSMFnCE[2]	25	PISMFRDY[0]	47	PBPIO[5]
4	POSMFnCE[3]	26	VCC3IO	48	PInTEST
5	VCCK	27	GND0,GNDIK	49	PBPIO[3]
6	PBSMFD[8]	28	VCCK	50	PVBUS
7	POSMFnWE1	29	POSMFnCE[1]	51	PBPIO[6]
8	PBSMFD[0]	30	PBSMFD[4]	52	PBPIO[7]
9	POSMFnRD1	31	PBSMFD[12]	53	VCCK
10	POSMFCLE0	32	PBSMFD[5]	54	XSCI
11	POSMFCLE1	33	PBSMFD[13]	55	XSCO
12	POSMFALE0	34	PBSMFD[6]	56	VCC3A_HSRT
13	POSMFALE1	35	PBSMFD[14]	57	GNDHSRT
14	POSMFnWE0	36	PBSMFD[7]	58	NC
15	VCC3IO	37	PBSMFD[15]	59	DM
16	GND0,GNDIK	38	POSMFnWP	60	DP
17	POSMFnRD0	39	PBPIO[4]	61	VCC3A
18	PBSMFD[1]	40	PBPIO[0]	62	GND A
19	PBSMFD[9]	41	PBPIO[1]	63	GND A_REG
20	PBSMFD[2]	42	PBPIO[2]	64	VCC5A_REG
21	PBSMFD[10]	43	PInRESET		
22	PBSMFD[3]	44	PInEA		

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D3. Pin Description

USB + Regulator Interface(13 Pins)			
No	Pin Name	Dir.	Pin Description
2	V18_REG	V18	1.8V (Regulator Digital Power output)
1	V33_REG	V33	3.3V (Regulator IO Power output)
64	VCC5A_REG	V50	5.0V
63	GND_A_REG	GND	
62	GND_A	GND	
61	VCC3A	V33	
60	DP	I/O	USB 2.0 data in positive pin terminal.
59	DM	I/O	USB 2.0 data in negative pin terminal.
58	NC		No connection
57	GND_HSRT	GND	
56	VCC3A_HSRT	VCC	
55	XSCO	O	Crystal oscillator output.
54	XSCI	I	Crystal oscillator input.
FLASH Interface(30 Pins)			
No	Pin Name	Dir.	Pin Description
24, 29, 3, 4	POSMFnCE[0:3]	I/O	Flash Chip Enable, Low active.
8, 18, 20, 22, 30, 32, 34, 36, 6, 19, 21, 23, 31, 33, 35, 37	PBSMFD[0:15]	I/O	Flash Data Bus
12, 13	POSMFnALE0, POSMFnALE1	O	Flash Address Latch Enable, High active.
10, 11	POSMFnCLE0, POSMFnCLE1	O	Flash Command Latch Enable, High active.
17, 9	POSMFnRD0, POSMFnRD1	O	Flash Read Control signal, Low active.
14, 7	POSMFnWE0, POSMFnWE1	O	Flash Write Control signal, Low active.
38	POSMFnWP	I/O	Flash Write Protect Control signal, Low active.
25	PISMFRDY[0]	I	Flash Ready/Busy signal.

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Global Signal(21 Pins)			
No	Pin Name	Dir.	Pin Description
43	PInRESET	I	Reset Signal
48	PInTEST	I	Test Mode Signal.
44	PInEA	I	EAMODE Select Signal.
50	PVBUS	I	
40, 41, 42, 49, 39, 47, 51, 52	PBPIO[0:7]	I/O	uP Port1[7:0]
15, 26, 46	VCC3IO	V33	3.3V (IO Power)
5, 28, 53	VCCK	V18	1.8V (Digital Power)
16, 27, 45	GNDIK, GNDO	GND	

E. System Power Consumption

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Item	Power Consumption (mA)	
	1 * Flash	2 * Flash
Idle	46.07	47.28
Suspend	0.32~0.40	0.32~0.40
Sleep	0.32~0.40	0.32~0.40
Read	58.26	63.77
Write	60.98	69.10
Un-configured	41.77	41.84
Configured	47.19	47.29

The above values are for reference only, it may change according to the flash memory used.

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F. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	$V_{DD}-V_{SS}$	DC Power Supply	-0.3	+5.5	V
2	V_{IN}	Input Voltage	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	T_a	Operating Temperature	0	+70	°C
4	T_{st}	Storage Temperature	-40	+85	°C

Parameter	Symbol	Min	Typ	MAX	Unit
Operating Temperature	T_a	0	+25	+70	°C
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

G. DC Characters

DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V _{CK}	Core Power Supply	Core Area	1.62	1.8	1.98	V
V _{CC3IO}	Power Supply	3.3V I/O	3.0	3.3	3.6	V
Temp	Junction Temperature		0	25	115	°C
V _t	Switching threshold	LVTTTL		1.5		V
V _{t-}	Schmitt Trigger Negative Going threshold voltage	LVTTTL	0.8	1.1		V
V _{t+}	Schmitt Trigger Positive Going threshold voltage			1.6	2.0	V
V _{ol}	Output Low voltage	I _{ol} = 2 ~ 16 mA			0.4	V
V _{oh}	Output High voltage	I _{oh} = 2 ~ 16 mA	$V_{CC3IO} - 0.4$			V
R _{pu}	Input Pull-Up Resistance	PU=high, PD=low	40	75	190	KΩ
R _{pd}	Input Pull-Down Resistance	PU=high, PD=low	40	75	190	KΩ
I _{in}	Input Leakage Current	V _{in} = V _{CC3I} or 0			1	μA
I _{oz}	Tri-state Output Leakage Current		-10	±1	10	μA

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H. AC Characters

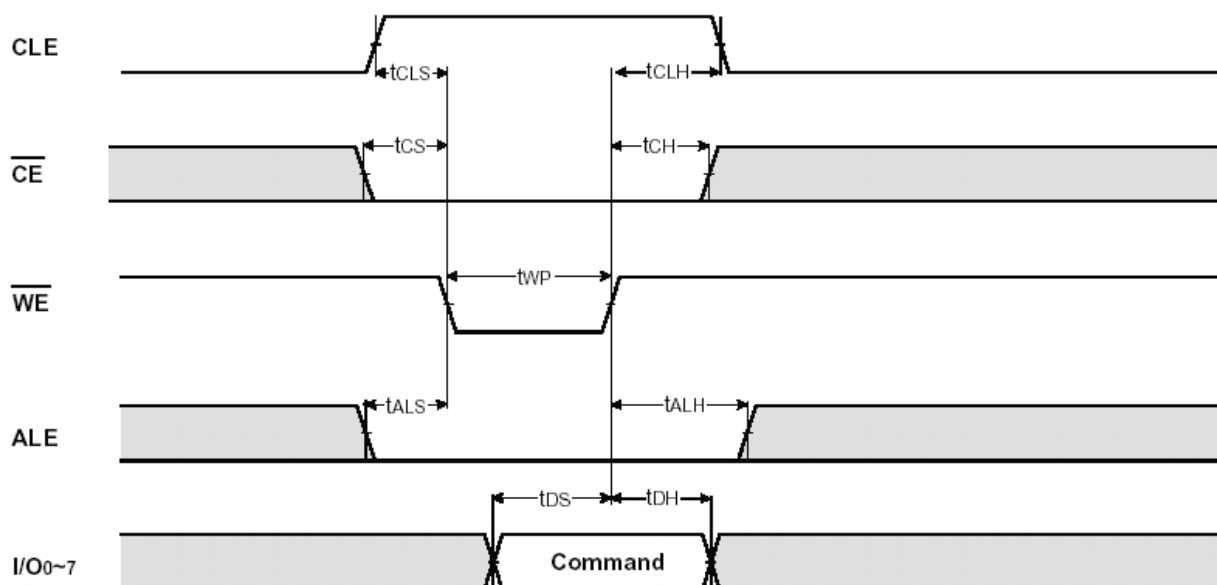
H1. Flash Memory Interface Timing

NAND Flash Memory Interface Timing

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
CE Setup Time	t_{CS}	0	-	ns
CE Hold Time	t_{CH}	10	-	ns
WE Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
WE High Hold Time	t_{WH}	15	-	ns
Read Cycle Time	t_{RC}	50	-	ns
/RE Pulse Width	t_{RP}	25	-	ns
/RE High Hold Time	t_{REH}	15	-	ns
Ready to /RE Low	t_{RR}	60	-	ns

H1.1 Command Latch Cycle

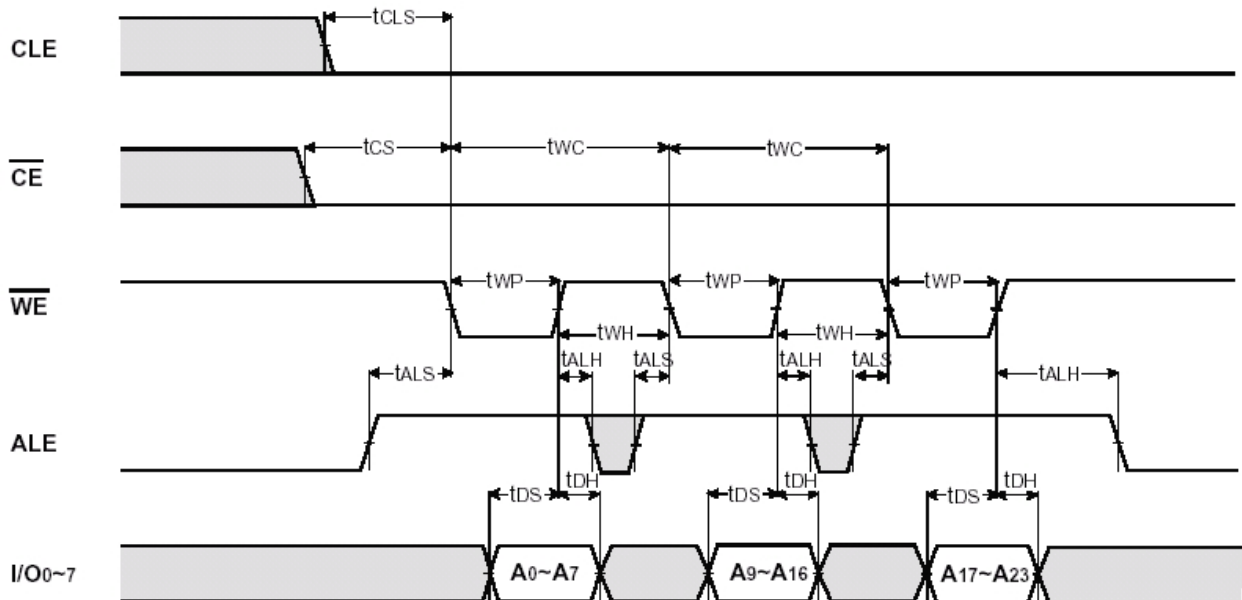
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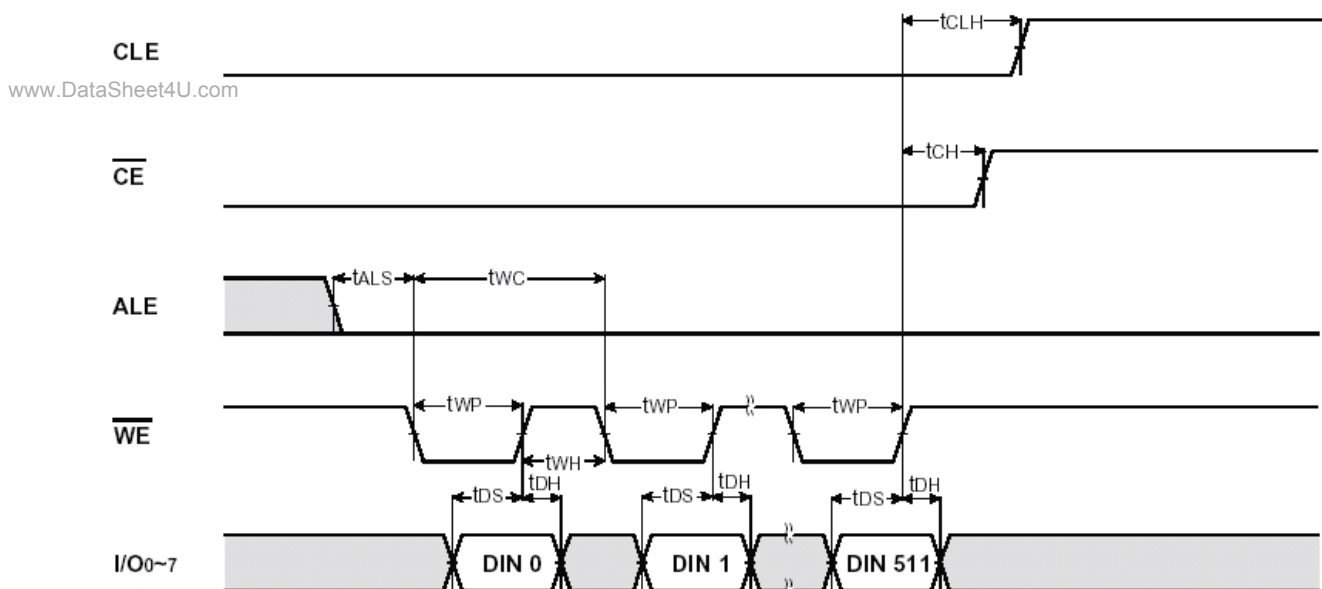
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H1.2 Address Latch Cycle



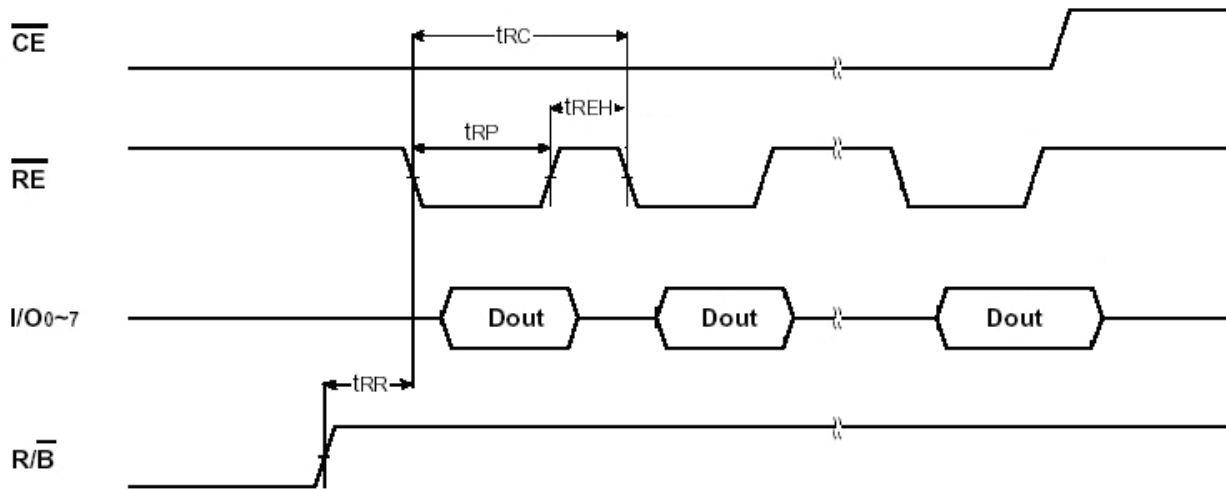
H1.3 Input Data Latch Cycle



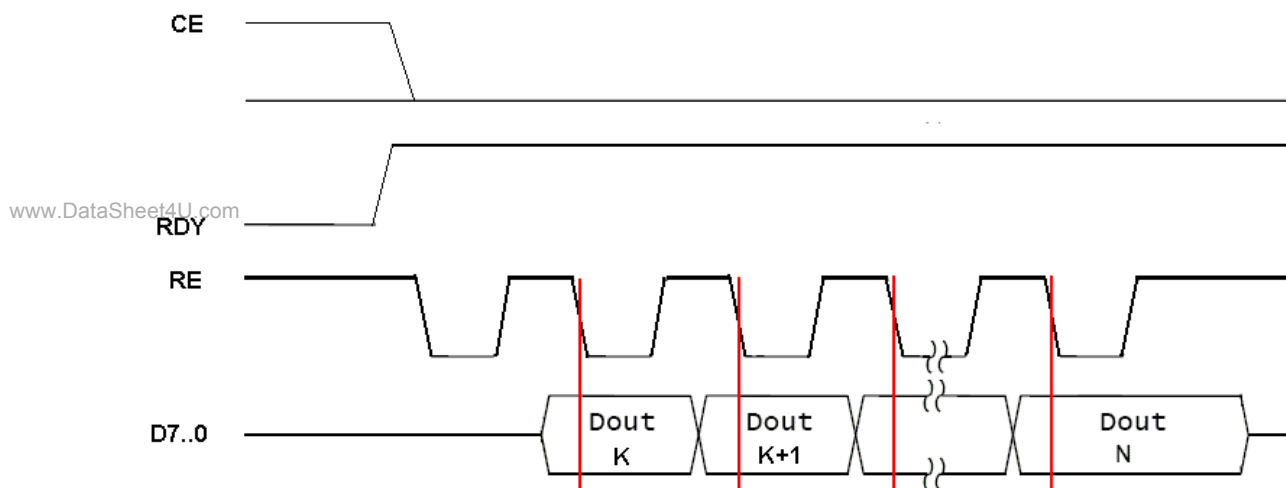
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H1.4 Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)



H1.5 EDO mode for data latch

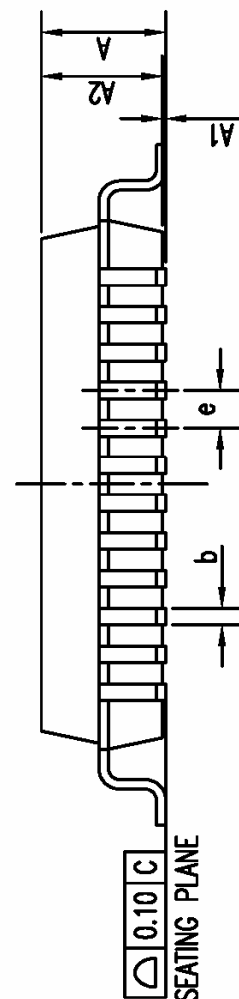
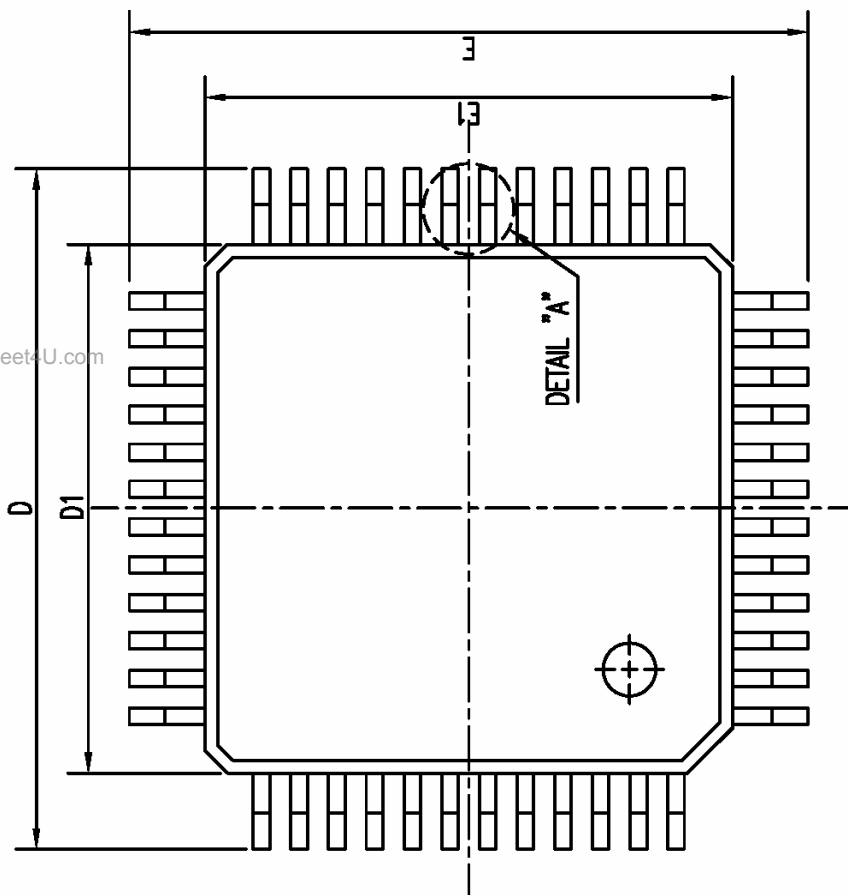
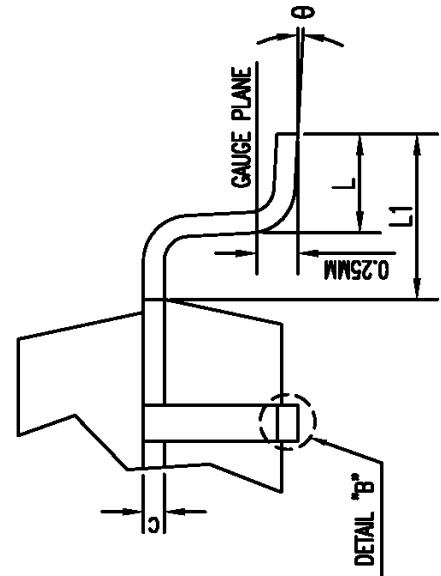


EDO mode to latch the data at the negative edge of RE.

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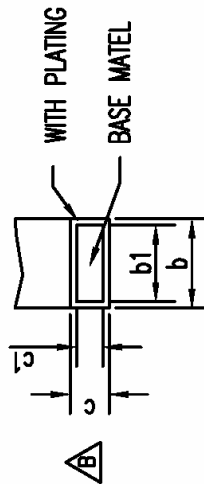
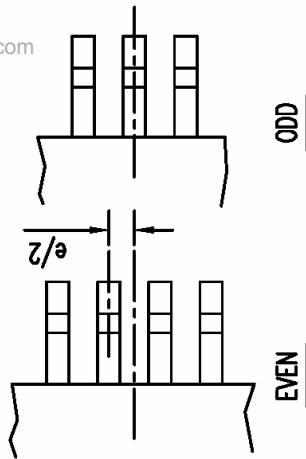
I. Package Information



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SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

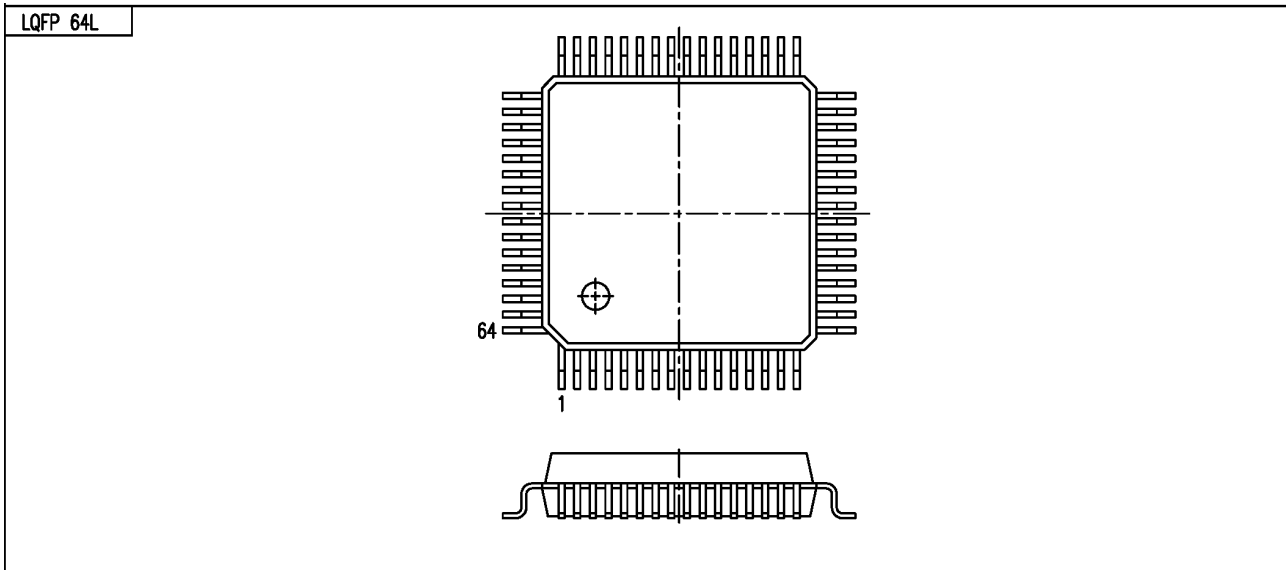


N	b (MM)			b1 (MM)			e (MM)		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.
64L	0.13	0.16	0.19	0.13	0.16	0.19	0.40 BSC.		
JEDEC									

UNLESS OTHERWISE SPECIFIED	DECIMAL X .xx ±.10 .xxx ±.05	ANGULAR ±3°	THIRD ANGLE PROJECTION :
DRAWN	Vivian Lin 2004.06.09	UNIT: mm	SCALE: 11:1
CHECKED	Vivian Lin 2004.06.09	JEDEC NO.: MS-026	TITLE: Package outline dimension drawing for LQFP 7x7x1.4mm family
APPROVED	Alex Hung	PACKAGE CODE : PAAG	
APPROVED	Alex Hung for	DWG. NO. : PD-PA01	REV.: B
		DOC. NO.: PD-PA01	REV.: B
		SHEET : 1	A3

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UNLESS OTHERWISE SPECIFIED	DECIMAL .X ± .XX ±.10 .XXX ±.05	ANGULAR ±3°	THIRD ANGLE PROJECTION : 						
DRAWN	Vivian Lin 2004.06.09	UNIT: mm	SCALE: 8:1	TITLE:					
CHECKED	Vivian Lin 2004.06.09	JEDEC NO.: MS-026		Package outline dimension drawing for LQFP 7x7x1.4mm family					
APPROVED	Alex Hung	PACKAGE CODE : PAAC							
APPROVED	Alex Hung for	DWG. NO. : PD-PA01	REV.: B	DOC. NO.: PD-PA01	REV.: B	SHEET :	2	A3	