8Ch, 24bit, 192kHz Digital Audio Processor for Full Digital Amplifier

Introduction

The PS9818 is a highly integrated system-on-chip solution for multi-channel AV systems such as 5.1 channel, 6.1 channel or 7.1 channel. The PS9818 is 8 channel and 3 additional channel PCM to PWM modulator with full 8 channel sample rate converter and pre-amplifier functions. It features 24-bit audio digital-to-digital converters and over-sampling digital filters, a sample rate converter, an audio DSP that functions as an on-chip pre-amplifier with, equalizer, volume control, bass management, and automatic gain limiting functions.

The sample rate converter is allowing for input of upto 96kHz, 8 channel and 192kHz, 2 channel. It automatically detects the sampling frequency and converts input sample rate to internal 192kHz sample rate. It makes easy for user to handle this chip.

The PS9818 accepts industry-standard audio data formats with 16- to 24-bit audio data. Sampling rates of up to 192 kHz are supported.

Application

- DVD Receiver (DVD player plus 7.1ch Receiver)
- HiFi A/V Receiver
- HDTV sets
- Settop Box
- Car A/V Systems
- DVD Add-On Cards for High-End PCs
- Digital Audio Workstations
- Other Multi-Channel Digital Audio Systems

Features

General

- 2 serial input ports for 8 Channel
- User can select the master/slave mode of input port
- Sub input port can be changed to serial output port
- Supports 16/18/20/24 bit Input
- Supports 32kHz~192kHz Input Sample Rate
- I^2C or SPI control bus
- Internal PLL (low jitter)
- 100 pin QFP Package
- 2.5V core, 3.3V I/O Power Supply
- 5V tolerant Inputs

Sample-rate-converter Section

- On chip Sample rate converter
- Supports upto 96kHz sample rate for 8 channel input
- Supports upto 192kHz sample rate for 2 channel input
- Automatic sample rate detection

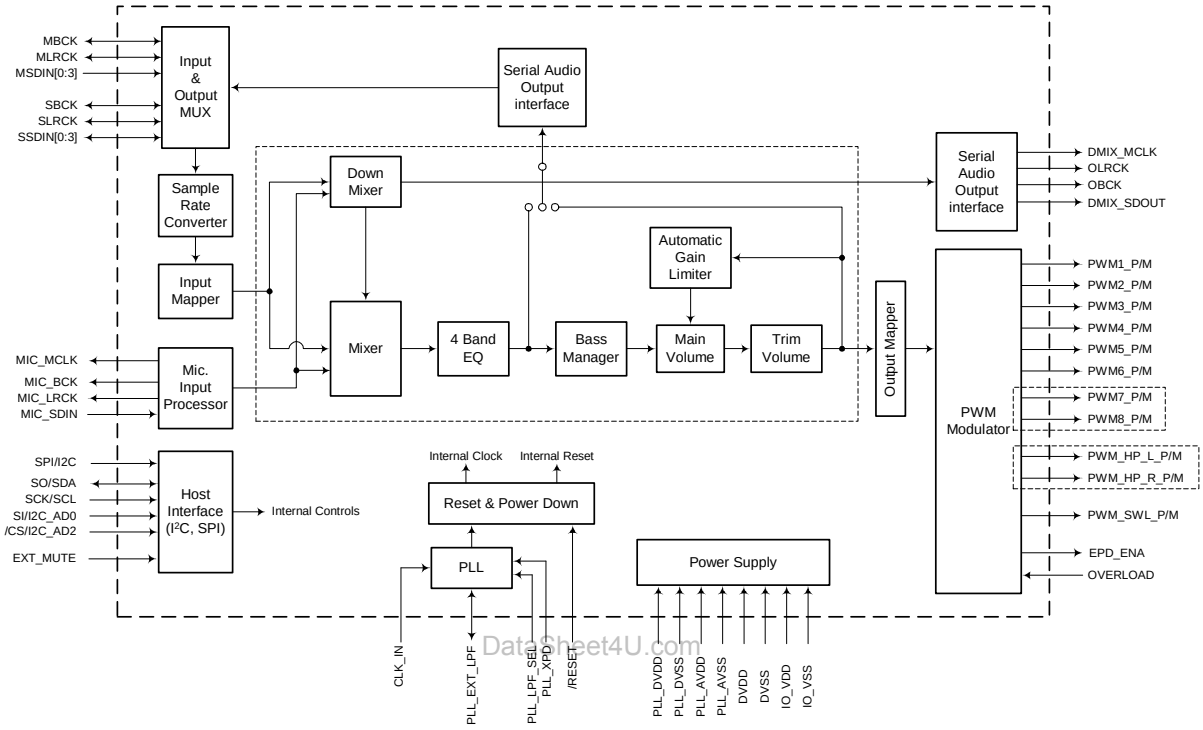
Preamplifier Section

- Input and Output mapping function
- On chip Digital De-emphasis filter
- Input mixing function
- Microphone mixing function
- Stereo Downmixing function and output
- Fully Programmable 4 band EQ per channel (1dB/step)
- Adjustable EQ processing position
- Two EQ coefficients sets
- Bass management function
- Four Bi-quad filter for subwoofer channel
- Main Volume control (+18 to -70, 0.5dB/step)
- Additional Trim control (+12 to -12, 0.5dB/step) per channel
- Soft Volume and Soft Volume Update
- Two independent Automatic Gain Limiter Group (peak detection)
- Soft Mute per channel
- DC input detect Auto-Mute (include Zero input)
- Clipping-free processing (30-bit data processing)

PCM-to-PWM modulator section

- 8 channel PWM Amplification output
- Selectable PWM line output on channel 7 and 8
- 2 channel PWM Headphone output
- 1 channel PWM Subwoofer line output
- PWM On/Off control per channel
- 102 dB Dynamic Range
- 105 dB SNR

Functional Block Diagram



Specifications

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Power Supply Voltage (IO_VDD)	- 0.5	4.0	V
Power Supply Voltage (DVDD, PLL_AVDD, PLL_DVDD)	- 0.5	3.3	V
Output Current (/Pin)	-	±30	mA
Input Voltage	V_{SS} – 0.5	5.5	V
Storage Temperature	-65	+150	°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

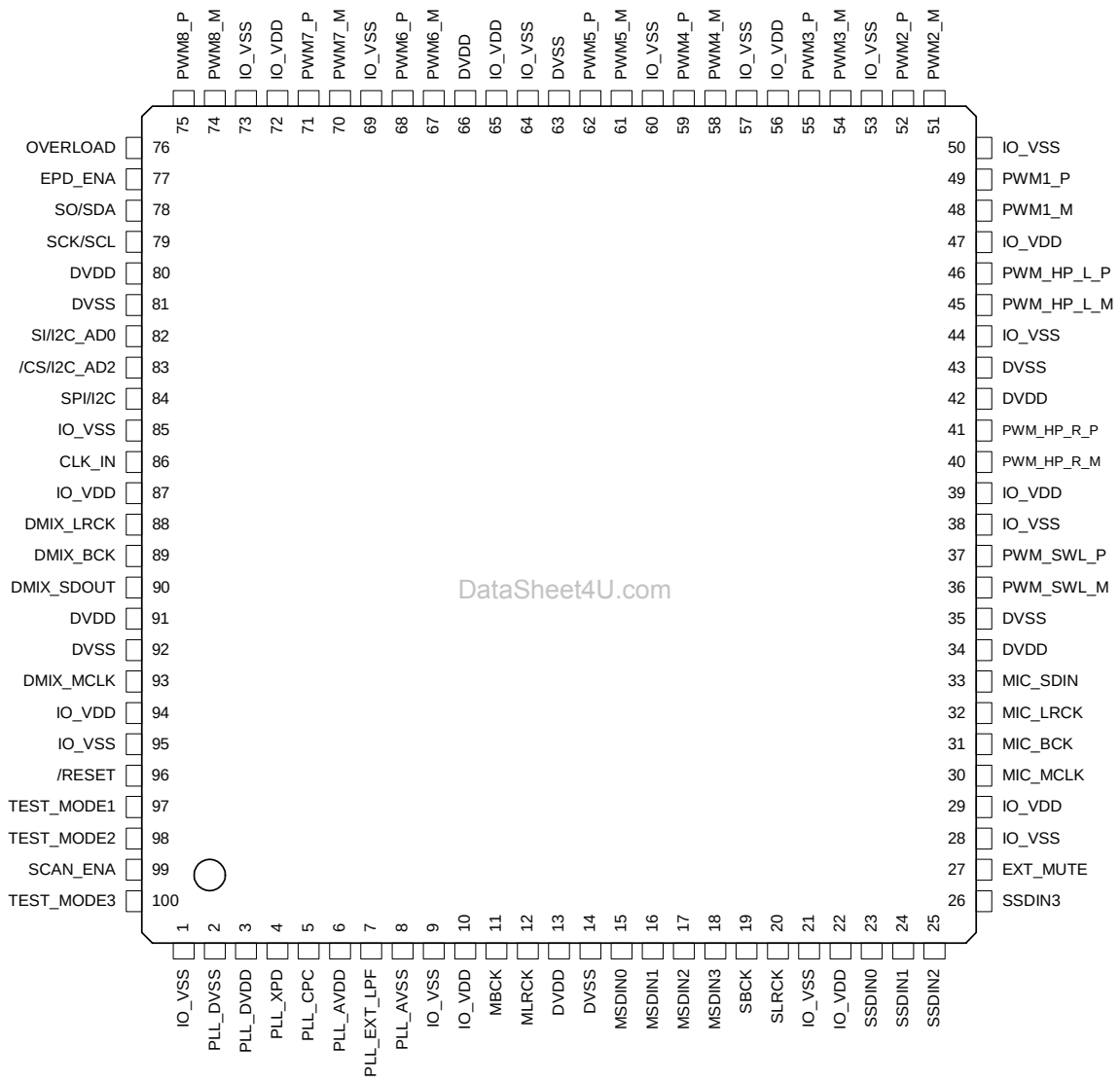
RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Power Supply Voltage (IO_VDD)	3.0	3.3	3.6	V
Supply Current (IO_VDD = 3.3V)	-	2.5	-	mA
Power Supply Voltage (DVDD)	2.25	2.5	2.75	V
Supply Current (DVDD = 2.5V)	-	210	-	mA
Power Supply Voltage (PLL_AVDD, PLL_DVDD)	2.35	2.5	2.75	V
Supply Current (PLL_AVDD, PLL_DVDD = 2.5V)	-	2.9	-	mA
Input Voltage	- 0.5	-	5.5	V
Ambient Operating Temperature	-20	-	+75	°C

ELECTRICAL CHARACTERISTICS

Parameter	Min	Typ	Max	Units
Input Leakage Current (except Pull-up, Pull-down Input)	-	-	30	µA
High-Level Input Voltage (except Schmitt Input)	2.0	-	-	V
Low-Level Input Voltage (except Schmitt Input)	-	-	0.8	V
High-Level Input Voltage (Schmitt Input)	1.39	-	2.06	V
Low-Level Input Voltage (Schmitt Input)	0.9	-	1.46	V
High-Level Output Voltage (I_O = 2mA)	V_{DD} – 0.4	-	-	V
Low-Level Output Voltage (I_O = 2mA)	-	-	0.4	V
Pull-up Resistance	20	50	100	kΩ
Pull-down Resistance	20	50	100	kΩ
Input Capacitance (f = 1MHz, V_{DD} = 0V)	-	-	10	pF
Output Capacitance (f = 1MHz, V_{DD} = 0V)	-	-	10	pF

Pin Assignment



PS9818 (100pin Plastic QFP, Top View)

Pin Descriptions

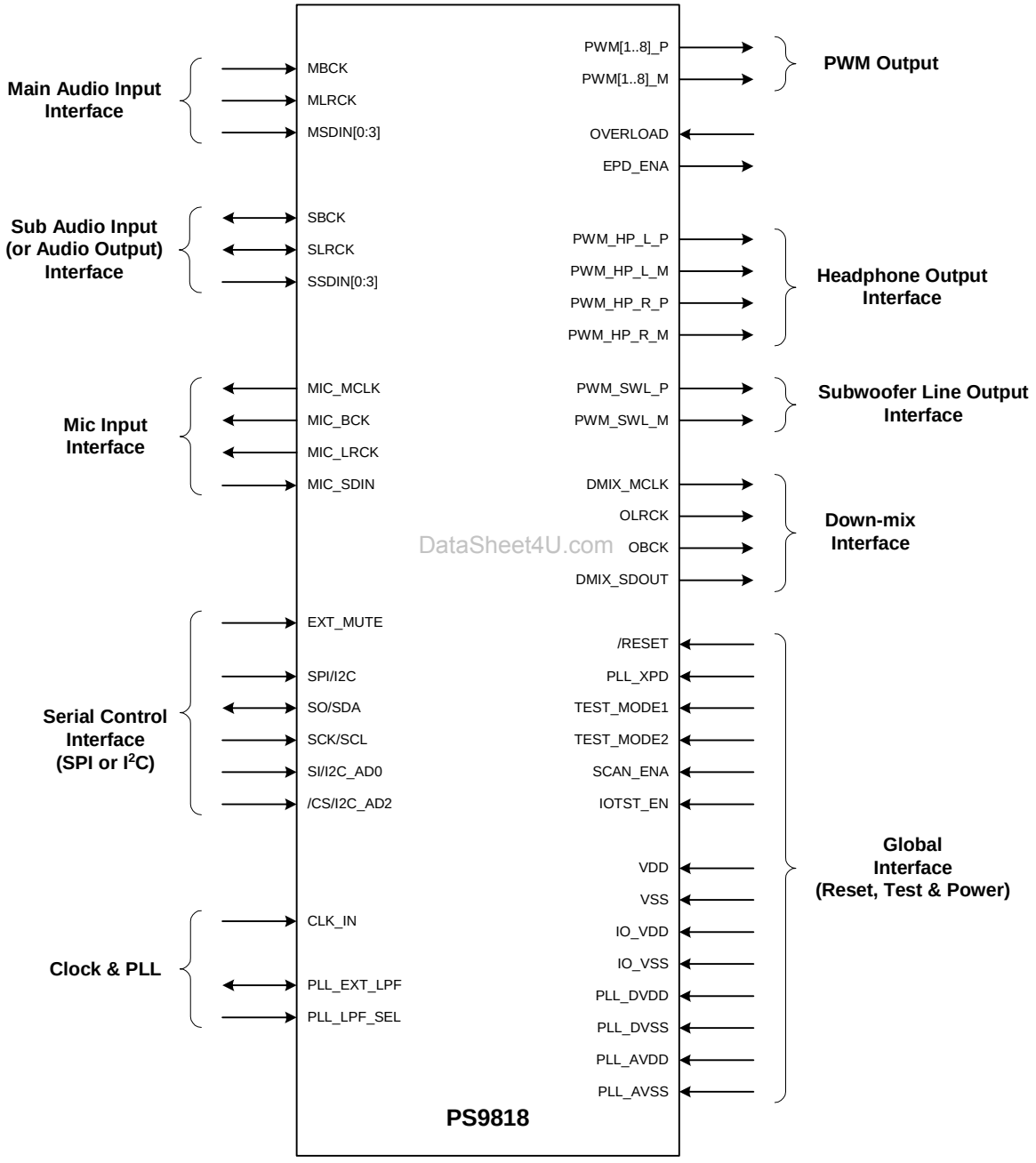
Name	Pin NO.	Type	Description
Power and Ground			
PLL_AVDD	6	Analog Power	PLL analog power supply. 2.5V supply voltage.
PLL_AVSS	8	Analog Ground	PLL analog ground.
PLL_DVDD	3	PLL Power	PLL peripheral digital power supply. 2.5V supply voltage.
PLL_DVSS	2	PLL Ground	PLL digital ground.
DVDD	13, 34, 42, 66, 80, 91	Power	2.5V Digital power supply. Core power supply.
DVSS	14, 35, 43, 63, 81, 92	Ground	Core digital ground.
IO_VDD	10, 22, 29, 39, 47, 56, 65, 72, 87, 94	Power	3.3V Digital power supply. I/O power supply.
IO_VSS	1, 9, 21, 28, 38, 44, 50, 53, 57, 60, 64, 69, 73, 85, 95	Ground	I/O digital ground.
System Services			
/RESET	96	I	H/W reset signal. Active Low Schmitt-Trigger input. The Schmitt-Trigger input allows a slowly rising input to reset the chip reliably. The RESET signal must be asserted 'Low' during power up. De-assert 'High' for normal operation.
CLK_IN	86	I	External clock input. 12.288MHz is recommended. When the PLL_BYPASS is "LOW", the external clock input from CLK_IN is used as PLL reference clock source. The external oscillator generates 12.288MHz clock and the internal PLL generates 196.608MHz (12.288MHz x 16) system clock.
PLL_XPD	4	I	Internal PLL Power Down. Active Low. Don't pull down "PLL_XPD" pin when PWM output is activated. *Internal pull-up resistor.*
PLL_CPC	5	I	Internal PLL Charge Pump Current Selection input. 'LOW' for 50uA, 'HIGH" for 100uA. *Internal pull-down resistor.*
PLL_EXT_LPF	7	Analog	External PLL low pass filter pin.
PCM Audio Input/Output Interface			
MBCK	11	I/O	PCM bit clock input/output of main 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.
MLRCK	12	I/O	PCM Word clock (left-right clock) input/output of main 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.
MSDIN[3:0]	18, 17, 16, 15	I	PCM serial data input of main 8-channel audio. Schmitt-Trigger input.
SBCK	19	I/O	PCM bit clock input/output of 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.

Name	Pin NO.	Type	Description
SLRCK	20	I/O	PCM Word clock (left-right clock) input/output of sub 8-channel audio. User can select the master/slave mode of this signal. Schmitt-Trigger input.
SSDIN[3:0]	26, 25, 24, 23	I/O	PCM serial data input of sub-channel audio. User can set this sub-channel data input pins to PCM serial data output pins. See the *Control Register Description* part.
MIC_MCLK	30	O	Main clock for external microphone input A/DC. Clock frequency can be selected between 6.144MHz, 12.288MHz, 24.576MHz.
MIC_BCK	31	O	PCM bit clock output of external microphone. Bit clock frequency is 3.072MHz (48kHz x 64, fixed)
MIC_LRCK	32	O	PCM Word clock (left-right clock) output of external microphone. Word clock rate is 48kHz (fixed).
MIC_SDIN	33	I	PCM serial data input of external microphone. Schmitt-Trigger input.
DMIX_MCLK	93	O	Main clock for external downmix line output D/AC.
DMIX_BCK	89	O	PCM bit clock output of downmix signal. Bit clock frequency is 6.144MHz (96kHz x 64, fixed)
DMIX_LRCK	88	O	PCM Word clock (left-right clock) output of downmix signal. Word clock rate is 96kHz (fixed).
DMIX_SDOUT	90	O	PCM serial data output of downmix signal. Schmitt-Trigger input.
PWM Audio Output			
PWM1_P	49	O	Positive PWM output of channel 1.
PWM1_M	48	O	Negative PWM output of channel 1.
PWM2_P	52	O	Positive PWM output of channel 2.
PWM2_M	51	O	Negative PWM output of channel 2.
PWM3_P	55	O	Positive PWM output of channel 3.
PWM3_M	54	O	Negative PWM output of channel 3.
PWM4_P	59	O	Positive PWM output of channel 4.
PWM4_M	58	O	Negative PWM output of channel 4.
PWM5_P	62	O	Positive PWM output of channel 5.
PWM5_M	61	O	Negative PWM output of channel 5.
PWM6_P	68	O	Positive PWM output of channel 6.
PWM6_M	67	O	Negative PWM output of channel 6.
PWM7_P	71	O	Positive PWM output of channel 7.
PWM7_M	70	O	Negative PWM output of channel 7.
PWM8_P	75	O	Positive PWM output of channel 8.
PWM8_M	74	O	Negative PWM output of channel 8.
PWM_HP_L_P	46	O	Positive PWM output of headphone left channel.
PWM_HP_L_M	45	O	Negative PWM output of headphone left channel.
PWM_HP_R_P	41	O	Positive PWM output of headphone right channel.
PWM_HP_R_M	40	O	Negative PWM output of headphone right channel.
PWM_SWL_P	37	O	Positive PWM output of subwoofer line output.
PWM_SWL_M	36	O	Negative PWM output of subwoofer line output.

Name	Pin NO.	Type	Description
System Control Interface			
SPI/I2C	84	I	Host interface mode (SPI or I2C) selector. Assert 'HIGH' for SPI mode. De-assert 'LOW' for I2C mode. *Internal pull-down resistor.*
SO/SDA	78	I/O	SO for SPI mode or SDA for I2C mode.
SCK/SCL	79	I	SCK for SPI mode or SCL for I2C mode. Schmitt-Trigger input.
SI/I2C_AD0	82	I	SI for SPI mode or Slave Address 0 for I2C mode. Schmitt-Trigger input. *Internal pull-down resistor.*
/CS/I2C_AD2	83	I	Chip selector (CS) for SPI mode or Slave Address 2 for I2C mode. Schmitt-Trigger input. *Internal pull-down resistor.*
Special Control Interface			
EXT_MUTE	27	I	External mute control input. Active High. Assert 'HIGH' to mute audio output. *Internal pull-down resistor.*
OVERLOAD	76	I	Power stage overload indication input. Polarity is programmable. Schmitt-Trigger input. When OVERLOAD is asserted, all PWM audio outputs go to "LOW". That shutdown process is programmable. *Internal pull-down resistor.*
EPD_ENA	77	O	External amplifier power device enable output. Active High.
Test Mode			
TEST_MODE1	97	I	Test mode selection pin 1. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
TEST_MODE2	98	I	Test mode selection pin 2. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
SCAN_ENA	99	I	Scan enable. Active High. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*
TEST_MODE3	100	I	Test mode selection pin 3. In normal operation, it should be "LOW" or not connected. *Internal pull-down resistor.*

※ All inputs and bi-directional inputs are 5 Volt tolerant. The corresponding pins can be connected to the buses that can swing between 0V and 5V. The output-only pins are not 5V tolerant and the buses they are connected to can swing only between 0V and 3.3V.

Signal Interface Diagram



Signal Descriptions

1. Clock and Reset

The PS9818 uses 196.608MHz (48KHz x 4096) system clock internally. The PS9818 uses external 12.288MHz clock source and has x16 PLL (Phase Locked Loop) for internal system clock generation. Main processing clock of the PS9818 is 98.304MHz that is PLL output divided by 2.

2. PCM Audio Input Signals

PS9818 uses serial interface for PCM audio data input using ***BCK***, ***LRCK***, and ***DIN*** pins. It has two input ports for eight channel audio data (main and sub). But the sub-input ports can be used as one eight-channel audio output port.

3. PWM Audio Output Signals

The PS9818 converts PCM audio data to PWM audio signal. It outputs one eight-channel PWM signal for main audio, one two-channel PWM signal for headphone and one additional one-channel PWM signal for subwoofer line output. All PWM signal consist of the both positive and negative PWM signals.

4. Control Interface Signals

The PS9818 supports internal control register I/O using both SPI and I^2C. The pin ***SPI/I2C*** selects the control interface method. The control registers has 8-bit address space and 16-bit or 24-bit data length. All internal control registers are both readable and writable.

5. Special Control Signals

The PS9818 can generate only AD mode PWM signal. For more information about the Power stage driving method and AD/BD mode of PWM amplifier, refer the “PULSUS PWM Amplification application notes”.

The PS9818 has Overload protection logic. When the pin ***OVERLOAD*** is “HIGH” (default setting, the polarity is programmable), the PS9818 goes to protection mode and all PWM outputs go to “LOW”.

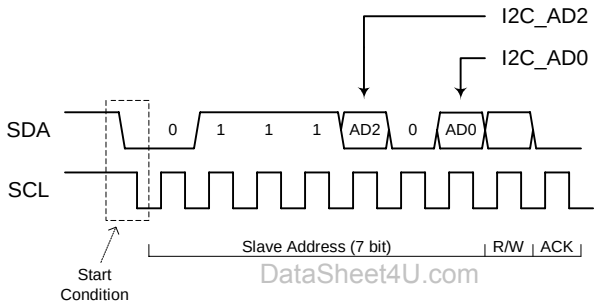
Also, the PS9818 has external power device control logic. Pin ***EPD_ENA*** (External Power Device Enable) output timing is programmable by control register. The PS9818 can handle various power devices with this ***EPD_ENA*** pin configuration function and miscellaneous PWM configuration functions.

Control Interface Protocol

1. I²C Control Interface

The pin ***SPI/I2C*** selects the control interface method. When the pin ***SPI/I2C*** is grounded, the control interface method is I²C interface.

The I²C slave address can be varied using two I²C slave address setting pin, ***I2C_AD0*** and ***I2C_AD2***. The base slave address is 0x38 with ***I2C_AD0*** and ***I2C_AD2*** pin grounded. Figure below shows you the configuration of slave address.

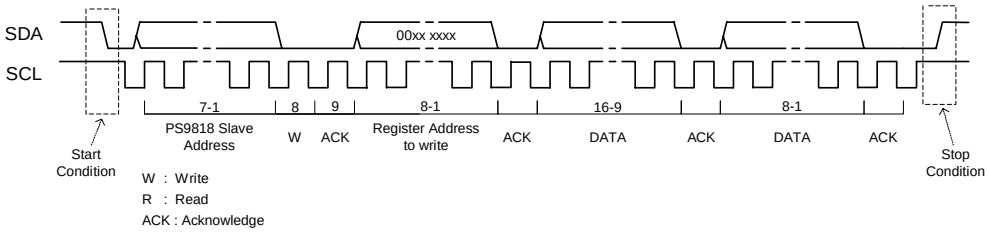


I2C_AD2	I2C_AD0	PS9818 Slave Address
0	0	0x38 (0b0111000)
0	1	0x39 (0b0111001)
1	0	0x3C (0b0111100)
1	1	0x3D (0b0111101)

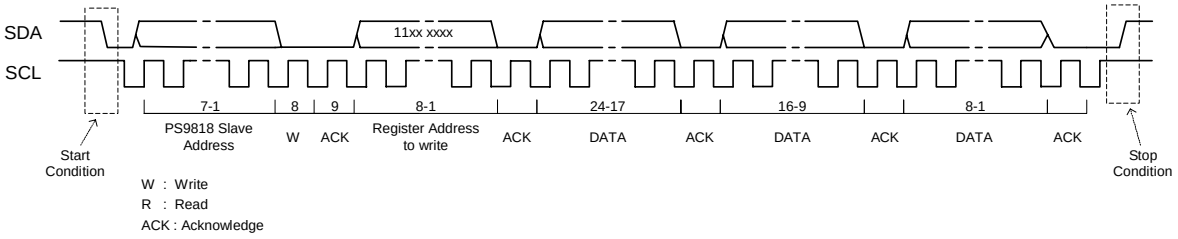
The control registers has 8-bit address space and 16-bit or 24-bit data length. If the upper two bits of register address are all HIGH, 11xx xxxx, then the data length will be three bytes (24 bits). The other case, the data length will be two bytes (16 bits).

The I²C control protocol diagram is in the next page.

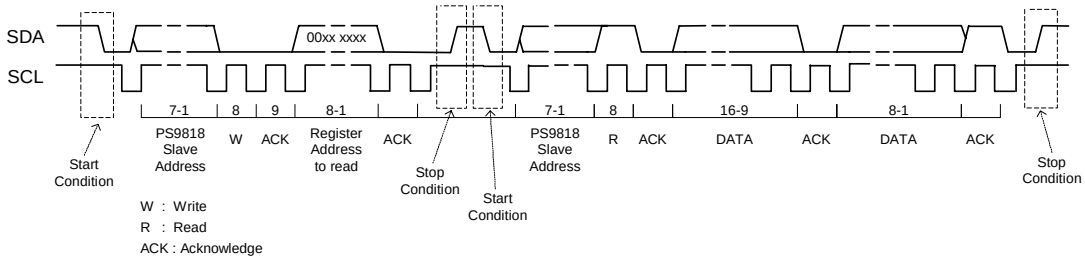
2Bytes Write Operation (I^2C interface)



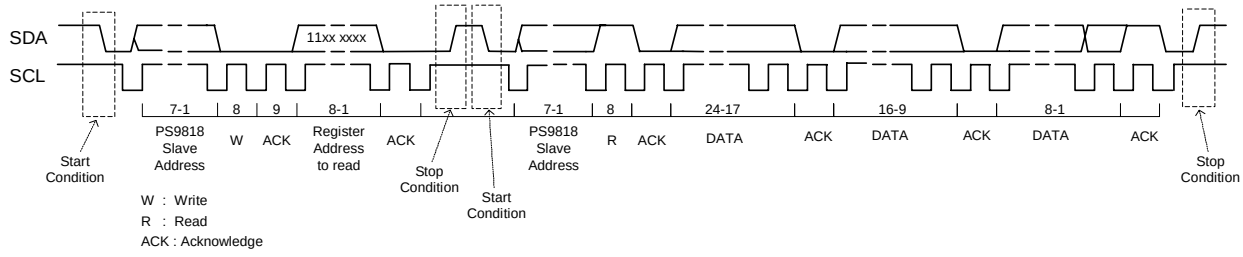
3Bytes Write Operation (I^2C interface)



2Bytes Read Operation (I^2C interface)



3Bytes Read Operation (I^2C interface)

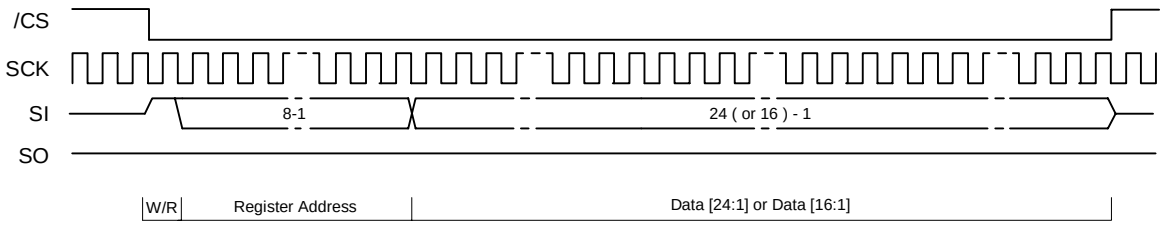


2. SPI Control Interface

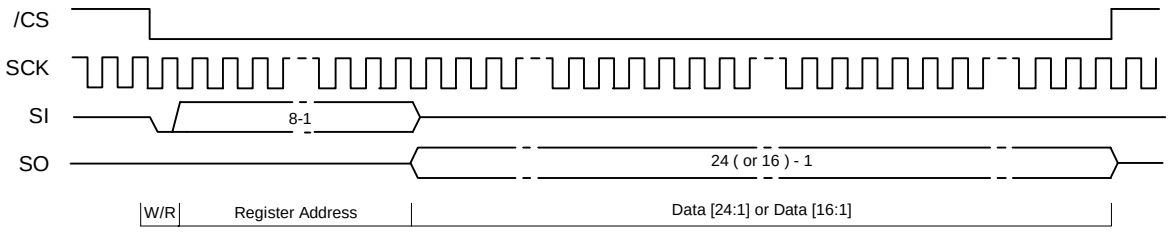
The pin ***SPI/I2C*** selects the control interface method. When the pin ***SPI/I2C*** is connected to VCC, the control interface method is SPI interface.

SPI control protocol diagram is below.

Write Operation (SPI interface)



Read Operation (SPI interface)



Control Register Descriptions

Register Name	Address	Word Length	Description
PWM output On/Off Control Register			
PWM_ON_OFF	0x00	2 Bytes	PWM output activation control register. [0]: Global Off/On control of PWM output. *Default = "1". (Off)* [4:1]: *Reserved.* [5]: Off/On control of Subwoofer Lineout PWM output. *Default = "0". (On)* [6]: Off/On control of Headphone Left PWM output. *Default = "0". (On)* [7]: Off/On control of Headphone Right PWM output. *Default = "0". (On)* [8]: Off/On control of PWM1 output. *Default = "0". (On)* [9]: Off/On control of PWM2 output. *Default = "0". (On)* [10]: Off/On control of PWM3 output. *Default = "0". (On)* [11]: Off/On control of PWM4 output. *Default = "0". (On)* [12]: Off/On control of PWM5 output. *Default = "0". (On)* [13]: Off/On control of PWM6 output. *Default = "0". (On)* [14]: Off/On control of PWM7 output. *Default = "0". (On)* [15]: Off/On control of PWM8 output. *Default = "0". (On)* "0" = PWM On "1" = PWM Off *Default = 0x0001 (Global PWM Off)*

Register Name	Address	Word Length	Description
Input Interface Unit Configuration Registers			
SRC_STATUS	0x01	2 Bytes	SRC (Sample Rate Converter) Status Indication register. Read only register. [0]: SRC (Sample Rate Converter) Lock indication. Active High. Read only. "0" = Unlock (or No signal) "1" = Lock [4:1]: Input sample rate indication. Read only. "0001" = 32KHz "0010" = 44.1KHz "0011" = 48KHz "0110" = 88.2KHz "0111" = 96KHz "1010" = 176.4KHz "1011" = 192KHz [5]: Out of Locking Range indication. Read only. '0' = in locking range '1' = out of locking range [15:6]: *Not Used*.
IN_CONTROL	0x02	2 Bytes	Serial audio data input interface control register. [1:0]: BCK count. *Default = "10".* "00" = 16bit, "01" = 24bit, "10" = 32bit. [2]: BCK polarity. *Default = "1".* "0" = Valid data at Negative edge "1" = Valid data at Positive edge [3]: Data align. "0" = Right aligned, "1" = Left aligned. *Default = "1".* [4]: First channel data along LRCK polarity. *Default = "0".* "0" = First channel data when LRCK is low. "1" = First channel data when LRCK is high. [5]: Data MSB first. "0" = LSB first, "1" = MSB first. *Default = "1".* [7:6]: Data word length. *Default = "11".* "00" = 16bit, "01" = 18bit, "10" = 20bit, "11" = 24bit. [8]: I2S compatible. "1" = Compatible. *Default = "1".* [15:9]: *Not Used*. *Default = 0x01EE*
IN_CONFIGURE	0x03	2 Bytes	Input port configuration register. [0]: Input port selector. *Default = "1".* "0" = SUB 8 channel input port (SSDIN[3:0]) "1" = MAIN 8 channel input port (MSDIN[3:0]) [1]: Master/slave mode selector for MBCK and MLRCK. *Default = "0".* "0" = Slave mode, "1" = Master mode. [2]: Master/slave mode selector for SBCK and SLRCK. *Default = "0".* "0" = Slave mode, "1" = Master mode. [3]: Input/output selector for SUB serial audio interface port. *Default = "0".* "0" = Serial audio data input, "1" = Serial audio data output. [15:4]: *Not Used*. *Default = 0x0001*

Register Name	Address	Word Length	Description
MIC_CONTROL	0x04	2 Bytes	MIC data input interface control register. [0]: BCK polarity. *Default = "1".* "0" = Valid data at Negative edge. "1" = Valid data at Positive edge. [1]: Data align. "0" = Right aligned. "1" = Left aligned. *Default = "1".* [2]: First channel data along LRCK polarity. *Default = "0".* "0" = First channel data when LRCK is low. "1" = First channel data when LRCK is high. [3]: Data MSB first. "0" = LSB first, "1" = MSB first. *Default = "1".* [5:4]: Data word length. *Default = "11".* "00" = 16bit, "01" = 18bit, "10" = 20bit, "11" = 24bit. [6]: I2S compatible. "1" = Compatible. *Default = "1".* [8:7]: MIC_MCLK frequency selection. *Default = "01".* "00" = 6.144MHz, "01" = 12.288MHz, "10" = 24.576MHz. [15:9]: *Not Used*. *Default = 0x00FB*
SERIAL_OUT_CONTROL	0x05	2 Bytes	Serial audio data output interface control register. [0]: BCK polarity. *Default = "1".* "0" = Valid data at Negative edge, "1" = Valid data at Positive edge. [1]: Data align. "0" = Right aligned. "1" = Left aligned. *Default = "1".* [2]: First channel data along LRCK polarity. *Default = "0".* "0" = First channel data when LRCK is low. "1" = First channel data when LRCK is high. [3]: Data MSB first. "0" = LSB first, "1" = MSB first. *Default = "1".* [5:4]: Data word length. *Default = "11".* "00" = 16bit, "01" = 18bit, "10" = 20bit, "11" = 24bit. [6]: I2S compatible. "1" = Compatible. *Default = "1".* [8:7]: DMIX_MCLK frequency selection. *Default = "01".* "00" = 6.144MHz, "01" = 12.288MHz, "10" = 24.576MHz. [9]: Data rate selection. *Default = "1".* "0" = 192kHz, "1" = 96kHz. [15:10]: *Not Used*. *Default = 0x02FB*

Register Name	Address	Word Length	Description
Volume Configuration Registers			
MASTER_VOL_CONTROL	0x10	2 Bytes	Master Volume Control register. The PS9818 have one master volume and individual trim volume per each channel. The master volume is adjustable in the resolution of 0.5dB/step. The maximum volume gain is +18dB and the minimum volume gain is -70dB. The volume control register has 8-bit resolution. The register value 0x0C (or less) means +18dB, and the value 0xBC means -70dB. And the register value larger than 0xBC means same attenuation level -70dB. Table A-1 shows the relations between the register value and volume gain. [7:0]: Master volume. [15:8]: *Not Used*. *Default = 0x00BC (-70dB)*
TRIM_FL_FR	0x11	2 Bytes	Trim control register of Front Left and Front Right channel. The PS9818 has individual trim volume per each channel. The individual trim volume is adjustable in the resolution of 0.5dB/step from -12dB to +12dB. Table A-2 shows the relations between the register value and trim gain. [5:0]: Front Left channel Trim volume. [7:6]: *Reserved.* [13:8]: Front Right channel Trim volume. [15:14]: *Reserved.* *Default = 0x0000 (0dB, 0dB)*
TRIM_SL_SR	0x12	2 Bytes	Trim control register of Surround Left and Surround Right channel. Table A-2 shows the relations between the register value and trim gain. [5:0]: Surround Left channel Trim volume. [7:6]: *Reserved.* [13:8]: Surround Right channel Trim volume. [15:14]: *Reserved.* *Default = 0x0000 (0dB, 0dB)*
TRIM_C_SW	0x013	2 Bytes	Trim control register of Center and Subwoofer channel. Table A-2 shows the relations between the register value and trim gain. [5:0]: Center channel Trim volume. [7:6]: *Reserved.* [13:8]: Subwoofer channel Trim volume. [15:14]: *Reserved.* *Default = 0x0000 (0dB, 0dB)*
TRIM_SBL_SBR	0x014	2 Bytes	Trim control register of Surround Back Left and Surround Back Right channel. Table A-2 shows the relations between the register value and trim gain. [5:0]: Surround Back Left channel Trim volume. [7:6]: *Reserved.* [13:8]: Surround Back Right channel Trim volume. [15:14]: *Reserved.* *Default = 0x0000 (0dB, 0dB)*

Register Name	Address	Word Length	Description
Automatic Gain Limiter Threshold Registers			
AGL_THR_FL_FR	0x15	2 Bytes	Automatic gain limiter (AGL) threshold levels of Front Left and Front Right channel. The AGL threshold level is controlled in dB magnitude and it is adjustable in the resolution of 0.5dB/step. This register has 8-bit resolution. The maximum threshold level is +18dB and the minimum threshold level is limited to -20dB. Table A-1 shows the relations between the register value and threshold level. [7:0]: AGL threshold of Front Left channel. [15:8]: AGL threshold of Front Right channel. *Default = 0x2C2C (+2dB, +2dB)*
AGL_THR_SL_SR	0x16	2 Bytes	AGL threshold levels of Surround Left and Surround Right channel. Table A-1 shows the relations between the register value and threshold level. But the minimum threshold level is limited to -20dB. [7:0]: AGL threshold of Surround Left channel. [15:8]: AGL threshold of Surround Right channel. *Default = 0x2C2C (+2dB, +2dB)*
AGL_THR_C_SW	0x017	2 Bytes	AGL threshold levels of Center and Subwoofer channel. Table A-1 shows the relations between the register value and threshold level. But the minimum threshold level is limited to -20dB. [7:0]: AGL threshold of Center channel. [15:8]: AGL threshold of Subwoofer channel. *Default = 0x2C2C (+2dB, +2dB)*
AGL_THR_SBL_SBR	0x018	2 Bytes	AGL threshold levels of Surround Back Left and Surround Back Right channel. Table A-1 shows the relations between the register value and threshold level. But the minimum threshold level is limited to -20dB. [7:0]: AGL threshold of Surround Back Left channel. [15:8]: AGL threshold of Surround Back Right channel. *Default = 0x2C2C (+2dB, +2dB)*

Register Name	Address	Word Length	Description
Mute Control Registers			
GLOBAL_MUTE	0x019	2 Bytes	Global Mute control register. The PS9818 have global mute control to affect all the channels and individual mute control per each channel. All the mute functions are soft mute. There are two methods to make the PS9818 go to the global mute status. When the external mute pin "EXT_MUTE" is asserted high, the PS9818 goes to the global mute status. And alternative way is setting this global mute control register bit. "0" = Mute Off "1" = Mute On [0]: Global Mute. Active High. [15:1]: *Not Used*. *Default = 0x0001 (Mute)*
CH_MUTE_CONTROL	0x01A	2 Bytes	Channel Mute control register. "0" = Mute Off "1" = Mute On [0]: Front Left channel Mute control. [1]: Front Right channel Mute control. [2]: Surround Left channel Mute control. [3]: Surround Right channel Mute control. [4]: Center channel Mute control. [5]: Subwoofer channel Mute control. [6]: Surround Back Left channel Mute control. [7]: Surround Back Right channel Mute control. [8]: Headphone Left channel Mute control. [9]: Headphone Right channel Mute control. [10]: Lineout Subwoofer channel Mute control. [15:11]: *Not Used*. *Default = 0x0000 (Mute Off)*
CH_MUTE_STATUS	0x01B	2 Bytes	Channel Mute status monitoring register. Read Only register. "0" = Mute Off "1" = Mute On [0]: Front Left channel Mute status. Read Only. [1]: Front Right channel Mute status. Read Only. [2]: Surround Left channel Mute status. Read Only. [3]: Surround Right channel Mute status. Read Only. [4]: Center channel Mute status. Read Only. [5]: Subwoofer channel Mute status. Read Only. [6]: Surround Back Left channel Mute status. Read Only. [7]: Surround Back Right channel Mute status. Read Only. [8]: Headphone Left channel Mute status. Read Only. [9]: Headphone Right channel Mute status. Read Only. [10]: Lineout Subwoofer channel Mute status. Read Only. [15:11]: *Not Used*.

Register Name	Address	Word Length	Description
Automatic Gain Limiter Configuration Registers			
AGL_GROUP_SEL	0x1C	2 Bytes	AGL Group selection register. The PS9818 has two Automatic Gain Limiter (AGL) Group. Each group operates independently. Each channel can be mapped to either group or not mapped. Gain of the non-mapped channel is not limited by any AGL group. "00" = no group (AGL Off) "01" = Group A "10" = Group B [1:0]: Front Left channel AGL Group selection. *Default = "01" (Group A).* [3:2]: Front Right channel AGL Group selection. *Default = "01" (Group A).* [5:4]: Surround Left channel AGL Group selection. *Default = "01" (Group A).* [7:6]: Surround Right channel AGL Group selection. *Default = "01" (Group A).* [9:8]: Center channel AGL Group selection. *Default = "01" (Group A).* [11:10]: Subwoofer channel AGL Group selection. *Default = "10" (Group B).* [13:12]: Surround Back Left channel AGL Group selection. *Default = "01" (Group A).* [15:14]: Surround Back Right channel AGL Group selection. *Default = "01" (Group A).* *Default = 0x5955 (Subwoofer: Group B, others: Group A)*
AGL_A_ATTACK	0x1D	2 Bytes	AGL Group A attack rate. - resolution : 20.83us / 0.25dB. - range : 20.83us ~ 1.33ms / 0.25dB. - attack rate : 20.83us * (user setting value + 1) / 0.25dB. [5:0]: AGL Group A attack rate. [15:6]: *Not Used*. *Default = 0x0004 (104.15us / 0.25dB)*
AGL_A_RELEASE	0x1E	2 Bytes	AGL Group A release rate. - resolution : 83.33us / 0.25dB. - range : 83.33us ~ 85.33ms / 0.25dB. - release rate : 83.33us * (user setting value + 1) / 0.25dB. [9:0]: AGL Group A release rate. [15:10]: *Not Used*. *Default = 0x00CC (17.08ms / 0.25dB)*
AGL_B_ATTACK	0x1F	2 Bytes	AGL Group B attack rate. [5:0]: AGL Group B attack rate. [15:6]: *Not Used*. *Default = 0x0004 (104.15us / 0.25dB)*
AGL_B_RELEASE	0x20	2 Bytes	AGL Group B release rate. [9:0]: AGL Group B release rate. [15:10]: *Not Used*. *Default = 0x00CC (17.08ms / 0.25dB)*

Register Name	Address	Word Length	Description
Soft Volume Configuration Register			
SOFT_VOL_SLOPE	0x21	2 Bytes	Soft volume increase/decrease rate. - resolution : 5.2083us / 0.25dB. - range : 5.21us ~ 5.33ms / 0.25dB - soft volume increase/decrease rate : 5.21us * (user setting value + 1). [9:0]: Soft volume increase/decrease rate. [15:10]: *Not Used*. *Default = 0x0020 (171.93us / 0.25dB)*
Auxiliary channel Configuration Registers			
PRESCALE_HP_LR	0x22	2 Bytes	Headphone output pre-scaling level. The each pre-scaling level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity ("0" : +, "1" : -) and LS 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and pre-scaling level. [7:0]: Headphone Left channel pre-scaling level. [15:8]: Headphone Right channel pre-scaling level. *Default = 0x2424 ((+) 0dB, (+) 0dB)*
PRESCALE_SWL	0x23	2 Bytes	Subwoofer lineout pre-scaling level. Table A-3 shows the relations between the register value and pre-scaling level. [7:0]: LFE-bypass pre-scaling level for sub-woofer lineout. [15:8]: Bass Sum pre-scaling level for sub-woofer lineout. *Default = 0x2424 ((+) 0dB, (+) 0dB)*
MASTER_SEL	0x24	2 Bytes	Master volume Off/On control "0" = Master volume On. "1" = Master volume Off. [0]: Master Volume Off control for Surround Back Left channel. [1]: Master Volume Off control for Surround Back Right channel. [2]: Master Volume Off control for Headphone Left channel. [3]: Master Volume Off control for Headphone Right channel. [4]: Master Volume Off control for Subwoofer lineout. [15:5]: *Not Used*. *Default = 0x0000 (Master volume On for SBL, SBR, HPL, HPR, SWL channel)*

Register Name	Address	Word Length	Description
MIC Mixer Configuration Register			
MIC_MIX_LEVEL	0x30	2 Bytes	Mixing level of two microphone input. The each mixing level value consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity ("0" : +, "1" : -) and LS 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: MIC0 input into Mic mixer output mixing level. [15..8]: MIC1 input into Mic mixer output mixing level. *Default = 0x3030. (-6dB, -6dB)*
De-Emphasis Control Register			
DE_EMPHASIS	0x31	2 Bytes	De-Emphasis control Register. [0]: De-Emphasis control of Front two channel. Active high. [15:1]: *Not Used.* *Default = 0x0000 (Off)*
Input Channel Mapping Configuration Registers			
INPUT_CH_MAPPING1	0x32	2 Bytes	Input channel Mapping Register1. "000" = Input Channel 0 (left channel data from SDIN0) "001" = Input Channel 1 (right channel data from SDIN0) "010" = Input Channel 2 (left channel data from SDIN1) "011" = Input Channel 3 (right channel data from SDIN1) "100" = Input Channel 4 (left channel data from SDIN2) "101" = Input Channel 5 (right channel data from SDIN2) "110" = Input Channel 6 (left channel data from SDIN3) "111" = Input Channel 7 (right channel data from SDIN3) [2:0]: Input Channel number that is linked to Front Left Channel. [3]: *Not Used.* [6:4]: Input Channel number that is linked to Front Right Channel. [7]: *Not Used.* [10:8]: Input Channel number that is linked to Surround Left Channel. [11]: *Not Used.* [14:12]: Input Channel number that is linked to Surround Right Channel. [15]: *Not Used.* *Default = 0x3210*
INPUT_CH_MAPPING2	0x33	2 Bytes	Input channel Mapping Register2. [2:0]: Input Channel number that is linked to Center Channel. [3]: *Not Used.* [6:4]: Input Channel number that is linked to LFE Channel. [7]: *Not Used.* [10:8]: Input Channel number that is linked to Surround Back Left Channel. [11]: *Not Used.* [14:12]: Input Channel number that is linked to Surround Back Right Channel. [15]: *Not Used.* *Default = 0x7654*

Register Name	Address	Word Length	Description
Input Mixer Configuration Registers			
FL_FR2FL_MIX_GAIN	0x34	2 Bytes	Front Left and Front Right into Front Left Mixing level register. Each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and other 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Left channel input into Front Left channel output mixing level. [15..8]: Front Right channel input into Front Left channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
C_M2FL_MIX_GAIN	0x35	2 Bytes	Center and MIC into Front Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Center channel input into Front Left channel output mixing level. [15..8]: MIC input into Front Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
FR_FL2FR_MIX_GAIN	0x36	2 Bytes	Front Right and Front Left into Front Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Right channel input into Front Right channel output mixing level. [15..8]: Front Left channel input into Front Right channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
C_M2FR_MIX_GAIN	0x37	2 Bytes	Center and MIC into Front Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Center channel input into Front Right channel output mixing level. [15..8]: MIC input into Front Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
SL_FL2SL_MIX_GAIN	0x38	2 Bytes	Surround Left and Front Left into Surround Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Left channel input into Surround Left channel output mixing level. [15..8]: Front Left channel input into Surround Left channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
FR_M2SL_MIX_GAIN	0x39	2 Bytes	Front Right and MIC into Surround Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Right channel input into Surround Left channel output mixing level. [15..8]: MIC input into Surround Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
SR_FL2SR_MIX_GAIN	0x3A	2 Bytes	Surround Right and Front Left into Surround Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Right channel input into Surround Right channel output mixing level. [15..8]: Front Left channel input into Surround Right channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
FR_M2SR_MIX_GAIN	0x3B	2 Bytes	Front Right and MIC into Surround Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Right channel input into Surround Right channel output mixing level. [15..8]: MIC input into Surround Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
C_FL2C_MIX_GAIN	0x3C	2 Bytes	Center and Front Left into Center Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Center channel input into Center channel output mixing level. [15..8]: Front Left channel input into Center channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
FR_M2C_MIX_GAIN	0x3D	2 Bytes	Front Right and MIC into Center Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Right channel input into Center channel output mixing level. [15..8]: MIC input into Center channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
SBL_SL2SBL_MIX_GAIN	0x3E	2 Bytes	Surround Back Left and Surround Left into Surround Back Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Back Left channel input into Surround Back Left channel output mixing level. [15..8]: Surround Left channel input into Surround Back Left channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
SR_SBR2SBL_MIX_GAIN	0x3F	2 Bytes	Surround Right and Surround Back Right into Surround Back Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Right channel input into Surround Back Left channel output mixing level. [15..8]: Surround Back Right channel input into Surround Back Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
SBR_SL2SBR_MIX_GAIN	0x40	2 Bytes	Surround Back Right and Surround Left into Surround Back Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Back Right channel input into Surround Back Right channel output mixing level. [15..8]: Surround Left channel input into Surround Back Right channel output mixing level. *Default = 0xFF24 (Mute, (+)0dB)*
SR_SBL2SBR_MIX_GAIN	0x41	2 Bytes	Surround Right and Surround Back Left into Surround Back Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Right channel input into Surround Back Right channel output mixing level. [15..8]: Surround Back Left channel input into Surround Back Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
M2SBL_SBR_MIX_GAIN	0x42	2 Bytes	MIC into Surround Back Left and Surround Back Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: MIC input into Surround Back Left channel output mixing level. [15..8]: MIC input into Surround Back Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
Down Mixer Configuration Registers			
FL_FR2LO_MIX_GAIN	0x43	2 Bytes	Front Left and Front Right into Downmix Left Mixing level register. Each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and other 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Left channel input into Downmix Left channel output mixing level. [15..8]: Front Right channel input into Downmix Left channel output mixing level. *Default = 0xFF40 (Mute, (+) -14dB)*
SL_SR2LO_MIX_GAIN	0x44	2 Bytes	Surround Left and Surround Right into Downmix Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Left channel input into Downmix Left channel output mixing level. [15..8]: Surround Right channel input into Downmix Left channel output mixing level. *Default = 0xC6C6 ((-) -17dB, (-) -17dB)*
C_LFE2LO_MIX_GAIN	0x45	2 Bytes	Center and LFE into Downmix Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Center channel input into Downmix Left channel output mixing level. [15..8]: LFE channel input into Downmix Left channel output mixing level. *Default = 0x3546 ((+) -8.5dB, (+) -17dB)*
SBL_SBR2LO_MIX_GAIN	0x46	2 Bytes	Surround Back Left and Surround Back Right into Downmix Left Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Back Left channel input into Downmix Left channel output mixing level. [15..8]: Surround Back Right channel input into Downmix Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
FL_FR2RO_MIX_GAIN	0x47	2 Bytes	Front Left and Front Right into Downmix Right Mixing level register. Each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and other 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Left channel input into Downmix Right channel output mixing level. [15..8]: Front Right channel input into Downmix Right channel output mixing level. *Default = 0x40FF ((+) -14dB, Mute)*
SL_SR2RO_MIX_GAIN	0x48	2 Bytes	Surround Left and Surround Right into Downmix Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Left channel input into Downmix Right channel output mixing level. [15..8]: Surround Right channel input into Downmix Right channel output mixing level. *Default = 0x4646 ((+) -17dB, (+) -17dB)*
C_LFE2RO_MIX_GAIN	0x49	2 Bytes	Center and LFE into Downmix Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Center channel input into Downmix Right channel output mixing level. [15..8]: LFE channel input into Downmix Right channel output mixing level. *Default = 0x3546 ((+) -8.5dB, (+) -17dB)*
SBL_SBR2RO_MIX_GAIN	0x4A	2 Bytes	Surround Back Left and Surround Back Right into Downmix Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Back Left channel input into Downmix Right channel output mixing level. [15..8]: Surround Back Right channel input into Downmix Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
MIC2LO_RO_MIX_GAIN	0x4B	2 Bytes	MIC into Downmix Left and Downmix Right Mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: MIC input into Downmix Left channel output mixing level. [15..8]: MIC input into Downmix Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
Equalizer Configuration Registers			
FL_FR_EQ_CONFIG	0x4C	2 Bytes	Front Left and Front Right channel Equalizer configuration Register. Equalizer Enable/Disable setting. "0" = Equalizer Disable. "1" = Equalizer Enable. Equalizer operation mode setting. "0" = Graphic EQ mode. In this mode, EQ level is effective. "1" = Static EQ mode. In this mode, EQ level is ineffective. [0]: Front Left channel Equalizer 1 Enable. *Default = "1" (Enable)* [1]: Front Left channel Equalizer 2 Enable. *Default = "1" (Enable)* [2]: Front Left channel Equalizer 3 Enable. *Default = "1" (Enable)* [3]: Front Left channel Equalizer 4 Enable. *Default = "0" (Disable)* [4]: Front Left channel Equalizer 1 Operation mode. *Default = "0" (Graphic)* [5]: Front Left channel Equalizer 2 Operation mode. *Default = "0" (Graphic)* [6]: Front Left channel Equalizer 3 Operation mode. *Default = "0" (Graphic)* [7]: Front Left channel Equalizer 4 Operation mode. *Default = "1" (Static)* [8]: Front Right channel Equalizer 1 Enable. *Default = "1" (Enable)* [9]: Front Right channel Equalizer 2 Enable. *Default = "1" (Enable)* [10]: Front Right channel Equalizer 3 Enable. *Default = "1" (Enable)* [11]: Front Right channel Equalizer 4 Enable. *Default = "0" (Disable)* [12]: Front Right channel Equalizer 1 Operation mode. *Default = "0" (Graphic)* [13]: Front Right channel Equalizer 2 Operation mode. *Default = "0" (Graphic)* [14]: Front Right channel Equalizer 3 Operation mode. *Default = "0" (Graphic)* [15]: Front Right channel Equalizer 4 Operation mode. *Default = "1" (Static)* *Default = 0x8787*
SL_SR_EQ_CONFIG	0x4D	2 Bytes	Surround Left and Surround Right channel Equalizer configuration Register. [0]: Surround Left channel Equalizer 1 Enable. *Default = "1" (Enable)* [1]: Surround Left channel Equalizer 2 Enable. *Default = "1" (Enable)* [2]: Surround Left channel Equalizer 3 Enable. *Default = "1" (Enable)* [3]: Surround Left channel Equalizer 4 Enable. *Default = "0" (Disable)* [4]: Surround Left channel Equalizer 1 Operation mode. *Default = "0" (Graphic)* [5]: Surround Left channel Equalizer 2 Operation mode. *Default = "0" (Graphic)* [6]: Surround Left channel Equalizer 3 Operation mode. *Default = "0" (Graphic)* [7]: Surround Left channel Equalizer 4 Operation mode. *Default = "1" (Static)* [8]: Surround Right channel Equalizer 1 Enable. *Default = "1" (Enable)* [9]: Surround Right channel Equalizer 2 Enable. *Default = "1" (Enable)* [10]: Surround Right channel Equalizer 3 Enable. *Default = "1" (Enable)* [11]: Surround Right channel Equalizer 4 Enable. *Default = "0" (Disable)* [12]: Surround Right channel Equalizer 1 Operation mode. *Default = "0" (Graphic)* [13]: Surround Right channel Equalizer 2 Operation mode. *Default = "0" (Graphic)* [14]: Surround Right channel Equalizer 3 Operation mode. *Default = "0" (Graphic)* [15]: Surround Right channel Equalizer 4 Operation mode. *Default = "1" (Static)* *Default = 0x8787*

Register Name	Address	Word Length	Description
C_HP_LR_EQ_CONFIG	0x4E	2 Bytes	Center and Headphone Left/Right channel Equalizer configuration Register. [0]: Center channel Equalizer 1 Enable. *Default = "1" (Enable)* [1]: Center channel Equalizer 2 Enable. *Default = "1" (Enable)* [2]: Center channel Equalizer 3 Enable. *Default = "1" (Enable)* [3]: Center channel Equalizer 4 Enable. *Default = "0" (Disable)* [4]: Center channel Equalizer 1 Operation mode. *Default = "0" (Graphic)* [5]: Center channel Equalizer 2 Operation mode. *Default = "0" (Graphic)* [6]: Center channel Equalizer 3 Operation mode. *Default = "0" (Graphic)* [7]: Center channel Equalizer 4 Operation mode. *Default = "1" (Static)* [8]: Headphone Left channel Equalizer 1 Enable. *Default = "1" (Enable)* [9]: Headphone Left channel Equalizer 2 Enable. *Default = "1" (Enable)* [10]: Headphone Left channel Equalizer 3 Enable. *Default = "1" (Enable)* [11]: Headphone Left channel Equalizer 4 Enable. *Default = "0" (Disable)* [12]: Headphone Right channel Equalizer 1 Enable. *Default = "1" (Enable)* [13]: Headphone Right channel Equalizer 2 Enable. *Default = "1" (Enable)* [14]: Headphone Right channel Equalizer 3 Enable. *Default = "1" (Enable)* [15]: Headphone Right channel Equalizer 4 Enable. *Default = "0" (Disable)* *Default = 0x7787*
SBL_SBR_EQ_CONFIG	0x4F	2 Bytes	Surround Back Left/Right channel Equalizer configuration Register. [0]: Surround Back Left channel Equalizer 1 Enable. *Default = "1" (Enable)* [1]: Surround Back Left channel Equalizer 2 Enable. *Default = "1" (Enable)* [2]: Surround Back Left channel Equalizer 3 Enable. *Default = "1" (Enable)* [3]: Surround Back Left channel Equalizer 4 Enable. *Default = "0" (Disable)* [4]: Surround Back Left channel Equalizer 1 Operation mode. *Default = "0" (Graphic)* [5]: Surround Back Left channel Equalizer 2 Operation mode. *Default = "0" (Graphic)* [6]: Surround Back Left channel Equalizer 3 Operation mode. *Default = "0" (Graphic)* [7]: Surround Back Left channel Equalizer 4 Operation mode. *Default = "1" (Static)* [8]: Surround Back Right channel Equalizer 1 Enable. *Default = "1" (Enable)* [9]: Surround Back Right channel Equalizer 2 Enable. *Default = "1" (Enable)* [10]: Surround Back Right channel Equalizer 3 Enable. *Default = "1" (Enable)* [11]: Surround Back Right channel Equalizer 4 Enable. *Default = "0" (Disable)* [12]: Surround Back Right channel Equalizer 1 Operation mode. *Default = "0" (Graphic)* [13]: Surround Back Right channel Equalizer 2 Operation mode. *Default = "0" (Graphic)* [14]: Surround Back Right channel Equalizer 3 Operation mode. *Default = "0" (Graphic)* [15]: Surround Back Right channel Equalizer 4 Operation mode. *Default = "1" (Static)* *Default = 0x8787*

Register Name	Address	Word Length	Description
Equalizer Level Control Registers			
EQ_FL12_LEVEL	0x55	2 Bytes	Front Left channel Equalizer 1, 2 level register. -12dB to 12dB in 1dB/step resolution. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Front Left channel Equalizer 1 level. [5]: Front Left channel Equalizer 1 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Front Left channel Equalizer 2 level. [13]: Front Left channel Equalizer 2 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_FL34_LEVEL	0x56	2 Bytes	Front Left channel Equalizer 3, 4 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Front Left channel Equalizer 3 level. [5]: Front Left channel Equalizer 3 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Front Left channel Equalizer 4 level. [13]: Front Left channel Equalizer 4 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_FR12_LEVEL	0x57	2 Bytes	Front Right channel Equalizer 1, 2 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Front Right channel Equalizer 1 level. [5]: Front Right channel Equalizer 1 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Front Right channel Equalizer 2 level. [13]: Front Right channel Equalizer 2 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*

Register Name	Address	Word Length	Description
EQ_FR34_LEVEL	0x58	2 Bytes	Front Right channel Equalizer 3, 4 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Front Right channel Equalizer 3 level. [5]: Front Right channel Equalizer 3 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Front Right channel Equalizer 4 level. [13]: Front Right channel Equalizer 4 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_SL12_LEVEL	0x59	2 Bytes	Surround Left channel Equalizer 1, 2 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Left channel Equalizer 1 level. [5]: Surround Left channel Equalizer 1 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Left channel Equalizer 2 level. [13]: Surround Left channel Equalizer 2 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_SL34_LEVEL	0x5A	2 Bytes	Surround Left channel Equalizer 3, 4 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Left channel Equalizer 3 level. [5]: Surround Left channel Equalizer 3 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Left channel Equalizer 4 level. [13]: Surround Left channel Equalizer 4 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*

Register Name	Address	Word Length	Description
EQ_SR12_LEVEL	0x5B	2 Bytes	Right surround channel Equalizer 1, 2 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Right channel Equalizer 1 level. [5]: Surround Right channel Equalizer 1 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Right channel Equalizer 2 level. [13]: Surround Right channel Equalizer 2 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_SR34_LEVEL	0x5C	2 Bytes	Surround Right channel Equalizer 3, 4 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Right channel Equalizer 3 level. [5]: Surround Right channel Equalizer 3 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Right channel Equalizer 4 level. [13]: Surround Right channel Equalizer 4 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_C12_LEVEL	0x5D	2 Bytes	Center channel Equalizer 1, 2 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Center channel Equalizer 1 level. [5]: Center channel Equalizer 1 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Center channel Equalizer 2 level. [13]: Center channel Equalizer 2 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*

Register Name	Address	Word Length	Description
EQ_C34_LEVEL	0x5E	2 Bytes	Center channel Equalizer 3, 4 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Center channel Equalizer 3 level. [5]: Center channel Equalizer 3 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Center channel Equalizer 4 level. [13]: Center channel Equalizer 4 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_SBL12_LEVEL	0x5F	2 Bytes	Surround Back Left channel Equalizer 1, 2 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Back Left channel Equalizer 1 level. [5]: Surround Back Left channel Equalizer 1 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Back Left channel Equalizer 2 level. [13]: Surround Back Left channel Equalizer 2 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_SBL34_LEVEL	0x60	2 Bytes	Surround Back Left channel Equalizer 3, 4 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Back Left channel Equalizer 3 level. [5]: Surround Back Left channel Equalizer 3 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Back Left channel Equalizer 4 level. [13]: Surround Back Left channel Equalizer 4 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*

Register Name	Address	Word Length	Description
EQ_SBR12_LEVEL	0x61	2 Bytes	Right Back surround channel Equalizer 1, 2 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Back Right channel Equalizer 1 level. [5]: Surround Back Right channel Equalizer 1 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Back Right channel Equalizer 2 level. [13]: Surround Back Right channel Equalizer 2 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*
EQ_SBR34_LEVEL	0x62	2 Bytes	Surround Back Right channel Equalizer 3, 4 level register. Table A-4 shows the relations between the register value and Equalizer level. [4..0]: Surround Back Right channel Equalizer 3 level. [5]: Surround Back Right channel Equalizer 3 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [7..6]: *Not Used.* [12..8]: Surround Back Right channel Equalizer 4 level. [13]: Surround Back Right channel Equalizer 4 Filter Coefficients set Select. "0" for Primary Coefficients set and "1" for Secondary Coefficients set. *Default = "0" (Primary coefficients set)* [15..14]: *Not Used.* *Default = 0x0000 (Primary, 0dB, Primary, 0dB)*

Register Name	Address	Word Length	Description
Sound Processing Sequence Configuration Registers			
EQ_HPF_BM_SEQ_SEL	0x63	2 Bytes	Equalizer, High-pass Filter, Volume & Bass Management sequence selection. [1..0]: Processing Sequence Selection. *Default = "00".* "00" = 3 Band Equalizer → HPF → Volume & Bass Management "01" = 4 Band Equalizer → Volume & Bass Management "10" = HPF → Volume & Bass Management → 3 Band Equalizer "11" = Volume & Bass Management → 4 Band Equalizer [15..2]: *Not Used*. *Default = 0x0000*
Bass Processing Path & Other Signal Path Control Registers			
BM_CONFIG	0x64	2 Bytes	Bass processing path & other signal path control Register [0]: Subwoofer output path selection control. "0" = Bass Sum is sent to Subwoofer output. "1" = LFE channel is sent to Subwoofer output. *Default = "1" (LFE channel to Subwoofer).* [1]: Bass Sum filter bypass control. *Default = "0" (Filter Enable).* "0" = Filter Enable "1" = Bypass (Filter Disable). [3..2]: *Not Used*. [4]: Bass Sum Filter 1 enable control. *Default = "1" (Filter Enable).* "0" = Disable. "1" = Enable. [5]: Bass Sum Filter 2 enable control. *Default = "1" (Filter Enable).* "0" = Disable. "1" = Enable. [6]: Bass Sum Filter 3 enable control. *Default = "0" (Filter Disable).* "0" = Disable. "1" = Enable. [7]: Bass Sum Filter 4 enable control. *Default = "0" (Filter Disable).* "0" = Disable. "1" = Enable. [10..8]: Headphone output source selection control. *Default = "100" (Downmix).* "000" = Front Left & Front Right channel to HeadPhone output "001" = Surround Left & Surround Right channel to HeadPhone output "010" = Center & LFE channel to HeadPhone output "011" = Surround Back Left & Surround Back Right channel to HeadPhone output "1xx" = Downmix output to HeadPhone output [11]: *Not Used*. [13..12]: PCM output path selection control. *Default = "01" (1 Band EQ).* "00" = 3 band EQ to PCM output "01" = 1 band EQ to PCM output "1x" = Volume & BM to PCM output [14]: *Not Used*. [15]: SBL & SBR channel source selection control. *Default = "0" (SBL & SBR).* '0' = SBL & SBR channel mixer output to SBL, SBR output '1' = LO & RO downmix output to SBL, SBR output *Default = 0x1431*

Register Name	Address	Word Length	Description
Bass Sum Mixer Configuration Registers			
BM_FL_FR2SUM_GAIN	0x65	2 Bytes	Front Left and Front Right channel into Bass Sum mixing level register. Each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and other 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Left channel input into Bass Sum mixing level. [15..8]: Front Right channel input into Bass Sum mixing level. *Default = 0x2424 ((+) 0dB, (+) 0dB)*
BM_SL_SR2SUM_GAIN	0x66	2 Bytes	Surround Left and Surround Right channel into Bass Sum mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Left channel input into Bass Sum mixing level. [15..8]: Surround Right channel input into Bass Sum mixing level. *Default = 0x2424 ((+) 0dB, (+) 0dB)*
BM_C_LFE2SUM_GAIN	0x67	2 Bytes	Center and LFE channel into Bass Sum mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Center channel input into Bass Sum mixing level. [15..8]: LFE channel input into Bass Sum mixing level. *Default = 0x1024 ((+) 10dB, (+) 0dB)*
BM_SBL_SBR2SUM_GAIN	0x68	2 Bytes	Surround Back Left and Surround Back Right channel into Bass Sum mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Back Left channel input into Bass Sum mixing level. [15..8]: Surround Back Right channel input into Bass Sum mixing level. *Default = 0x2424 ((+) 0dB, (+) 0dB)*

Register Name	Address	Word Length	Description
Input Mixer Configuration Registers (Addendum)			
SL_SBL2L_MIX_GAIN	0x69	2 Bytes	Surround Left and Surroud Back Left into Front Left Mixing level register. Each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and other 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Left channel input into Front Left channel output mixing level. [15..8]: Surround Back Left channel input into Front Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
SR_SBR2R_MIX_GAIN	0x6A	2 Bytes	Surround Right and Surroud Back Right into Front Right Mixing level register. Each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and other 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Right channel input into Front Right channel output mixing level. [15..8]: Surround Back Right channel input into Front Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
SBL2SL_SBR2SR_MIX	0x6B	2 Bytes	Surroud Back Left into Surround Left Mixing level and Surround Back Right into Surroud Right Mixing level register. Each mixing level register consists of mixing polarity (1-bit) and mixing level coefficient (7-bit). MSB is the mixing polarity (“0” : +, “1” : -) and other 7-bit is the mixing level coefficient. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surroud Back Left channel input into Surround Left channel output mixing level. [15..8]: Surroud Back Right channel input into Surround Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
Bass Management Configuration Registers			
BM_FL2FL_GAIN	0x70	2 Bytes	Front Left channel input into Front Left channel pass-through mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Left channel input into Front Left channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFE_SUM2FL_GAIN	0x71	2 Bytes	LFE channel and Bass Sum into Front Left channel output mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Front Left channel output mixing level. [15..8]: Bass Sum into Front Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_FR2FR_GAIN	0x72	2 Bytes	Front Right channel input into Front Right channel pass-through mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Front Right channel input into Front Right channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFE_SUM2FR_GAIN	0x73	2 Bytes	LFE channel and Bass Sum into Front Right channel output mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Front Right channel output mixing level. [15..8]: Bass Sum into Front Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_SL2SL_GAIN	0x74	2 Bytes	Surround Left channel input into Surround Left channel pass-through mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Left channel input into Surround Left channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFE_SUM2SL_GAIN	0x75	2 Bytes	LFE channel and Bass Sum into Surround Left channel output mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Surround Left channel output mixing level. [15..8]: Bass Sum into Surround Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
BM_SR2SR_GAIN	0x76	2 Bytes	Surround Right channel input into Surround Right channel pass-through mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Right channel input into Surround Right channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFE_SUM2SR_GAIN	0x77	2 Bytes	LFE channel and Bass Sum into Surround Right channel output mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Surround Right channel output mixing level. [15..8]: Bass Sum into Surround Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_C2C_GAIN	0x78	2 Bytes	Center channel input into Center channel pass-through mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Center channel input into Center channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFE_SUM2C_GAIN	0x79	2 Bytes	LFE channel and Bass Sum into Center channel output mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Center channel output mixing level. [15..8]: Bass Sum into Center channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_SBL2SBL_GAIN	0x7A	2 Bytes	Surround Back Left channel input into Surround Back Left channel pass-through mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Back Left channel input into Surround Back Left channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFE_SUM2SBL_GAIN	0x7B	2 Bytes	LFE channel and Bass Sum into Surround Back Left channel output mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Surround Back Left channel output mixing level. [15..8]: Bass Sum into Surround Back Left channel output mixing level. *Default = 0xFFFF (Mute, Mute)*

Register Name	Address	Word Length	Description
BM_SBR2SBR_GAIN	0x7C	2 Bytes	Surround Back Right channel input into Surround Back Right channel pass-through mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: Surround Back Right channel input into Surround Back Right channel pass-through mixing level. [15..8]: *Not Used*. *Default = 0x0024 ((+) 0dB)*
BM_LFE_SUM2SBR_GAIN	0x7D	2 Bytes	LFE channel and Bass Sum into Surround Back Right channel output mixing level register. Table A-3 shows the relations between the register value and mixing level. [7..0]: LFE channel input into Surround Back Right channel output mixing level. [15..8]: Bass Sum into Surround Back Right channel output mixing level. *Default = 0xFFFF (Mute, Mute)*
BM_LFE_SUM_GAIN	0x7E	2 Bytes	LFE channel and Bass Sum into Subwoofer output bypass level register. Table A-3 shows the relations between the register value and bypass level. [7..0]: LFE into Subwoofer output bypass level. This is effective when LFE channel input is bypassed to Subwoofer output. [15..8]: Bass Sum into Subwoofer output level. This is effective when Bass Sum is passed to Subwoofer output. *Default = 0x2410 ((+) 0dB, (+) 10dB)*

Register Name	Address	Word Length	Description
PWM Modulator Control Registers			
PWM_CONTROL	0x80	2 Bytes	PWM modulator control register. [1:0]: Modulation index (PCM to PWM gain). *Default = "01" (93.75%).* "00" = 90.63%, "01" = 93.75%, "10" = 96.88% [2]: Auto DC cut enable. Active high. *Default = "1" (Enable).* [3]: Dither enable. "0" = Dither disable, "1" = Dither enable. *Default = "0".* [4]: High S/N mode enable. "0" = Normal mode, "1" = High S/N mode. *Default = "0".* [5]: High bandwidth Noise shaping filter enable. *Default = "0".* "0" = Normal mode, "1'" = High bandwidth N/S filter enable. [7:6]: Switching Frequency. *Default = "00".* "00", "11" = 384KHz "01" = 192KHz "10" = 96KHz [15:8]: *Reserved.* *Default = 0x0005*
PWM_LIMIT1	0x81	2 Bytes	PWM Modulation Limit control register 1. This control register limits the minimum PWM pulse width. - resolution : 10ns. - range : 20ns ~ 170ns - Minimum PWM pulse width : (user setting value + 2) * 10ns. [3:0]: PWM 1 Modulation limit. *Default = "0110" (80ns).* [7:4]: PWM 2 Modulation limit. *Default = "0110" (80ns).* [11:8]: PWM 3 Modulation limit. *Default = "0110" (80ns).* [15:12]: PWM 4 Modulation limit. *Default = "0110" (80ns).* *Default = 0x6666*
PWM_LIMIT2	0x82	2 Bytes	PWM Modulation Limit control register 2. This control register limits the minimum PWM pulse width. - resolution : 10ns. - range : 20ns ~ 170ns - Minimum PWM pulse width : (user setting value + 2) * 10ns. [3:0]: PWM 5 Modulation limit. *Default = "0110" (80ns).* [7:4]: PWM 6 Modulation limit. *Default = "0110" (80ns).* [11:8]: PWM 7 Modulation limit. *Default = "0110" (80ns).* [15:12]: PWM 8 Modulation limit. *Default = "0110" (80ns).* *Default = 0x6666*

Register Name	Address	Word Length	Description
PWM_DEADTIME1	0x83	2 Bytes	PWM Deadtime (between positive and negative PWM signal) control register 1. - resolution : 5ns. - range : 0ns ~ 75ns - Deadtime : (user setting value) * 5ns. [3:0]: PWM 1 Deadtime. *Default = "0000" (0ns).* [7:4]: PWM 2 Deadtime. *Default = "0000" (0ns).* [11:8]: PWM 3 Deadtime. *Default = "0000" (0ns).* [15:12]: PWM 4 Deadtime. *Default = "0000" (0ns).* *Default = 0x0000*
PWM_DEADTIME2	0x84	2 Bytes	PWM Deadtime (between positive and negative PWM signal) control register 2. [3:0]: PWM 5 Deadtime. *Default = "0000" (0ns).* [7:4]: PWM 6 Deadtime. *Default = "0000" (0ns).* [11:8]: PWM 7 Deadtime. *Default = "0000" (0ns).* [15:12]: PWM 8 Deadtime. *Default = "0000" (0ns).* *Default = 0x0000*
OUTPUT_CH_MAPPING1	0x85	2 Bytes	Internal processing channel into output PWM Mapping register 1. "000" : Front Left channel (FL) "001" : Front Right channel (FR) "010" : Surround Left channel (SL) "011" : Surround Right channel (SR) "100" : Center channel (C) "101" : Subwoofer channel (SW) "110" : Surround Back Left channel (SBL) "111" : Surround Back Right channel (SBR) [2:0]: Internal processing channel which is linked to PWM 1. *Default = "111" (SBR).* [3]: *Reserved.* [6:4]: Internal processing channel which is linked to PWM 2. *Default = "110" (SBL).* [7]: *Reserved.* [10:8]: Internal processing channel which is linked to PWM 3. *Default = "011" (SR).* [11]: *Reserved.* [14:12]: Internal processing channel which is linked to PWM 4. *Default = "001" (FR).* [15]: *Reserved.* *Default = 0x1367*
OUTPUT_CH_MAPPING2	0x86	2 Bytes	Internal processing channel into output PWM Mapping register 2. [2:0]: Internal processing channel which is linked to PWM 5. *Default = "101" (SW).* [3]: *Reserved.* [6:4]: Internal processing channel which is linked to PWM 6. *Default = "100" (C).* [7]: *Reserved.* [10:8]: Internal processing channel which is linked to PWM 7. *Default = "010" (SL).* [11]: *Reserved.* [14:12]: Internal processing channel which is linked to PWM 8. *Default = "000" (FL).* [15]: *Reserved.* *Default = 0x0245*

Register Name	Address	Word Length	Description
HEADPHONE_CONTROL	0x87	2 Bytes	Headphone output control register. [0]: Surround Left channel Off when Headphone mode is On. *Default = "1" (Off).* [1]: Surround Right channel Off when Headphone mode is On. *Default = "1" (Off).* [2]: Center channel Off when Headphone mode is On. *Default = "1" (Off).* [3]: Subwoofer channel Off when Headphone mode is On. *Default = "1" (Off).* [4]: Surround Back Left channel Off when Headphone mode is On. *Default = "1" (Off).* [5]: Surround Back Right channel Off when Headphone mode is On. *Default = "1" (Off).* [6]: Subwoofer Lineout channel Off when Headphone mode is On. *Default = "1" (Off).* [7]: *Reserved.* [8]: Headphone mode On/Off. *Default = "0" (Off).* [15:9]: *Not Used*. *Default = 0x007F*
OVERLOAD_CONTROL	0x88	2 Bytes	Overload status monitoring register. [6:0]: Overload detection time. 0.667ms/step. *Default = "0001111" (10ms)* [7]: Overload input signal polarity. *Default = "1"* "0" = Active Low, "1" = Active High. [13:8]: Overload sustained time. When overload condition is detected, all PWM outputs go to shutdown during assigned time. *Default = "100000" (2.73sec)* "000000" = No shutdown. "000001" ~ "111110" = multiple of 0.0853sec. "111111" = No recovery. To recover PWM signal, set the PWM_ON_OFF register (0x00) to "1" (PWM off) and then "0" (PWM on). [14]: *Not Used.* [15]: Overload monitoring bit. Active High. Overload Sustained time = "000000" : external overload monitoring bit Overload Sustained time /= "000000" : internal overload monitoring bit *Default = 0x208F*
EPD_CONTROL	0x89	2 Bytes	EPD_ENA (External Power Device Enable) output timing control register. [6:0]: EPD_ENA proceeding time (multiple of 5.33ms). This register bits are effective when the lower EPD_ENA control type is set to "1". *Default = "0000001" (5.33ms).* [7]: EPD_ENA control type. *Default = "1" (Linkage upon Global Off control).* "0" = User direct control. "1" = Linkage upon Global Off control. EPD_ENA output can be controlled by Global Off/On control bit in PWM_ON_OFF register (0x00). [8]: User EPD_ENA output status setting register. This register bit is effective when the upper EPD_ENA control type is set to "0". *Default = "0"* [15:9]: *Not Used.* *Default = 0x0081*

Register Name	Address	Word Length	Description
POP_CONTROL	0x8A	2 Bytes	PWM On/Off sequence timing control register. [7:0]: Soft PWM start time (multiple of 0.667ms). *Default = "00010000" (10.67ms).* [15:8]: Minimum PWM pulse time (multiple of 0.083ms). *Default = "10000000" (10ms).* *Default = 0x8010*
OVERLOAD_LINKAGE	0x8B	2 Bytes	Overload linkage control register. "0" = Overload Linkage Off "1" = Overload Linkage On [0]: Subwoofer Lineout channel. *Default = "0" (Linkage Off).* [4]: Headphone Left channel. *Default = "0" (Linkage Off).* [5]: Headphone Right channel. *Default = "0" (Linkage Off).* [8]: PWM 1. *Default = "1" (Linkage On).* [9]: PWM 2. *Default = "1" (Linkage On).* [10]: PWM 3. *Default = "1" (Linkage On).* [11]: PWM 4. *Default = "1" (Linkage On).* [12]: PWM 5. *Default = "1" (Linkage On).* [13]: PWM 6. *Default = "1" (Linkage On).* [14]: PWM 7. *Default = "1" (Linkage On).* [15]: PWM 8. *Default = "1" (Linkage On).* *Default = 0xFF00*

Register Name	Address	Word Length	Description
Coefficient for Primary Equalizing Filters Registers			
EQ_P_EQ1_A1	0xA0	3 Bytes	-A1 coefficient for Primary Equalizing filter 1. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FCA47 (Coefficient for 150Hz +6dB peaking filter)*
EQ_P_EQ1_A2	0xA1	3 Bytes	-A2 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE03587 (Coefficient for 150Hz +6dB peaking filter)*
EQ_P_EQ1_B0	0xA2	3 Bytes	B0 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x001AC3 (Coefficient for 150Hz +6dB peaking filter)*
EQ_P_EQ1_B1	0xA3	3 Bytes	B1 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (Coefficient for 150Hz +6dB peaking filter)*
EQ_P_EQ1_B2	0xA4	3 Bytes	B2 coefficient for Primary Equalizing filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFFE53D (Coefficient for 150Hz +6dB peaking filter)*
EQ_P_EQ2_A1	0xA5	3 Bytes	-A1 coefficient for Primary Equalizing filter 2. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3E9908 (Coefficient for 1kHz +6dB peaking filter)*
EQ_P_EQ2_A2	0xA6	3 Bytes	-A2 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE15E62 (Coefficient for 1kHz +6dB peaking filter)*
EQ_P_EQ2_B0	0xA7	3 Bytes	B0 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x00AF31 (Coefficient for 1kHz +6dB peaking filter)*
EQ_P_EQ2_B1	0xA8	3 Bytes	B1 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (Coefficient for 1kHz +6dB peaking filter)*
EQ_P_EQ2_B2	0xA9	3 Bytes	B2 coefficient for Primary Equalizing filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFF50CF (Coefficient for 1kHz +6dB peaking filter)*

Register Name	Address	Word Length	Description
EQ_P_EQ3_A1	0xAA	3 Bytes	-A1 coefficient for Primary Equalizing filter 3. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x349361 (Coefficient for 8kHz +6dB peaking filter)*
EQ_P_EQ3_A2	0xAB	3 Bytes	-A2 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE991D4 (Coefficient for 8kHz +6dB peaking filter)*
EQ_P_EQ3_B0	0xAC	3 Bytes	B0 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x04C8EA (Coefficient for 8kHz +6dB peaking filter)*
EQ_P_EQ3_B1	0xAD	3 Bytes	B1 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (Coefficient for 8kHz +6dB peaking filter)*
EQ_P_EQ3_B2	0xAE	3 Bytes	B2 coefficient for Primary Equalizing filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFB3716 (Coefficient for 8kHz +6dB peaking filter)*
EQ_P_EQ4_A1	0xAF	3 Bytes	-A1 coefficient for Primary Equalizing filter 4. The filter is a bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FDA16 (Coefficient for 100Hz High pass filter)*
EQ_P_EQ4_A2	0xB0	3 Bytes	-A2 coefficient for Primary Equalizing filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE025D3 (Coefficient for 100Hz High pass filter)*
EQ_P_EQ4_B0	0xB1	3 Bytes	B0 coefficient for Primary Equalizing filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FED11 (Coefficient for 100Hz High pass filter)*
EQ_P_EQ4_B1	0xB2	3 Bytes	B1 coefficient for Primary Equalizing filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xC025DE (Coefficient for 100Hz High pass filter)*
EQ_P_EQ4_B2	0xB3	3 Bytes	B2 coefficient for Primary Equalizing filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FED11 (Coefficient for 100Hz High pass filter)*

Register Name	Address	Word Length	Description
Coefficient for Secondary Equalizing Filters Registers			
EQ_S_EQ1_A1	0xB4	3 Bytes	-A1 coefficient for Secondary Equalizing Filter 1. The filter is a 30-bit bi-quad filter. Coefficient A0 is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3F955A (Coefficient for 150Hz -6dB peaking filter)*
EQ_S_EQ1_A2	0xB5	3 Bytes	-A2 coefficient for Secondary Equalizing Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE06A74 (Coefficient for 150Hz -6dB peaking filter)*
EQ_S_EQ1_B0	0xB6	3 Bytes	B0 coefficient for Secondary Equalizing Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x00353A (Coefficient for 150Hz -6dB peaking filter)*
EQ_S_EQ1_B1	0xB7	3 Bytes	B1 coefficient for Secondary Equalizing Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (Coefficient for 150Hz -6dB peaking filter)*
EQ_S_EQ1_B2	0xB8	3 Bytes	B2 coefficient for Secondary Equalizing Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFFCAC6 (Coefficient for 150Hz -6dB peaking filter)*
EQ_S_EQ2_A1	0xB9	3 Bytes	-A1 coefficient for Secondary Equalizing Filter 2. The filter is a 30-bit bi-quad filter. Coefficient A0 is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3D4B0F (Coefficient for 1kHz -6dB peaking filter)*
EQ_S_EQ2_A2	0xBA	3 Bytes	-A2 coefficient for Secondary Equalizing Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE2AC8A (Coefficient for 1kHz -6dB peaking filter)*
EQ_S_EQ2_B0	0xBB	3 Bytes	B0 coefficient for Secondary Equalizing Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x015645 (Coefficient for 1kHz -6dB peaking filter)*
EQ_S_EQ2_B1	0xBC	3 Bytes	B1 coefficient for Secondary Equalizing Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (Coefficient for 1kHz -6dB peaking filter)*
EQ_S_EQ2_B2	0xBD	3 Bytes	B2 coefficient for Secondary Equalizing Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xFEA9BB (Coefficient for 1kHz -6dB peaking filter)*

Register Name	Address	Word Length	Description
EQ_S_EQ3_A1	0xBE	3 Bytes	-A1 coefficient for Secondary Equalizing Filter 3. The filter is a 30-bit bi-quad filter. Coefficient A0 is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x2DC3DB (Coefficient for 8kHz -6dB peaking filter)*
EQ_S_EQ3_A2	0xBF	3 Bytes	-A2 coefficient for Secondary Equalizing Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xF09EDA (Coefficient for 8kHz -6dB peaking filter)*
EQ_S_EQ3_B0	0xC0	3 Bytes	B0 coefficient for Secondary Equalizing Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x084F6D (Coefficient for 8kHz -6dB peaking filter)*
EQ_S_EQ3_B1	0xC1	3 Bytes	B1 coefficient for Secondary Equalizing Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000 (Coefficient for 8kHz -6dB peaking filter)*
EQ_S_EQ3_B2	0xC2	3 Bytes	B2 coefficient for Secondary Equalizing Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xF7B093 (Coefficient for 8kHz -6dB peaking filter)*
EQ_S_EQ4_A1	0xC3	3 Bytes	-A1 coefficient for Secondary Equalizing Filter 4. The filter is a 30-bit bi-quad filter. Coefficient A0 is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
EQ_S_EQ4_A2	0xC4	3 Bytes	-A2 coefficient for Secondary Equalizing Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
EQ_S_EQ4_B0	0xC5	3 Bytes	B0 coefficient for Secondary Equalizing Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
EQ_S_EQ4_B1	0xC6	3 Bytes	B1 coefficient for Secondary Equalizing Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*
EQ_S_EQ4_B2	0xC7	3 Bytes	B2 coefficient for Secondary Equalizing Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000000*

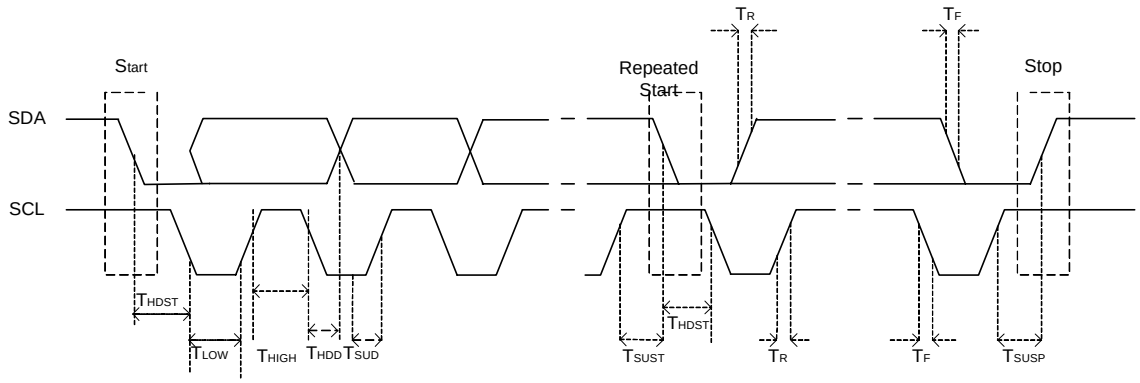
Register Name	Address	Word Length	Description
Coefficient for Bass Sum Filters Registers			
BSUM_FILTER1_A1	0xC8	3 Bytes	-A1 coefficient for Bass Sum Filter 1. The bass sum filters consist of user-programmable 4 cascaded 30-bit bi-quad filters. Each filter configured into any kind of filter such as low-pass fitler, high-pass filter, band-pass filter and notch filter. A0 coefficient is fixed at value 1. Sampling Frequency of the filter is 192KHz. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FDA16 (100Hz Low pass filter)*
BSUM_FILTER1_A2	0xC9	3 Bytes	-A2 coefficient for Bass Sum Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE025D3 (100Hz Low pass filter)*
BSUM_FILTER1_B0	0xCA	3 Bytes	B0 coefficient for Bass Sum Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000006 (100Hz Low pass filter)*
BSUM_FILTER1_B1	0xCB	3 Bytes	B1 coefficient for Bass Sum Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x00000C (100Hz Low pass filter)*
BSUM_FILTER1_B2	0xCC	3 Bytes	B2 coefficient for Bass Sum Filter 1. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000006 (100Hz Low pass filter)*
BSUM_FILTER2_A1	0xCD	3 Bytes	-A1 coefficient for Bass Sum Filter 2. The filter is a 30-bit bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FDA16 (100Hz Low pass filter)*
BSUM_FILTER2_A2	0xCE	3 Bytes	-A2 coefficient for Bass Sum Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE025D3 (100Hz Low pass filter)*
BSUM_FILTER2_B0	0xCF	3 Bytes	B0 coefficient for Bass Sum Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000006 (100Hz Low pass filter)*
BSUM_FILTER2_B1	0xD0	3 Bytes	B1 coefficient for Bass Sum Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x00000C (100Hz Low pass filter)*
BSUM_FILTER2_B2	0xD1	3 Bytes	B2 coefficient for Bass Sum Filter 2. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x000006 (100Hz Low pass filter)*

Register Name	Address	Word Length	Description
BSUM_FILTER3_A1	0xD2	3 Bytes	-A1 coefficient for Bass Sum Filter 3. The filter is a 30-bit bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FF86B (20Hz High pass filter)*
BSUM_FILTER3_A2	0xD3	3 Bytes	-A2 coefficient for Bass Sum Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE00794 (20Hz High pass filter)*
BSUM_FILTER3_B0	0xD4	3 Bytes	B0 coefficient for Bass Sum Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FFC36 (20Hz High pass filter)*
BSUM_FILTER3_B1	0xD5	3 Bytes	B1 coefficient for Bass Sum Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xC00794 (20Hz High pass filter)*
BSUM_FILTER3_B2	0xD6	3 Bytes	B2 coefficient for Bass Sum Filter 3. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FFC36 (20Hz High pass filter)*
BSUM_FILTER4_A1	0xD7	3 Bytes	-A1 coefficient for Bass Sum Filter 4. The filter is a 30-bit bi-quad filter. A0 coefficient is fixed at value 1. $H(z) = (B0 + B1 \cdot z^{-1} + B2 \cdot z^{-2}) / (1 + A1 \cdot z^{-1} + A2 \cdot z^{-2})$ Sampling Frequency of the filter is 192KHz. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x3FF4A0 (30Hz High pass filter)*
BSUM_FILTER4_A2	0xD8	3 Bytes	-A2 coefficient for Bass Sum Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xE00B5E (30Hz High pass filter)*
BSUM_FILTER4_B0	0xD9	3 Bytes	B0 coefficient for Bass Sum Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FFA51 (30Hz High pass filter)*
BSUM_FILTER4_B1	0xDA	3 Bytes	B1 coefficient for Bass Sum Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0xC00B5E (30Hz High pass filter)*
BSUM_FILTER4_B2	0xDB	3 Bytes	B2 coefficient for Bass Sum Filter 4. 3.21 format (3 bits for the integer part and 21 bits for the fractional part). *Default = 0x1FFA51 (30Hz High pass filter)*

AC Characteristics

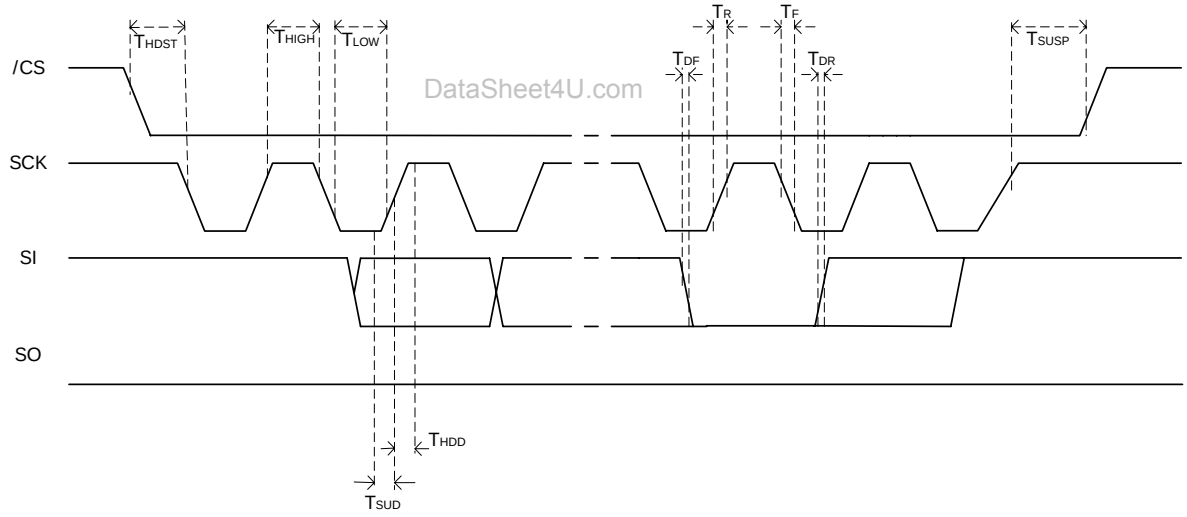
1. I²C Control Interface Timing

Parameter	Symbol	Min	-	Max	Units
SCL Clock Frequency				800	kHz
Start Condition Hold Time (Prior to first clock pulse)	T_{HDST}	200			ns
Clock Low Time	T_{LOW}	400			ns
Clock High Time	T_{HIGH}	400			ns
Setup Time For Repeated Start Condition	T_{SUST}	200			ns
Data Hold Time	T_{HDD}	0			ns
Data Set-Up Time	T_{SUD}	100			ns
Rise Time of both SDA and SCL	T_R			300	ns
Falling Time of both SDA and SCL	T_F			300	ns
Setup Time for Stop Condition	T_{SUSP}	200			ns



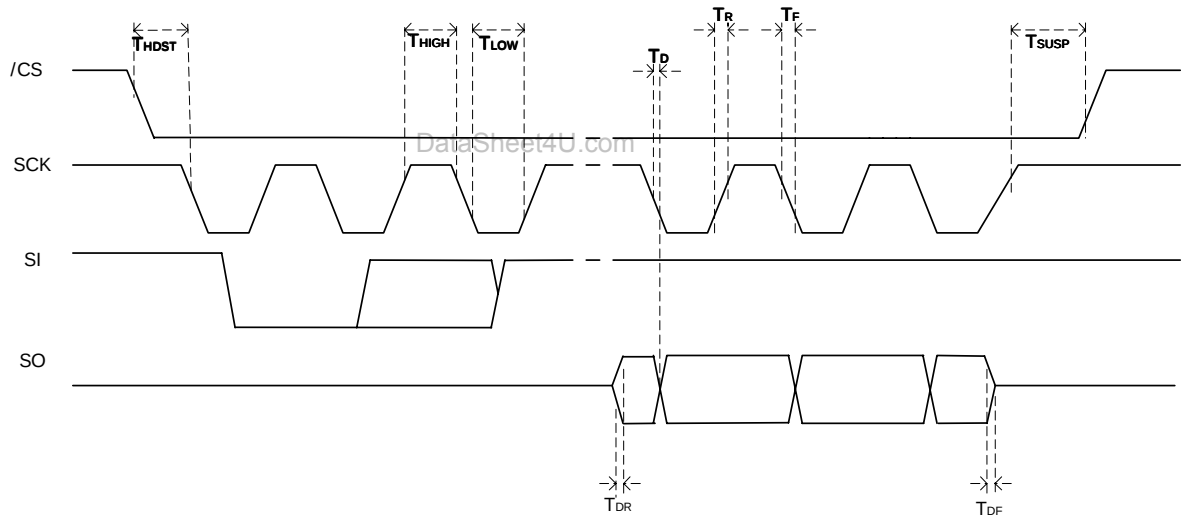
2. SPI Write Timing

Parameter	Symbol	Min	-	Max	Units
Start Condition Hold Time	T_{HDST}	200			ns
Clock High Time	T_{HIGH}	400			ns
Clock Low Time	T_{LOW}	400			ns
SI Setup Time to SCK	T_{SUD}	100			ns
Data Hold Time	T_{HDD}	0			ns
Falling Time of both SI and SCK	T_{DF}			300	ns
Rising Time of both SI and SCK	T_{DR}			300	ns
Setup Time for Stop Condition	T_{SUSP}	200			ns



3. SPI Read Timing

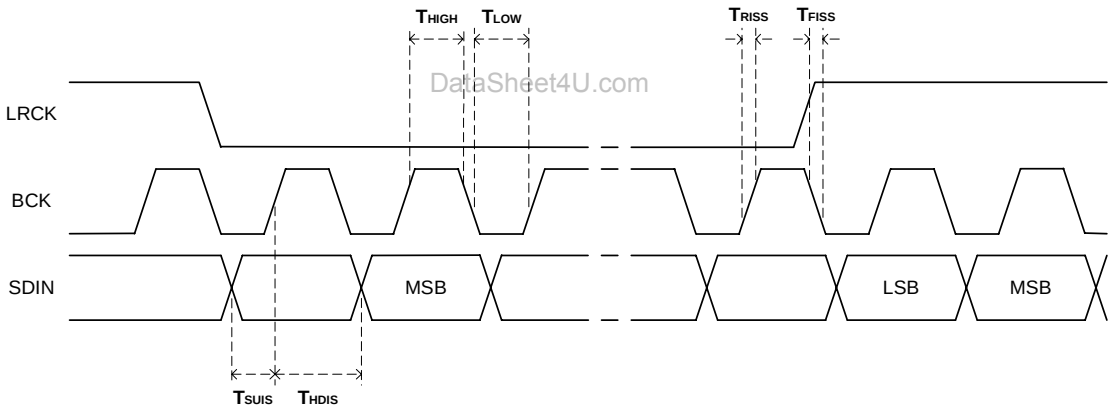
Parameter	Symbol	Min	-	Max	Units
Start Condition Hold Time	T_{HDST}	200			ns
Clock High Time	T_{HIGH}	400			ns
Clock Low Time	T_{LOW}	400			ns
SO Delay time for Valid Data	T_D	100			ns
Falling Time of both SO and SCK	T_{DF}			300	ns
Rising Time of both SO and SCK	T_{DR}			300	ns
Setup Time for Stop Condition	T_{SUSP}	200			ns



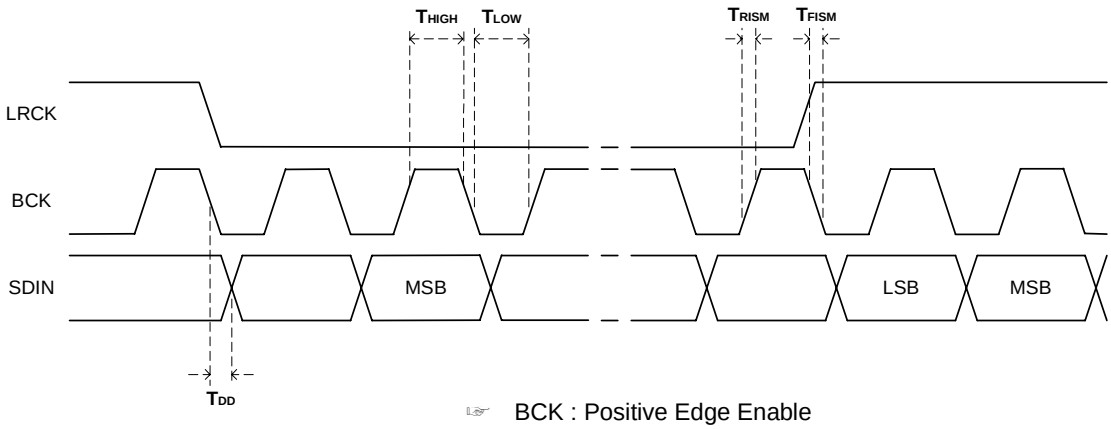
4. I²S Data Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Data Holding Time	T_{HDIS}	25			ns
Data Setup Time	T_{SUIS}	25			ns
Clock High Time	T_{HIGH}	80	180		ns
Clock Low Time	T_{LOW}	80	180		ns
Rising Time of BCK (Slave Mode)	T_{RISS}			20	ns
Falling Time of BCK (Slave Mode)	T_{FISS}			20	ns
Rising Time of BCK (Master Mode)	T_{RISM}		3	5	ns
Falling Time of BCK (Master Mode)	T_{FISM}		3	5	ns
Delay until valid Data	T_{DD}	20		40	ns

Slave Mode



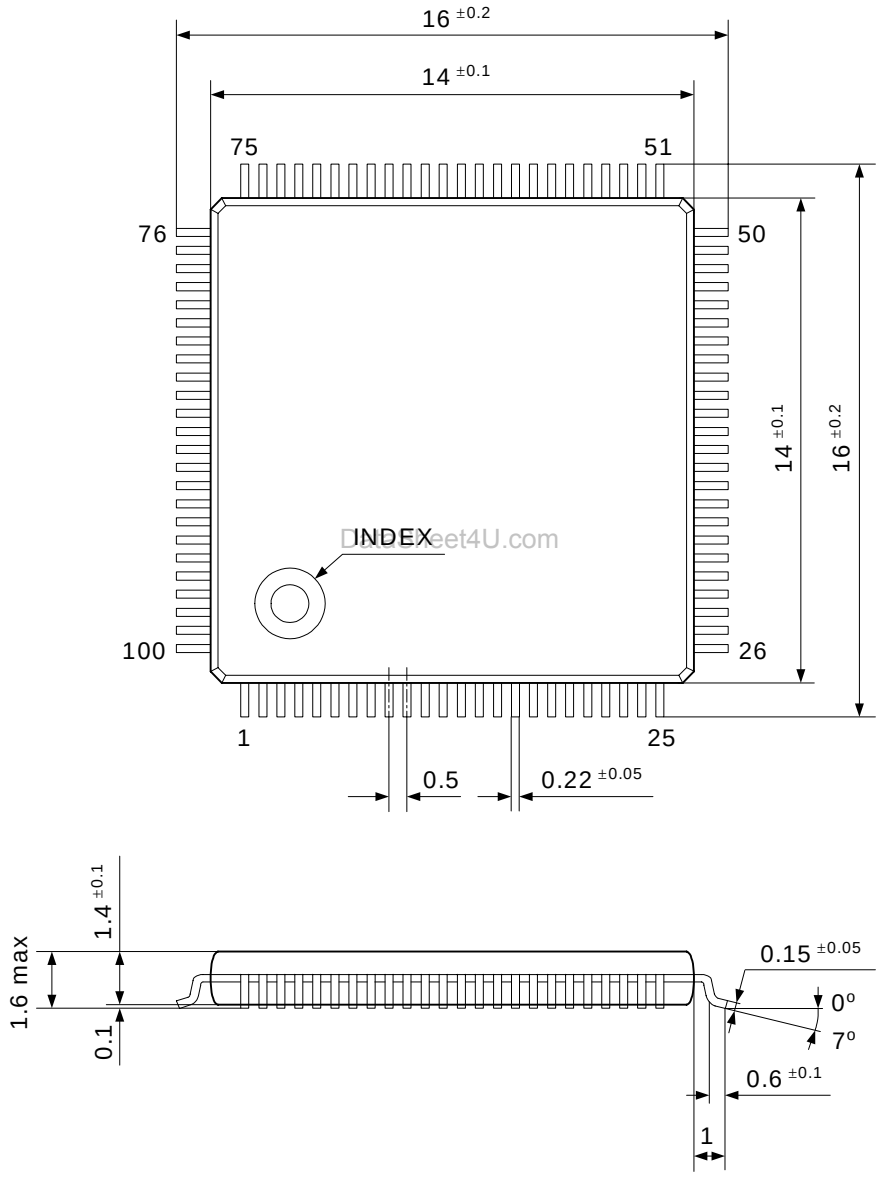
Master Mode



☞ BCK : Positive Edge Enable

Package Dimensions

Unit : mm



Appendix A
Gain-Register Value Tables

Table A-1. Master Volume Gain Values

Gain (dB)	Register Value	Gain (dB)	Register Value	Gain (dB)	Register Value	Gain (dB)	Register Value
18.0	0x0C	-4.5	0x39	-27.0	0x66	-49.5	0x93
17.5	0x0D	-5.0	0x3A	-27.5	0x67	-50.0	0x94
17.0	0x0E	-5.5	0x3B	-28.0	0x68	-50.5	0x95
16.5	0x0F	-6.0	0x3C	-28.5	0x69	-51.0	0x96
16.0	0x10	-6.5	0x3D	-29.0	0x6A	-51.5	0x97
15.5	0x11	-7.0	0x3E	-29.5	0x6B	-52.0	0x98
15.0	0x12	-7.5	0x3F	-30.0	0x6C	-52.5	0x99
14.5	0x13	-8.0	0x40	-30.5	0x6D	-53.0	0x9A
14.0	0x14	-8.5	0x41	-31.0	0x6E	-53.5	0x9B
13.5	0x15	-9.0	0x42	-31.5	0x6F	-54.0	0x9C
13.0	0x16	-9.5	0x43	-32.0	0x70	-54.5	0x9D
12.5	0x17	-10.0	0x44	-32.5	0x71	-55.0	0x9E
12.0	0x18	-10.5	0x45	-33.0	0x72	-55.5	0x9F
11.5	0x19	-11.0	0x46	-33.5	0x73	-56.0	0xA0
11.0	0x1A	-11.5	0x47	-34.0	0x74	-56.5	0xA1
10.5	0x1B	-12.0	0x48	-34.5	0x75	-57.0	0xA2
10.0	0x1C	-12.5	0x49	-35.0	0x76	-57.5	0xA3
9.5	0x1D	-13.0	0x4A	-35.5	0x77	-58.0	0xA4
9.0	0x1E	-13.5	0x4B	-36.0	0x78	-58.5	0xA5
8.5	0x1F	-14.0	0x4C	-36.5	0x79	-59.0	0xA6
8.0	0x20	-14.5	0x4D	-37.0	0x7A	-59.5	0xA7
7.5	0x21	-15.0	0x4E	-37.5	0x7B	-60.0	0xA8
7.0	0x22	-15.5	0x4F	-38.0	0x7C	-60.5	0xA9
6.5	0x23	-16.0	0x50	-38.5	0x7D	-61.0	0xAA
6.0	0x24	-16.5	0x51	-39.0	0x7E	-61.5	0xAB
5.5	0x25	-17.0	0x52	-39.5	0x7F	-62.0	0xAC
5.0	0x26	-17.5	0x53	-40.0	0x80	-62.5	0xAD
4.5	0x27	-18.0	0x54	-40.5	0x81	-63.0	0xAE
4.0	0x28	-18.5	0x55	-41.0	0x82	-63.5	0xAF
3.5	0x29	-19.0	0x56	-41.5	0x83	-64.0	0xB0
3.0	0x2A	-19.5	0x57	-42.0	0x84	-64.5	0xB1
2.5	0x2B	-20.0	0x58	-42.5	0x85	-65.0	0xB2
2.0	0x2C	-20.5	0x59	-43.0	0x86	-65.5	0xB3
1.5	0x2D	-21.0	0x5A	-43.5	0x87	-66.0	0xB4
1.0	0x2E	-21.5	0x5B	-44.0	0x88	-66.5	0xB5
0.5	0x2F	-22.0	0x5C	-44.5	0x89	-67.0	0xB6
0.0	0x30	-22.5	0x5D	-45.0	0x8A	-67.5	0xB7
-0.5	0x31	-23.0	0x5E	-45.5	0x8B	-68.0	0xB8
-1.0	0x32	-23.5	0x5F	-46.0	0x8C	-68.5	0xB9
-1.5	0x33	-24.0	0x60	-46.5	0x8D	-69.0	0xBA
-2.0	0x34	-24.5	0x61	-47.0	0x8E	-69.5	0xBB
-2.5	0x35	-25.0	0x62	-47.5	0x8F	-70.0	0xBC
-3.0	0x36	-25.5	0x63	-48.0	0x90	|	|
-3.5	0x37	-26.0	0x64	-48.5	0x91	|	|
-4.0	0x38	-26.5	0x65	-49.0	0x92	-70.0	0xFF

Table A-2. Trim Gain Values

Gain (dB)	Register Value	Gain (dB)	Register Value
+12.0	0x18	-0.5	0x3F
+11.5	0x17	-1.0	0x3E
+11.0	0x16	-1.5	0x3D
+10.5	0x15	-2.0	0x3C
+10.0	0x14	-2.5	0x3B
+9.5	0x13	-3.0	0x3A
+9.0	0x12	-3.5	0x39
+8.5	0x11	-4.0	0x38
+8.0	0x10	-4.5	0x37
+7.5	0x0F	-5.0	0x36
+7.0	0x0E	-5.5	0x35
+6.5	0x0D	-6.0	0x34
+6.0	0x0C	-6.5	0x33
+5.5	0x0B	-7.0	0x32
+5.0	0x0A	-7.5	0x31
+4.5	0x09	-8.0	0x30
+4.0	0x08	-8.5	0x2F
+3.5	0x07	-9.0	0x2E
+3.0	0x06	-9.5	0x2D
+2.5	0x05	-10.0	0x2C
+2.0	0x04	-10.5	0x2B
+1.5	0x03	-11.0	0x2A
+1.0	0x02	-11.5	0x29
+0.5	0x01	-12.0	0x28
0.0	0x00		

Table A-3. Mixer Gain Values

Signal Polarity	Gain (dB)	Register Value	Signal Polarity	Gain (dB)	Register Value	Signal Polarity	Gain (dB)	Register Value
+	18.0	0x00	+	-2.5	0x29	+	-23.0	0x52
+	17.5	0x01	+	-3.0	0x2A	+	-23.5	0x53
+	17.0	0x02	+	-3.5	0x2B	+	-24.0	0x54
+	16.5	0x03	+	-4.0	0x2C	+	-24.5	0x55
+	16.0	0x04	+	-4.5	0x2D	+	-25.0	0x56
+	15.5	0x05	+	-5.0	0x2E	+	-25.5	0x57
+	15.0	0x06	+	-5.5	0x2F	+	-26.0	0x58
+	14.5	0x07	+	-6.0	0x30	+	-26.5	0x59
+	14.0	0x08	+	-6.5	0x31	+	-27.0	0x5A
+	13.5	0x09	+	-7.0	0x32	+	-27.5	0x5B
+	13.0	0x0A	+	-7.5	0x33	+	-28.0	0x5C
+	12.5	0x0B	+	-8.0	0x34	+	-28.5	0x5D
+	12.0	0x0C	+	-8.5	0x35	+	-29.0	0x5E
+	11.5	0x0D	+	-9.0	0x36	+	-29.5	0x5F
+	11.0	0x0E	+	-9.5	0x37	+	-30.0	0x60
+	10.5	0x0F	+	-10.0	0x38	+	-30.5	0x61
+	10.0	0x10	+	-10.5	0x39	+	-31.0	0x62
+	9.5	0x11	+	-11.0	0x3A	+	-31.5	0x63
+	9.0	0x12	+	-11.5	0x3B	+	-32.0	0x64
+	8.5	0x13	+	-12.0	0x3C	+	-32.5	0x65
+	8.0	0x14	+	-12.5	0x3D	+	-33.0	0x66
+	7.5	0x15	+	-13.0	0x3E	+	-33.5	0x67
+	7.0	0x16	+	-13.5	0x3F	+	-34.0	0x68
+	6.5	0x17	+	-14.0	0x40	+	-34.5	0x69
+	6.0	0x18	+	-14.5	0x41	+	-35.0	0x6A
+	5.5	0x19	+	-15.0	0x42	+	-35.5	0x6B
+	5.0	0x1A	+	-15.5	0x43	+	-36.0	0x6C
+	4.5	0x1B	+	-16.0	0x44	+	-36.5	0x6D
+	4.0	0x1C	+	-16.5	0x45	+	-37.0	0x6E
+	3.5	0x1D	+	-17.0	0x46	+	-37.5	0x6F
+	3.0	0x1E	+	-17.5	0x47	+	-38.0	0x70
+	2.5	0x1F	+	-18.0	0x48	+	-38.5	0x71
+	2.0	0x20	+	-18.5	0x49	+	-39.0	0x72
+	1.5	0x21	+	-19.0	0x4A	+	-39.5	0x73
+	1.0	0x22	+	-19.5	0x4B	+	-40.0	0x74
+	0.5	0x23	+	-20.0	0x4C	+	-40.5	0x75
+	0.0	0x24	+	-20.5	0x4D	+	-41.0	0x76
+	-0.5	0x25	+	-21.0	0x4E	+	-41.5	0x77
+	-1.0	0x26	+	-21.5	0x4F	+	-42.0	0x78
+	-1.5	0x27	+	-22.0	0x50		Mute	0x79
+	-2.0	0x28	+	-22.5	0x51		Mute	0x7F

Table A-3. Mixer Gain Values (Continued)

Signal Polarity	Gain (dB)	Register Value
-	18.0	0x80
-	17.5	0x81
-	17.0	0x82
-	16.5	0x83
-	16.0	0x84
-	15.5	0x85
-	15.0	0x86
-	14.5	0x87
-	14.0	0x88
-	13.5	0x89
-	13.0	0x8A
-	12.5	0x8B
-	12.0	0x8C
-	11.5	0x8D
-	11.0	0x8E
-	10.5	0x8F
-	10.0	0x90
-	9.5	0x91
-	9.0	0x92
-	8.5	0x93
-	8.0	0x94
-	7.5	0x95
-	7.0	0x96
-	6.5	0x97
-	6.0	0x98
-	5.5	0x99
-	5.0	0x9A
-	4.5	0x9B
-	4.0	0x9C
-	3.5	0x9D
-	3.0	0x9E
-	2.5	0x9F
-	2.0	0xA0
-	1.5	0XA1
-	1.0	0XA2
-	0.5	0XA3
-	0.0	0XA4
-	-0.5	0xA5
-	-1.0	0xA6
-	-1.5	0xA7
-	-2.0	0xA8
-	-2.5	0xA9
-	-3.0	0xAA
-	-3.5	0xAB
-	-4.0	0xAC
-	-4.5	0xAD
-	-5.0	0xAE
-	-5.5	0xAF
-	-6.0	0xB0
-	-6.5	0xB1
-	-7.0	0xB2
-	-7.5	0xB3
-	-8.0	0xB4
-	-8.5	0xB5
-	-9.0	0xB6
-	-9.5	0xB7
-	-10.0	0xB8
-	-10.5	0xB9
-	-11.0	0xBA
-	-11.5	0xBB
-	-12.0	0xBC
-	-12.5	0xBD
-	-13.0	0xBE
-	-13.5	0xBF
-	-14.0	0xC0
-	-14.5	0xC1
-	-15.0	0xC2
-	-15.5	0xC3
-	-16.0	0xC4
-	-16.5	0xC5
-	-17.0	0xC6
-	-17.5	0xC7
-	-18.0	0xC8
-	-18.5	0xC9
-	-19.0	0xCA
-	-19.5	0xCB
-	-20.0	0xCC
-	-20.5	0xCD
-	-21.0	0xCE
-	-21.5	0xCF
-	-22.0	0xD0
-	-22.5	0xD1
-	-23.0	0xD2
-	-23.5	0xD3
-	-24.0	0xD4
-	-24.5	0xD5
-	-25.0	0xD6
-	-25.5	0xD7
-	-26.0	0xD8
-	-26.5	0xD9
-	-27.0	0xDA
-	-27.5	0xDB
-	-28.0	0xDC
-	-28.5	0xDD
-	-29.0	0xDE
-	-29.5	0xDF
-	-30.0	0xE0
-	-30.5	0xE1
-	-31.0	0xE2
-	-31.5	0xE3
-	-32.0	0xE4
-	-32.5	0xE5
-	-33.0	0xE6
-	-33.5	0xE7
-	-34.0	0xE8
-	-34.5	0xE9
-	-35.0	0xEA
-	-35.5	0xEB
-	-36.0	0xEC
-	-36.5	0xED
-	-37.0	0xEE
-	-37.5	0xEF
-	-38.0	0xF0
-	-38.5	0xF1
-	-39.0	0xF2
-	-39.5	0xF3
-	-40.0	0xF4
-	-40.5	0xF5
-	-41.0	0xF6
-	-41.5	0xF7
-	-42.0	0xF8
	Mute	0xF9
	Mute	0xFF

Table A-4. EQ Gain Values

Gain (dB)	Register Value	Gain (dB)	Register Value
+12.0	0x0C	-1.0	0x1F
+11.0	0x0B	-2.0	0x1E
+10.0	0x0A	-3.0	0x1D
+9.0	0x09	-4.0	0x1C
+8.0	0x08	-5.0	0x1B
+7.0	0x07	-6.0	0x1A
+6.0	0x06	-7.0	0x19
+5.0	0x05	-8.0	0x18
+4.0	0x04	-9.0	0x17
+3.0	0x03	-10.0	0x16
+2.0	0x02	-11.0	0x15
+1.0	0x01	-12.0	0x14
0.0	0x00		