SIEMENS

Dual-Tone Multi-Frequency Generator (DTMF)

PSB 8593

CMOS IC

Type	Ordering Code	Package
PSB 8593	Q67100-H8168	P-DIP-20

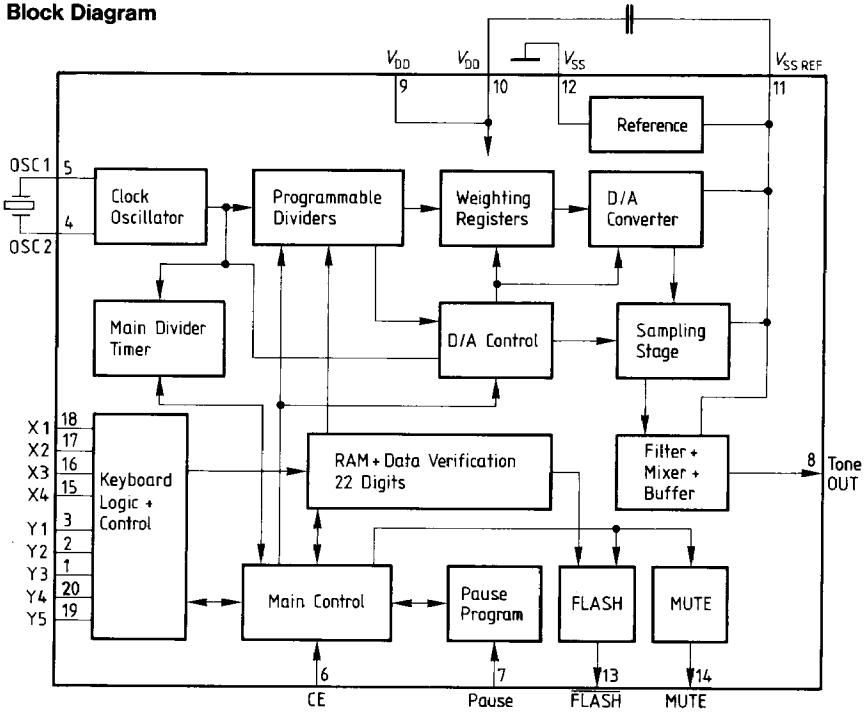
The DTMF generator PSB 8593 is specially designed to implement a dual-tone telephone dialing system. The device can be connected directly to a standard pushbutton keyboard (single-contact, type X-Y matrix code) and is operated together with an integrated speech circuit. All necessary dual-tone frequencies are derived from the commonly used standard TV crystal (3.58 MHz) which features a very high degree of accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. The speech circuit regulates the signal levels of the dual tones to meet the recommended specifications for telephone sets. The buffer amplifier therefore is located on the speech circuit.

Applications of the device include radio and mobile telephones, remote control and process control.

Features

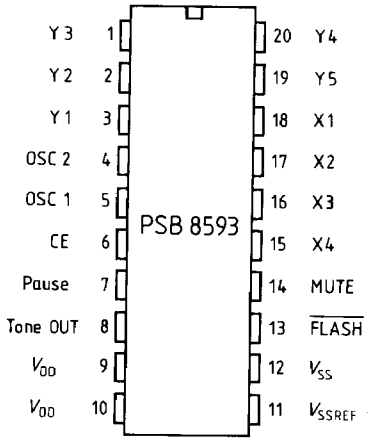
- Advanced CMOS technology
- Last-number redial (up to 22 digits)
- Flash generation (register call)
- CEPT-compatible without external filtering
- Standard low-cost TV crystal (3.58 MHz)
- High frequency accuracy (better than 0.4%)
- Operation with single-contact matrix keyboard, 20 keys
- Multi-key lockout and debouncing
- Binary data input
- Dual-tone and single-tone output
- Defined audio output time and interdigital pause
- Programmable access pause
- Low operating and standby current
- MUTE output
- Chip enable input (CE)
- Internal power-on reset
- Internal reference:
  DTMF level independent of supply voltage

Block Diagram



Pin Configuration

(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function
1	Y3	Keyboard interface
2	Y2	
3	Y1	
4	OSC 2	Connection for crystal 3.5795 MHz
5	OSC 1	
6	CE	Hook switch – chip enable
7	Pause	Programmable pin for pause
8	Tone OUT	Output for dual tone multi-frequencies
9	V_{DD}	Positive supply voltage
10	V_{DD}	(internally connected)
11	$V_{SS\ REF}$	Reference voltage
12	V_{SS}	Ground
13	$\overline{\text{FLASH}}$	$\overline{\text{FLASH}}$ output
14	MUTE	MUTE output
15	X4	Keyboard interface
16	X3	
17	X2	
18	X1	
19	Y5	
20	Y4	

Functional Description

Internal Logic Description

After recognizing a key closure, oscillator operation is started. When the oscillation is high enough to activate the first flipflop, the oscillator current is reduced and the entire logic is reset. The chip command first starts the logic comparator to suppress the switch bouncing. When the protection time has lapsed, the valid code is stored in the RAM. The RAM is reset if the valid code is a new dialed number. Then, the code is read out of the RAM, and it programs the two dividers of the sinewave synthesizer. This is done continuously as long as the sending timer is active (80 ms), or until the key is released. In the meantime, further digits can be stored in the RAM. When the sending timer has stopped operation or the key contact is opened, a command will activate the pause timer (80 ms); the same counter is used in both cases. At this point, the command reads out the next digit from the RAM location. The command also sets the MUTE output high when programming the dividers and low after completing the function. The MUTE output will remain low until new sinewaves are generated. If the recognized key closure is a redial function, a command will start to read out the stored number from RAM location. If the recognized key closure is a single-tone mode, the command will just program the appropriate divider during key depression. The MUTE output has the same function as in dual-tone mode without timing.

Tone Generation

When a valid key closure is recognized or a digit is still in the RAM that is marked for access, the command programs the high and low group dividers with appropriate divider ratios. This means, the outputs of these dividers cycle at 26 times the desired high-group and low-group frequencies, respectively, for a minimum of 80 ms. The outputs of the programmable dividers drive two 6-stage up/down counters with connected sign bit. Every time, an up and down counting process has been completed, the sign bit is changed. In this way 26 equal time segments are generated within each output cycle. The 26 segments are used to digitally snythesize a stair-step waveform in order to approximate the sinewave function **(see figure)** in one D/A converter for the high and low-group frequency. Synthesizing the two sinewave functions in one D/A converter requires the converter's working below 600 ns, as it is to be multiplexed between the two functions. This is done by connecting a sinewave-adjusted capacitor network between the two outputs of the converter via a sign bit circuit that is applied to $V_{REF} = V_{DD}$ or V_{SS} and virtual ground. The peak-to-peak amplitude of the stair-step function is adjusted by a connected sample and hold capacitor having a different value for the high and low frequency group, respectively. The sample and hold capacitor is followed by two low-pass filters, one for the high and one for the low-frequency group. The individual tones generated with different amplitudes and filtered separately are added linearly and drive an output buffer.

Single-Tone Mode

A low-group tone can be generated by activating the appropriate row inputs connected to ground. A high-group tone can be generated by activating the appropriate column inputs with V_{DD}. In this mode no digit-frequency combination will be activated and no digit will be stored in the RAM.

The generation time depends on the duration of the input function. A stored phone number remains in the RAM.

Clock Generation

The device contains an oscillator circuit with the necessary parasitic capacitances on-chip, so it its only required to connect the standard 3.58-MHz TV crystal across the OSC1 and OSC2 terminals in order to implement the oscillator function.

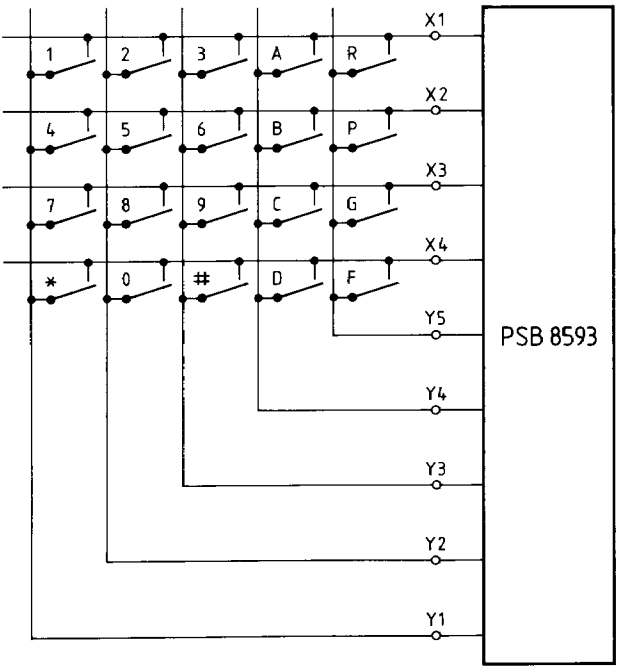
Whenever a row or column input is activated the oscillator is operating until all timing functions are terminated.

Keyboard Interface

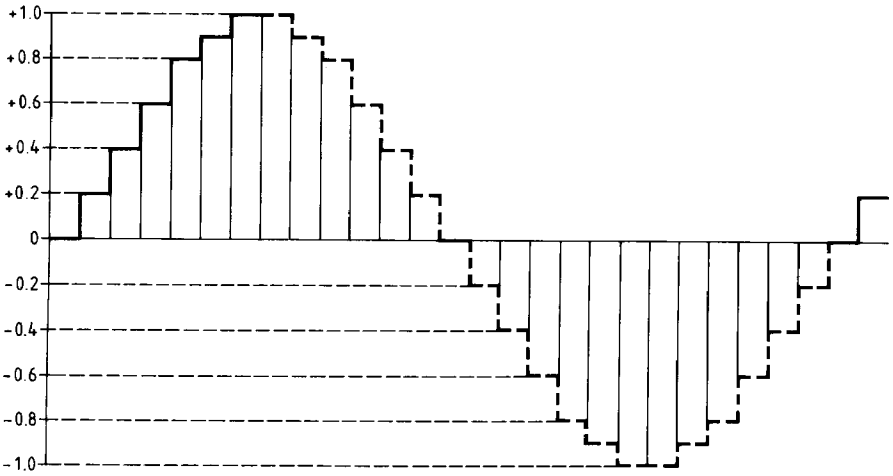
The device can be connected directly to a X-Y matrix keyboard and requires no protection against multi-key function. An internal logic prevents the transmission of illegal tones when more than one key is pressed. Single tones can be obtained by connecting a column input to V_{DD} or grounding a row input. After key recognition the inputs are static, i.e. there is no noise generation as it is the case with scanned or dynamic inputs.

An interrupt of longer than 4 ms on the key inputs releases the key function in the recognition circuit. After this the next digit is detected.

Connection to Keyboard



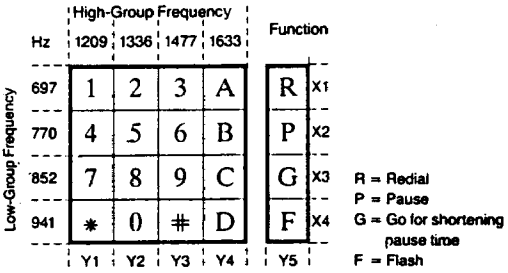
Synthesized Output Waveforms



Active Input	Output Frequency (Hz) Specified	Actual	(%) without Crystal Drift
X1	697	695.32731	−0.241
X2	770	773.4539	+0.448
X3	852	849.84449	−0.254
X4	941	942.97813	+0.210
Y1	1209	1207.67375	−0.110
Y2	1336	1336.64862	+0.049
Y3	1477	1480.37428	+0.228
Y4	1633	1638.98581	+0.365

Special Functions

Keyboard Configuration (with maximum number of keys)



The order of the 4 additional keys R, P, G, F is mask-programmable.

Redial Function

If the redial button is pressed after the handset has been picked up, all numbers stored in the RAM including pause and flash function will be sent out.

After termination and during redial function it is possible to dial also further digits which will be sent out after the redial function is finished.

Before starting the redial function a supervisory equipment checks the usefulness of the RAM contents.

Programming of Pause

If the telephone system needs pauses e.g. for trunk searching or dial-tone connection, the pauses must be stored in the RAM. To store such pauses, only depress the pause-button; afterwards further digits can be dialed. The number of pauses is unlimited. The timing of the pause is programmable via the pause-programming pin.

There are 3 choices:

Programming pin	connected to V_{DD}:	3 s
	connected to ground (V_{SS}):	5 s
	open:	unlimited pause.

Go Function

The go button terminates the unlimited pause. Furthermore, it is possible to terminate also pause functions with fixed timing. With a transistor connected in parallel to the go button switch the pause can be terminated by operating the transistor via a dial-tone recognition circuit.

Flash Function

The flash function is stored also in the RAM. The number of flashes is unlimited. The flash output goes to V_{SS} for 90 ms; once the flash function is completed the DTMF signaling will continue after a pause of 900 ms.

Binary Data Input

The CE-Input must be at high level (chip enabled).

Binary data is written into memory, when the lines X1 and X4 (low level active) are connected to V_{SS} for a minimum of 7 ms. The data must be present at the same time synchronously to X1 and X4 at the data lines Y1 to Y5. The lines X2 and X3 remain unloaded (open).

The device is sending the DTMF tones according to the data written into memory as long as the accompanying X1 and X4 are at low level, at least for 80 ms.

Between two data inputs, there must be a pause of minimum 10 ms with X1 and X4 at V_{DD} (high level) and Y1 to Y5 at V_{SS} (low level).

The level at the data lines Y1 to Y5 should not exceed the actual supply voltage V_{DD}, in certain circumstances it is necessary to connect open collector gates or transistors.

The binary codes are given in the following table ("0" = V_{SS}, "1" = V_{DD}):

Digit (Key)	Binary Input Code					DTMF Output Frequencies
	Y5	Y4	Y3	Y2	Y1	
1	0	0	0	0	0	697 Hz / 1209 Hz
4	0	0	0	0	1	770 Hz / 1209 Hz
7	0	0	0	1	0	852 Hz / 1209 Hz
*	0	0	0	1	1	941 Hz / 1209 Hz
2	0	0	1	0	0	697 Hz / 1336 Hz
5	0	0	1	0	1	770 Hz / 1336 Hz
8	0	0	1	1	0	852 Hz / 1336 Hz
0	0	0	1	1	1	941 Hz / 1336 Hz
3	0	1	0	0	0	697 Hz / 1477 Hz
6	0	1	0	0	1	770 Hz / 1477 Hz
9	0	1	0	1	0	852 Hz / 1477 Hz
#	0	1	0	1	1	941 Hz / 1477 Hz
A	0	1	1	0	0	697 Hz / 1633 Hz
B	0	1	1	0	1	770 Hz / 1633 Hz
C	0	1	1	1	0	852 Hz / 1633 Hz
D	0	1	1	1	1	941 Hz / 1633 Hz
R	1	0	0	0	0	–
P	1	0	0	0	1	–
G	1	0	0	1	0	–
F	1	0	0	1	1	–

Hook Switch/Power Down

The device is in power down mode when the hook switch input is low. In this mode, the pullup resistors are disconnected at the 4 row inputs and all inputs are passive. In this case, the maximum ratings apply to the inputs. If the hook switch input is high = V_{DD}, the row and column inputs will be activated and the device can be started via the inputs.

Option: Various branch exchanges show interrupts in the line-power supply during trunk searching. Therefore, it is difficult to detect the right onhook-switch function; we recommend to use our line-power fault detection featuring the following: After every interrupt of line power supply, the device starts a "wait cycle" of 240 ms, during this time power is supplied by the buffer capacitor (only DTMF and PAUSE function). If the line power supply is restored in the meantime, the device will ignore the interrupt; after 240 ms, the device will accept the interrupt as an exchange release and the stored digits are prepared for redial. During interrupt, the device accepts dialing but can not send DTMF.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DC supply voltage	$V_{DD}-V_{SS}$	−0.3	7	V
Input voltage at any pin	V_I	−0.3	V_{DD} +0.3	V
Power dissipation at 25 °C	P		10	mW
Operating temperature	T_A	−25	70	°C
Storage temperature	T_{stg}	−55	125	°C

DC Characteristics

$T_A = -25\,°C$ to $70\,°C$, $V_{DD} = 3.5$ V; unless otherwise noted

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
Supply voltage = reference voltage	V_{DD}	3.0	3.5	6.0	V	
Operating current	I_{DD}	1	1.5	2.0	mA	one key selected tone and MUTE output unloaded $V_{DD} = 3.5$ V
Standby current	I_{DD}		1	2	µA	no key selected output unloaded $V_{DD} = 3.5$ V
Standby voltage	V_{DD}	1.2		6	V	for data retention
MUTE output	I_{OH} I_{OH} I_{OL}	0.5 1	1 2	2 2 3	mA mA mA	$V_{DD} = 3.5$ V $V_{OH} = 3$ V $V_{OL} = 0.4$ V
Flash output	I_{OL}	1	2	3	mA	Open drain
Inputs						
Chip enable CE	V_{IH} V_{IL}	3		3.5 0.5	V V	
Input leakage current	$+I_{IH}$ $-I_{IL}$			50 50	nA nA	CE = H CE = L
Pause programming pin high level low level	 V_{IH} V_{IL}	 3		 3.5 0.5	 V V	 during scanning, load capacitance $C_L = 50$ pF
Open input		600			kΩ	
Matrix keyboard operation Keyboard current	I_{Key}	100	150	200	µA	X connected of Y CE = H
Keyboard						
ON resistance	$R_{Key\ ON}$			1	kΩ	contact ON
OFF resistance	$R_{Key\ OFF}$	100			kΩ	contact OFF
Input current for X_n ON Y_n ON	 $-I_{IL}$ $+I_{IH}$	 100 200	 150 300	 300 400	 µA µA	 $V_I = 0 \ldots 1$ V $V_I = 2.5 \ldots 3.5$ V
Frequency output						
Output DC level		1.8	2.0	2.2	V	CE = H
Small-signal output impedance	Z_O	0.5	1.5	3	kΩ	

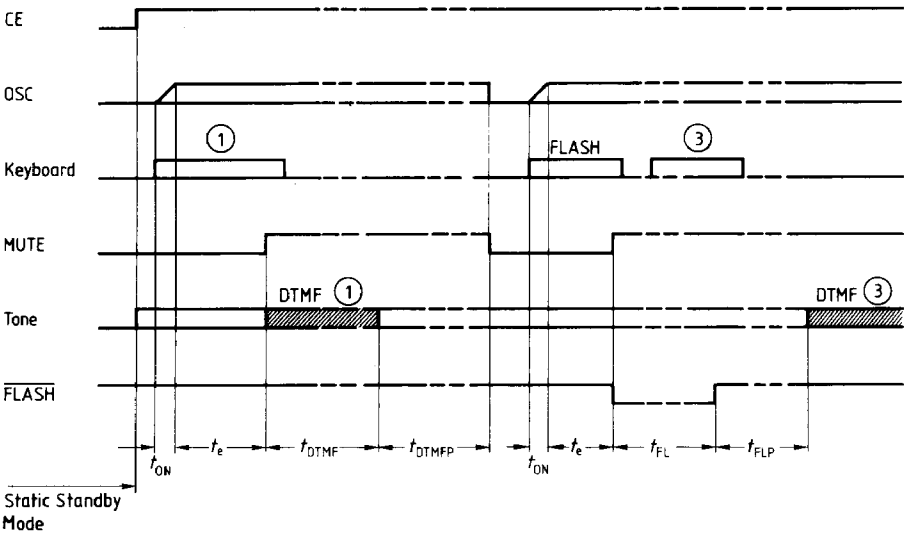
AC Characteristics

$T_A = -25\,°C$ to $70\,°C$, $V_{DD} = 3.5$ V; unless otherwise noted

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Minimum load, AC-coupled (For specified distortion according to CEPT)	R_L	15			kΩ
Frequency Output					
Sum level	P_S		426		mV_{rms}
Low group	P_L	236	265	297	mV_{rms}
High group	P_H	297	333	373	mV_{rms}
Preemphasis	P_D	1	2	3	dB
Frequency deviation	Δf	−0.254		0.448	%
Timing specifications					
Debounce time	t_d	4.5			ms
Setup time (key pressed to frequency OUT) (Min. debounce + oscillator start-up time)	t_s	5.5	6.0	6.5	ms
Binary Input					
Data valid	t	7			ms
Data change	t	10			ms

Timing Diagrams

Figure 1

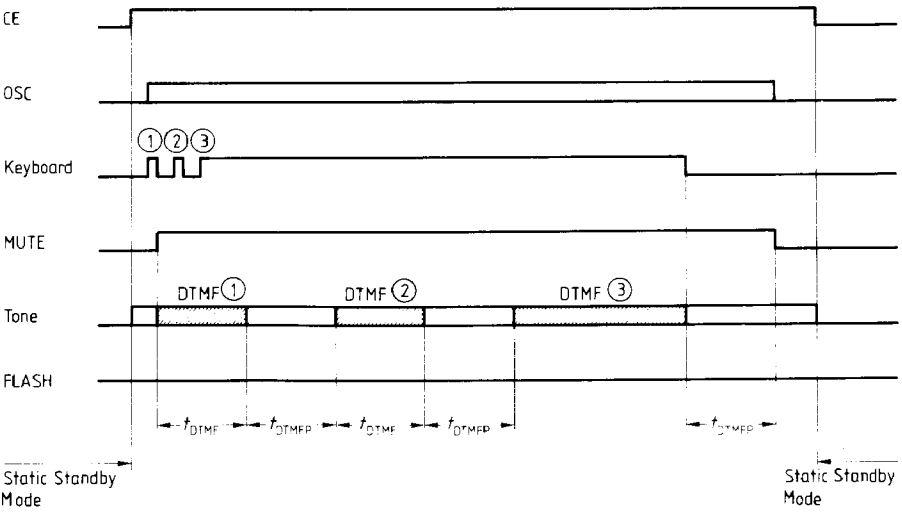


Oscillator start-up upon key depression (t_{on}), key recognition time (t_e), DTMF (t_{DTMF}, t_{DTMFP}), and FLASH (t_{FL}, t_{FLP})

Timing specs:

	typ.	max.	Unit
t_{on}		2	ms
t_e	4.7		ms
t_{DTMF}	80		ms
t_{DTMFP}	80		ms
t_{FL}	90		ms
t_{FLP}	870		ms

Figure 2



Signals at fast as well as slow data entry (sending time extension)

Figure 3

Key Closure Recognition with X-Y Keyboard

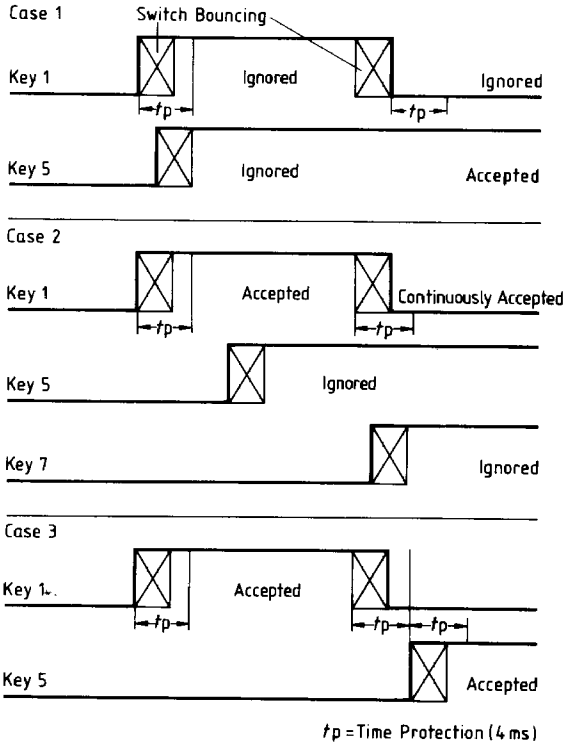


Figure 4

Simplified Circuit Example
Telephone Set with PSB 8593

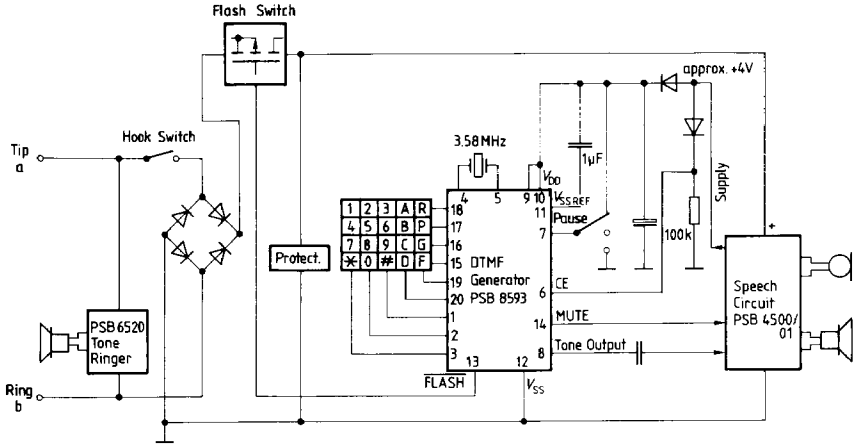


Figure 5

Auxiliary Test Circuit