USB-Compliant Single-Cell Li-Ion Switching Charger with USB-OTG Boost Regulator

Description

The PSC5425 combines a highly integrated switch-mode charger, to minimize single-cell Lithium-ion (Li-ion) charging time from a USB power source, and a boost regulator to power a USB peripheral from the battery.

The charging parameters and operating modes are programmable through an I^2C interface that operates up to 400kbps. The charger circuits switch at 1.5MHz to minimize the size of external passive components.

The PSC5425 provides battery charging in three phases: conditioning, constant current, and constant voltage.

To ensure USB compliance and minimize charging time, the input current is limited to the value set through the I^2C host.

The integrated circuit (IC) automatically restarts the charge cycle when the battery falls below an internal threshold. If the input source is removed, the IC enters a high-impedance mode with leakage from the battery to the input prevented. Charge status is reported back to the host through the I^2C port.

The PSC5425 can operate as a boost regulator on command from the system. The boost regulator includes a soft-start that limits inrush current from the battery.

The PSC5425 is available in a 2.04 x 2.0mm, 20-bump, 0.4mm pitch WLCSP package.

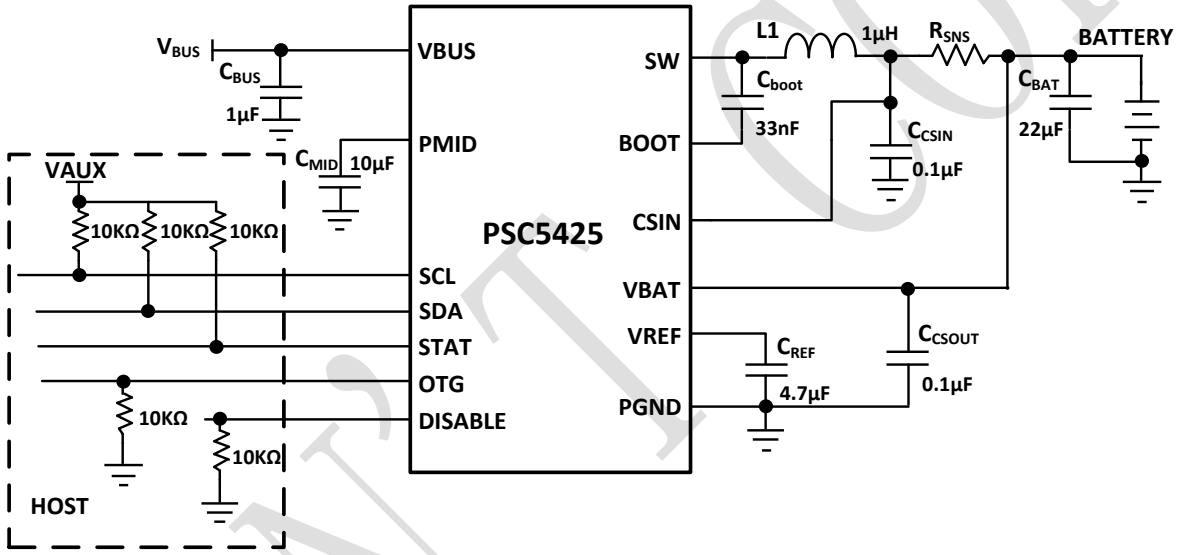


Figure 1: Typical Application

Feature

- Fully Integrated, High-Efficiency Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
- Faster Charging than Linear
- Charge Voltage Accuracy: ±0.5% 25℃
- ±5% Charge Current Regulation Accuracy
- 20V Absolute Maximum Input Voltage
- 13.5V Maximum Input Operating Voltage
- 2.5A Maximum Charge Rate

Application

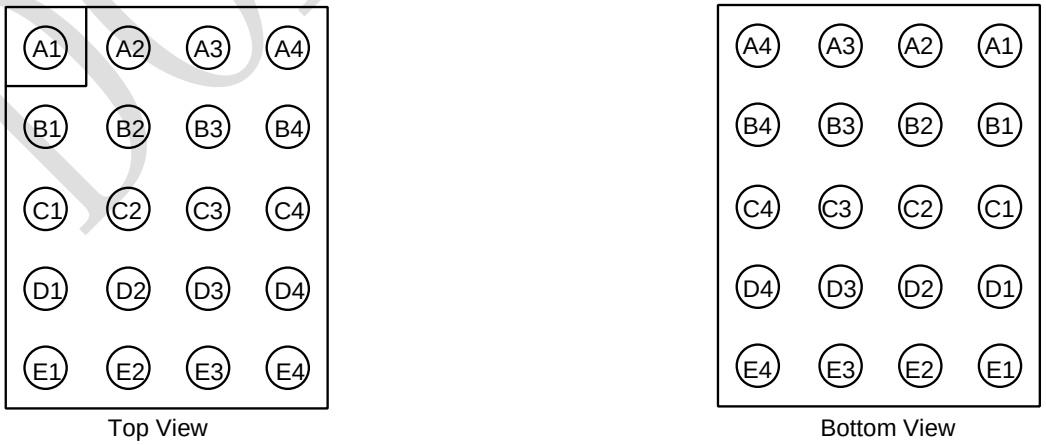
- Cellular Phones, Smart Phones, PDAs
- Tablet, Portable Media Players
- Gaming Device, Digital Cameras

- Programmable through I^2C Interface:
  -Input Current
  -Fast-Charge/Termination Current
  -Charger Voltage
  -Termination Enable
- 1.5MHz Synchronous Buck PWM Controller with Wide Duty Cycle Range
- Small Footprint 1uH/2.2uH External Inductor
- Weak Input Sources Accommodated by Reducing Charging Current to Maintain Minimum VBUS Voltage
- Low Reverse Leakage to Prevent Battery Drain to VBUS
- 5V, 1A Boost Mode for USB OTG for 3.0 to 4.5V Battery Input

Recommended External Components

Component	Description	Vendor	Parameter	Typ.	Units
L1 (Ich<=2.5A)	1.0uH, 30%, 2.6A 2.5mm*2.5mm*1.1mm	Murata:LQH2HPN1R0NJR	L	1.0	μH
			DCR(Series R)	57	mΩ
C_{BAT}	22μF,10%,6.3V,X5R,0603	Murata: GRM188R60J226M	C	22	μF
C_{MID}	10μF,5%,25V,X7R,0603	Murata: GRM1881X1E103	C	10	μF
C_{BUS}	1.0μF,10%,25V,X5R,0603	Murata: GRM188R61E105M	C	1.0	μF
D1	SchottkyBarrierDiode	PRISEMI：PSBD3D30V1H	DIODE	-	-

Pin Configuration



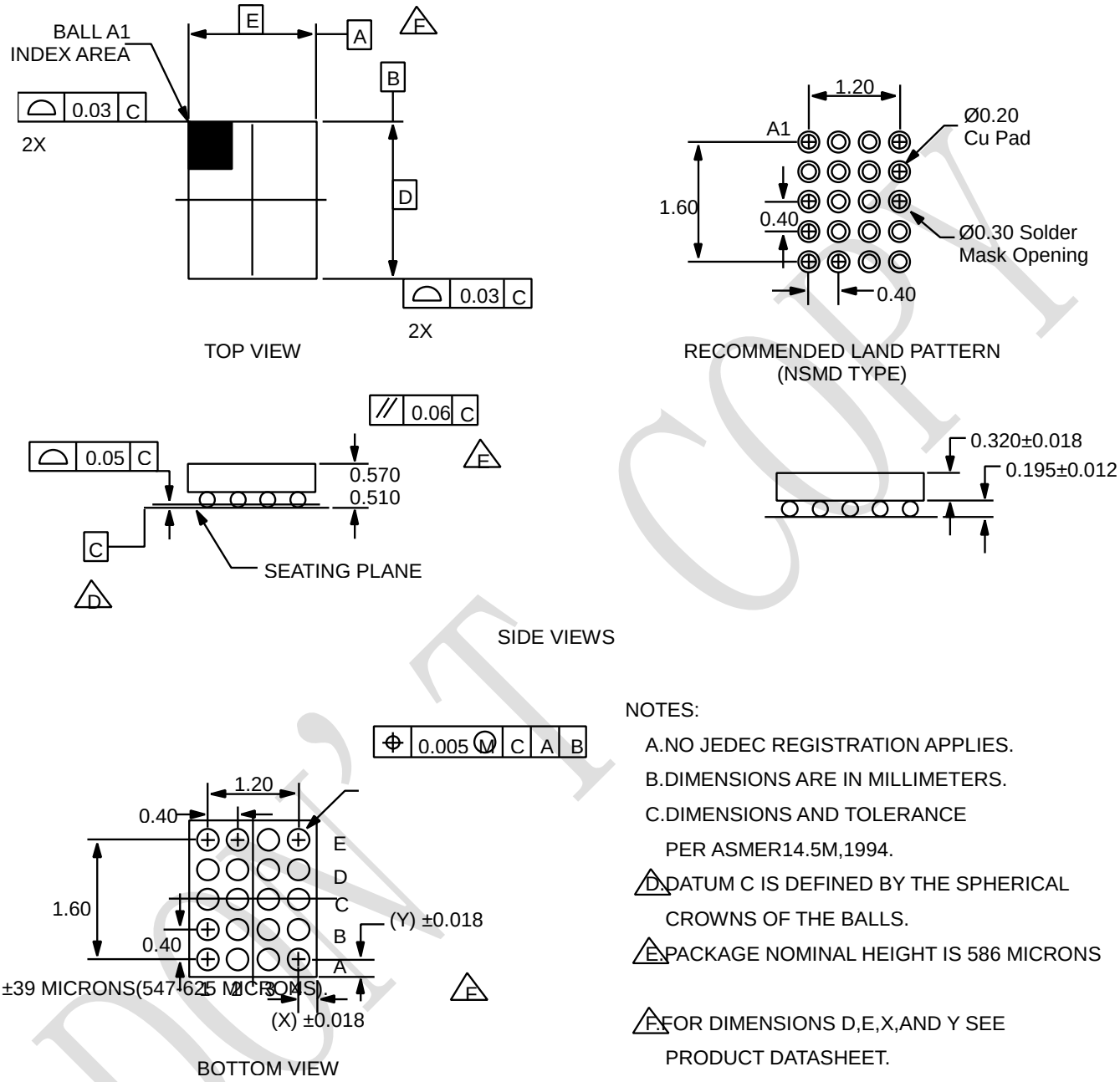
Top View　　Bottom View

Figure 3: WLCSP-20 Pin Assignments

Pin Definitions

Pin#	Name	Description
A1,A2	VBUS	**Charger Input Voltage** and USB-OTG output voltage. Bypass with a 1μF capacitor to PGND
A3	BOOT	**Boost strap capacitor** connection for high side NMOS gate driver. Connect 33nF~100nF ceramic capacitor (voltage rating ≥ 10V) from BOOT to SW pin.
A4	SCL	**I^2C Interface Serial Clock.** This pin should not be left floating.
B1-B3	PMID	**Power Input Voltage.** Power input to the charger regulator, bypass point for the input current sense, and high-voltage input switch. Bypass with a minimum of 10μF, 25V capacitor to PGND.
B4	SDA	**I^2C Interface Serial Data.** This pin should not be left floating.
C1-C3	SW	**Switching Node.** Connect to output inductor.
C4	STAT	**Status.** Open-drain output indicating charge status. The IC pulls this pin LOW when charge is in process.
D1-D3	PGND	**Power Ground.** Power return for gate drive and power transistors. The connection from this pin to the bottom of C_{MID} should be as short as possible.
D4	OTG	**On-The-Go.** Enables boost regulator in conjunction with OTG_EN and OTG_PL bits *(see Table 16)*.
E1	CSIN	**Current-Sense Input.** Connect to the sense resistor in series with the battery. The IC uses this node to sense current into the battery. Bypass this pin with a 0.1μF capacitor to PGND.
E2	DISABLE	**Charge Disable.** If this pin is “1”, charging is disabled. When LOW, charging is controlled by I2C registers.
E3	VREF	**Bias voltage.** Connect to a 1uF capacitor to PGND. The output voltage is limited to 6.5V. Any resistor loading to VREF is **NOT** recommended.
E4	VBAT	**Battery Voltage.** Connect to the positive (+) terminal of the battery pack. Bypass with a 0.1μF capacitor to PGND if the battery is connected through long leads.

Product dimension



NOTES:

A.NO JEDEC REGISTRATION APPLIES.

B.DIMENSIONS ARE IN MILLIMETERS.

C.DIMENSIONS AND TOLERANCE PER ASMER14.5M,1994.

D.DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E.PACKAGE NOMINAL HEIGHT IS 586 MICRONS

F.FOR DIMENSIONS D,E,X,AND Y SEE PRODUCT DATASHEET.

G.DRAWING FILNAME:MKT-UC020AArev2.

Figure 50. 20-Ball WLCSP, 4x5 Array, 0.4mm Pitch, 250µm Ball

Product-Specific Dimensions (mm)

Product	D	E	X	Y
PSC5425	2.040±0.030	2.000±0.030	0.400	0.220

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