Prisemi®

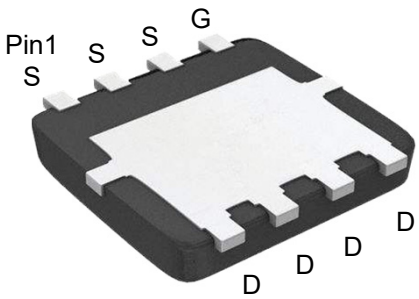
PSM8PN03R3

N-Channel MOSFET

Description

The PSM8PN03R3 uses split gate trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device is suitable for power management and high efficiency applications at high switching frequencies applications.

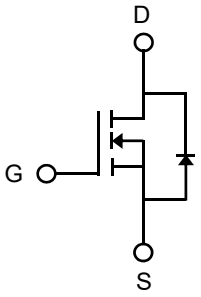
MOSFET Product Summary		
V_{DS}(V)	$R_{DS(on)}$(mΩ)(Typ)	I_D(A)
30	1.8@ V_{GS} = 10V	108
	2.5@ V_{GS} = 4.5V	



PDFN3333-8L
(Bottom View)

Feature

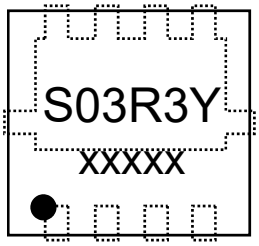
- Low $R_{DS(ON)}$ - Ensures On-State Losses are Minimized
- Excellent Q_{gd} x $R_{DS(ON)}$ Product(FOM)
- Advanced Technology for DC-DC Converts
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- 100% UIS (Avalanche) Rated
- Lead-Free Finish ; RoHS Compliant
- Halogen and Antimony Free. "Green" Device



Circuit Diagram

Applications

- PWM applications
- Load switch
- Power management
- DC-DC Converters
- Wireless Chargers



Marking (Top View)

Absolute maximum rating@25℃

Rating		Symbol	Value	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Drain Current-Continuous(V_{GS}=10V)[1]	T_C=25℃	I_D	108	A
	T_C=100℃		69	
Pulsed Drain Current[2]		I_{DM}	434	A
Total Power Dissipation	T_C=25℃	P_D	38	W
	T_C=100℃		15	
Avalanche Current @ L=0.1mH		I_{AS}	45	A
Avalanche Energy[3]		E_{AS}	101	mJ
Thermal Resistance , Junction-to-Case[5]		$R_{\theta JC}$	3.3	℃/W
Thermal Resistance Junction-to-Ambient[4]		$R_{\theta JA}$	56	℃/W
Junction and Storage Temperature Range		T_J,T_{STG}	-55~+150	℃

Electrical characteristics per line@25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Off Characteristics[6)]						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V,I_D = 10mA	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24V,V_{GS} = 0V	-	-	0.5	mA
Gate-Body Leakage Current	I_{GSS}	V_{GS} = ±20V,V_{DS} = 0V	-	-	±100	nA
On Characteristics[6)]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS},I_D = 250μA	1.0	1.5	2.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V,I_D = 20A	-	1.8	2.1	mΩ
		V_{GS} = 4.5V,I_D = 20A	-	2.5	3.2	
Forward Transconductance	g_{fs}	V_{DS} = 5V,I_D = 20A	-	37	-	S
Diode Forward Voltage	V_{SD}	V_{GS} = 0V,I_S = 2A	-	0.5	0.7	V
Dynamic Characteristics[7)]						
Input Capacitance	C_{lss}	V_{DS} = 15V,V_{GS} = 0V, f = 1.0MHz	-	1437	-	pF
Output Capacitance	C_{oss}		-	1041	-	
Reverse Transfer Capacitance	C_{rss}		-	52	-	
Switching Characteristics[7)]						
Turn-on Delay Time	$t_{d(on)}$	V_{DS} = 15V, V_{GS} = 10V, R_G = 3Ω, I_D = 20A	-	3.0	-	ns
Turn-on Rise Time	t_r		-	11	-	
Turn-Off Delay Time	$t_{d(off)}$		-	16	-	
Turn-Off Fall Time	t_f		-	12	-	
Total Gate Charge(V_{GS} =10V)	Q_g	V_{DS} =15V, I_D = 20A, V_{GS} =10V,	-	21	-	nC
Gate-Source Charge	Q_{gs}		-	3.8	-	
Gate-Drain Charge	Q_{gd}		-	2.6	-	
Gate Plateau Voltage	$V_{plateau}$		-	2.7	-	V
Gate Resistance	R_g	V_{GS}=0V,V_{DS}=0V,f=1MHz	-	3.1	-	Ω
Drain-Source Diode Characteristics[7)]						
Body Diode Reverse Recovery Time	t_{rr}	I_F=20A, d_i/d_t=100A/μs	-	31	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	12	-	nC
Diode Forward Current	I_S	-	-	-	60	A

Notes:
1. This current is chip limited, which is calculated based on $R_{\theta JC}$.
2. This current is calculated on single pulse with 10μs Pulse & Duty Cycle = 1%.
3. Defined by design, not subject to production test, EAS condition: T_J=25℃, V_{DD}=15V, V_{GS}=10V, L=1.0mH.
4. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.
5. Thermal resistance from junction to the exposed drain pad.
6. Short duration pulse test used to minimize self-heating effect.
7. Defined by design, not subject to production.

Typical Characteristics

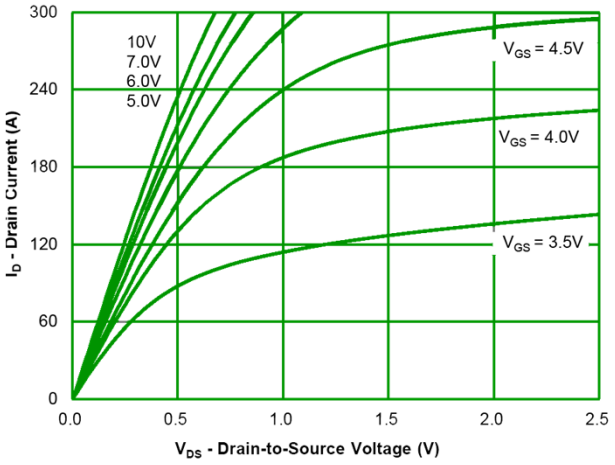


Figure 1: Output Characteristics

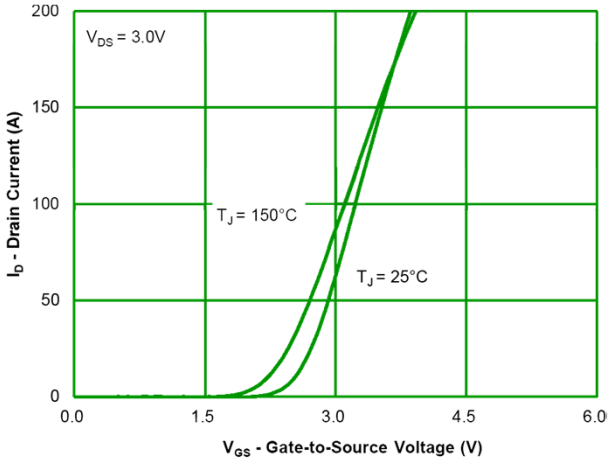


Figure 2: Transfer Characteristics

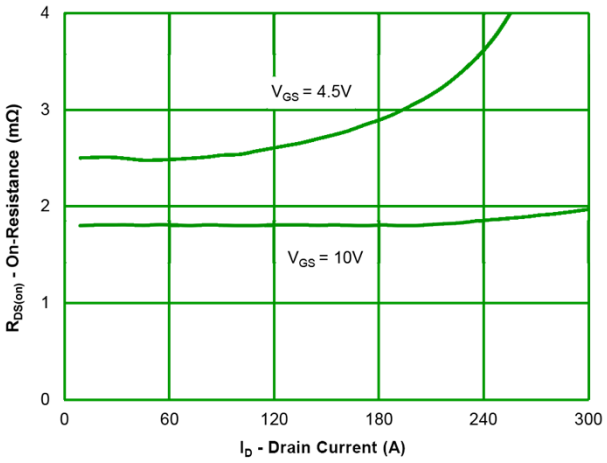


Figure 3: On-Resistance vs. Gate-Source Voltage

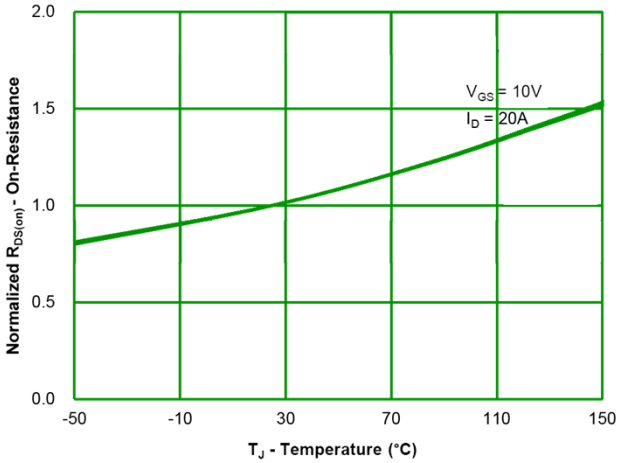


Figure 4: On-Resistance vs. Junction Temperature

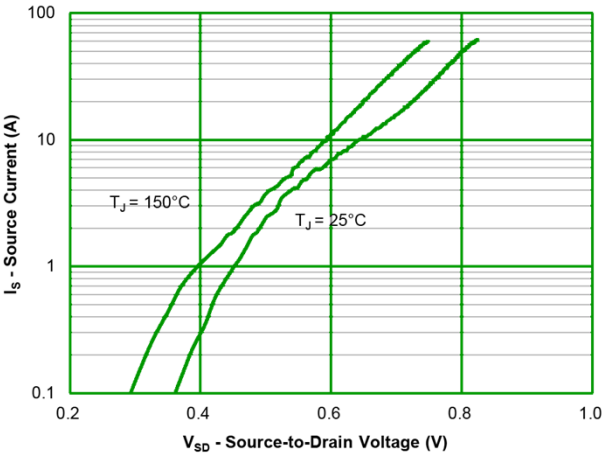


Figure 5: Source-Drain Diode Forward Voltage

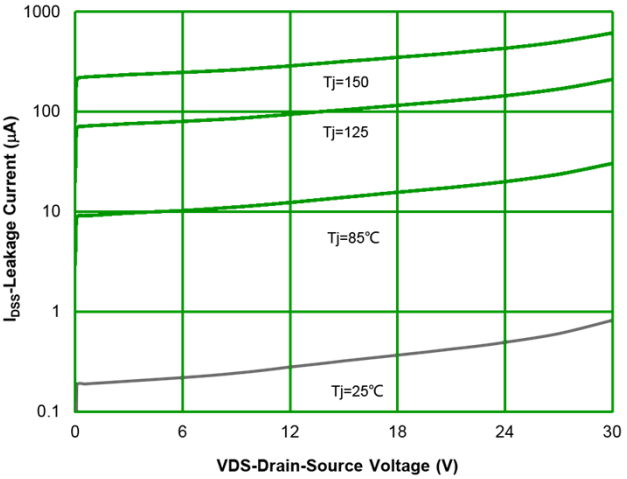


Figure 6:Typical Drain-Source Leakage Current vs Voltage

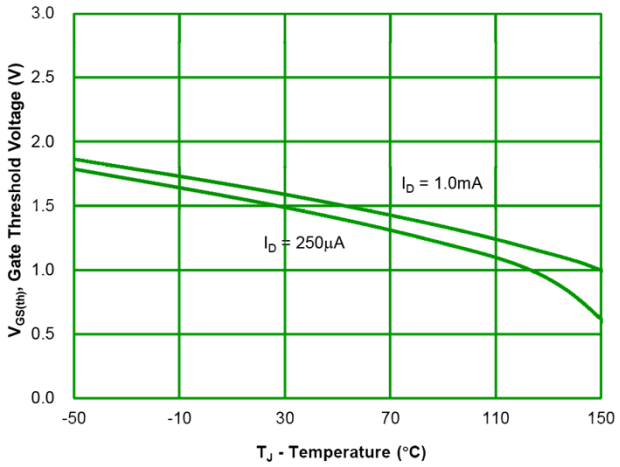


Figure 7: Gate Threshold Variation vs. Junction Temperature

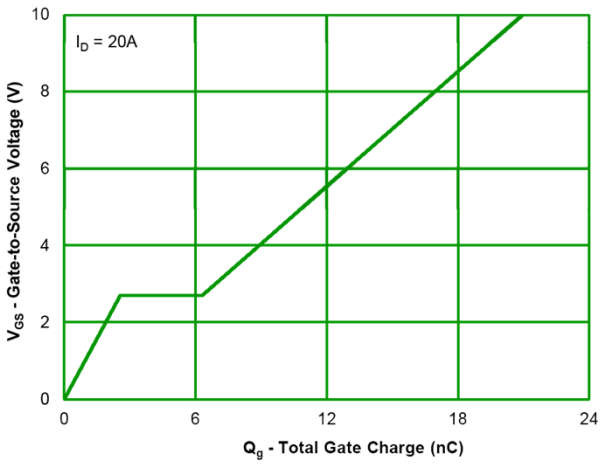


Figure 8: Gate Charge Characteristics

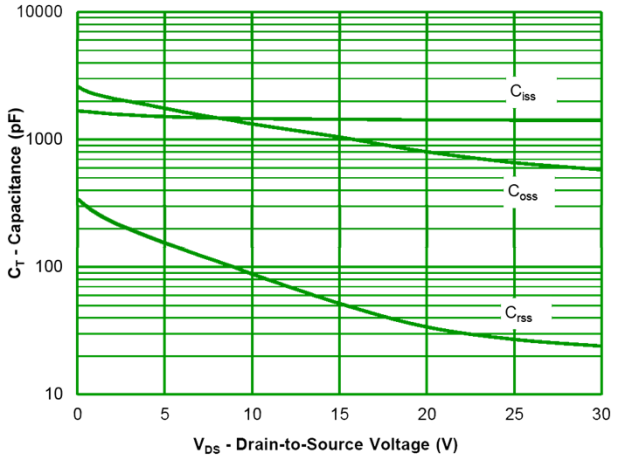


Figure 9: Capacitance Characteristics

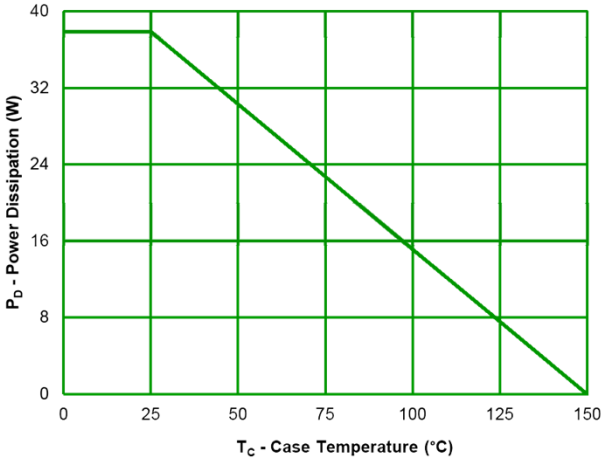


Figure 10: Power Derating

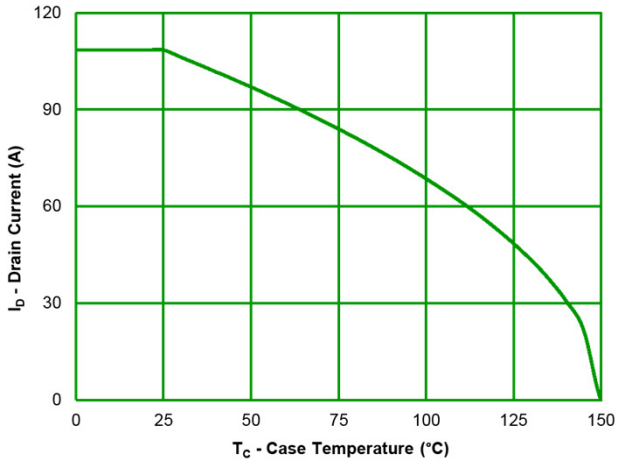


Figure 11: Current Derating

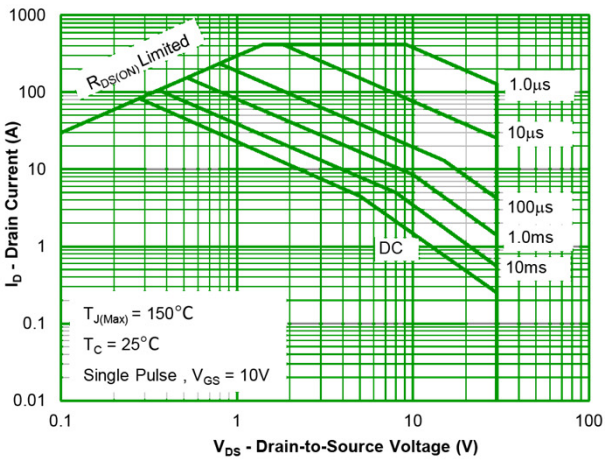


Figure 12: Safe Operating Area

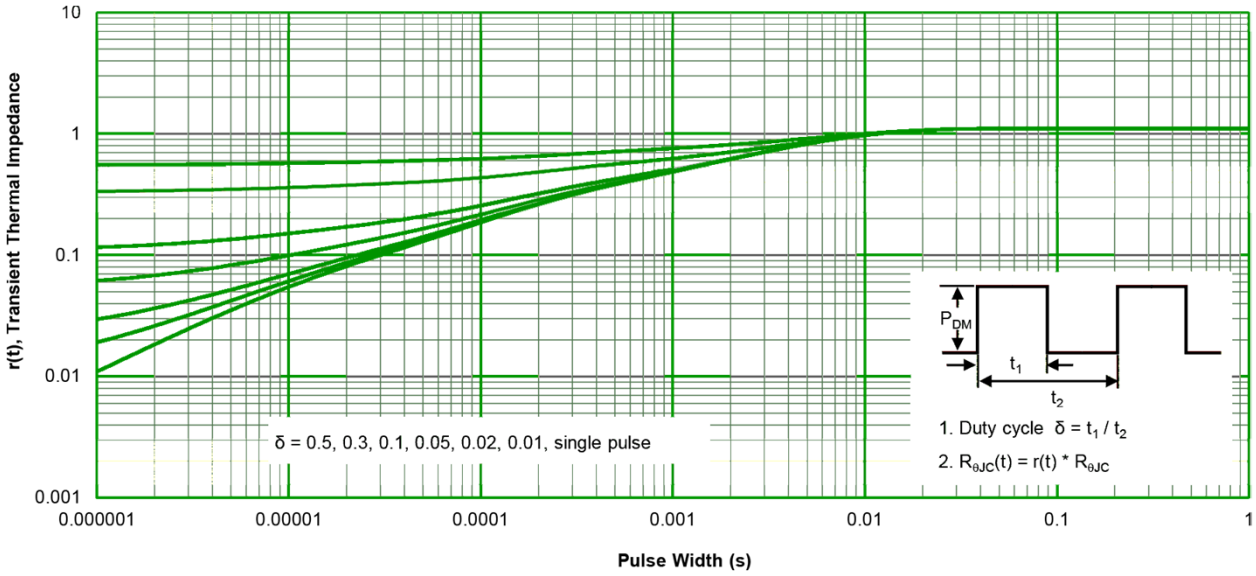
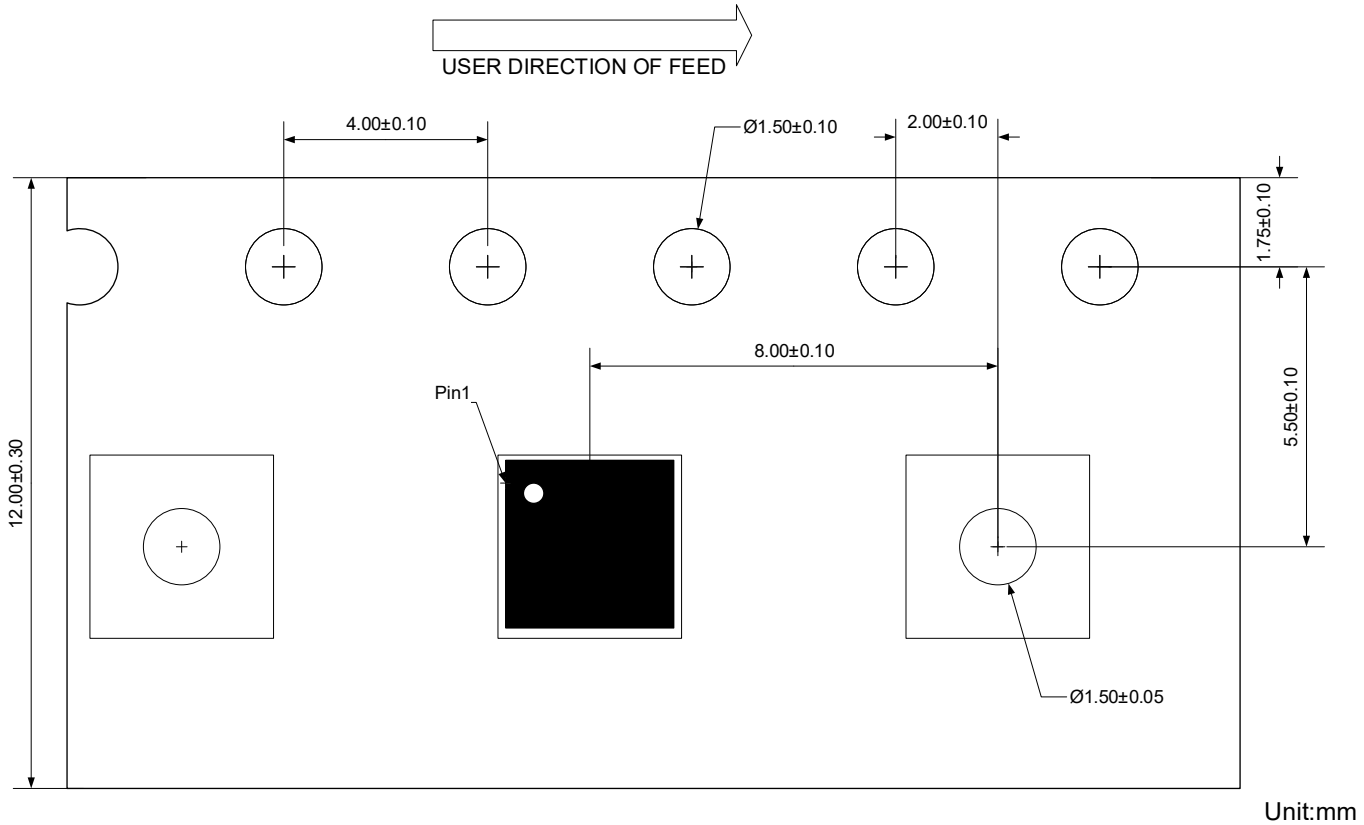


Figure 13: Normalized Maximum Transient Thermal Impedance

Ordering Information

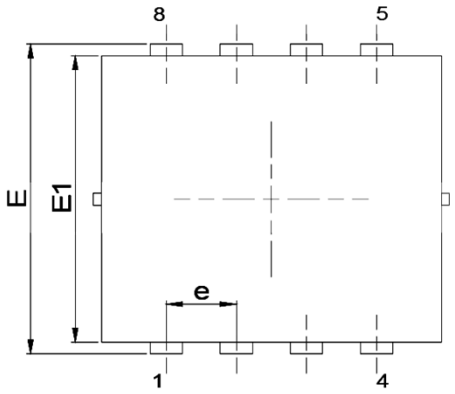
Package	Reel	Shipping
PDFN3333-8L	13"	5000 / Tape & Reel

Load With Information

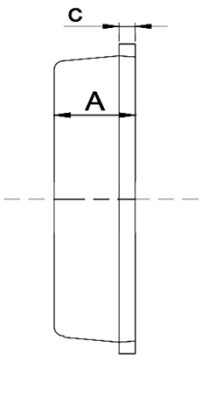


Unit:mm

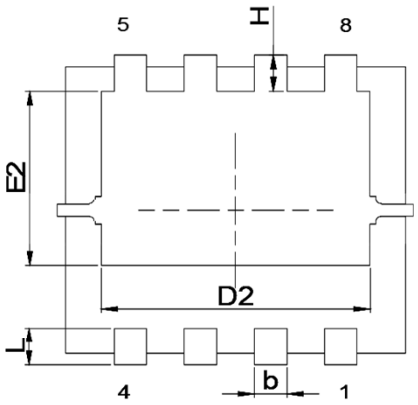
Product Dimension (PDFN3333-8L)



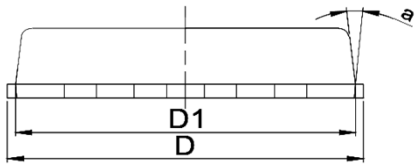
Top View



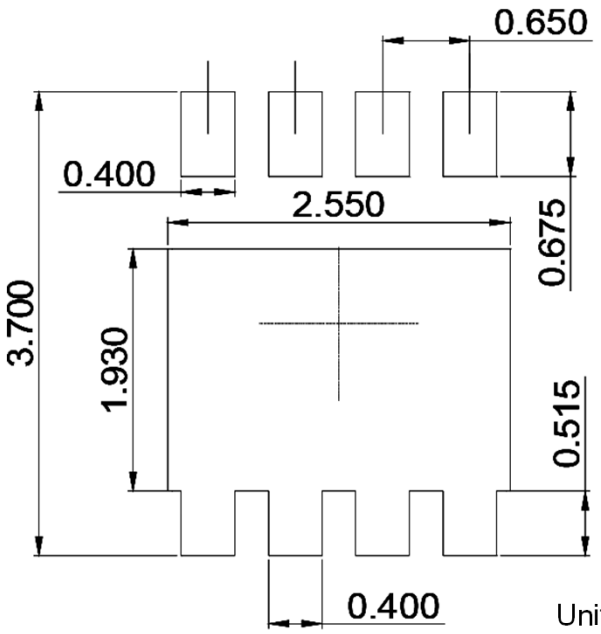
Side View



Bottom View



Front View



Unit: mm

Suggested PCB Layout

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.90	0.028	0.035
b	0.20	0.40	0.008	0.016
c	0.10	0.25	0.004	0.008
D	3.10	3.40	0.126	0.134
D1	3.00	3.25	0.120	0.128
D2	2.35	2.69	0.093	0.106
E	3.20	3.45	0.126	0.136
E1	2.85	3.20	0.112	0.124
E2	1.48	1.98	0.065	0.075
e	0.65 BSC.		0.026 BSC.	
H	0.25	0.60	0.010	0.024
L	0.25	0.50	0.010	0.020
a	-	15°	-	15°

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