



PSMN011-100YSF

NextPower 100V, 10.9 mΩ N-channel MOSFET in LFAK56 package

18 March 2019

Product data sheet

1. General description

NextPower 100V standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial & consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Qualified to 175 °C
- Low $Q_G \times R_{DSon}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFAK56 package
- Wave-solderable LFAK56 package
- Low-stress LFAK leadframe for high-reliability applications

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- LED lighting
- Full-bridge and half-bridge applications
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

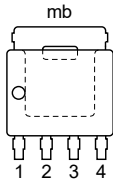
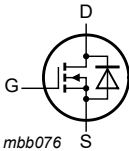
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|----------------------------------|---------------------------------------------------------------------------------------------------------------------------|-----|------|------|------|
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | - | - | 100 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | - | - | 79.5 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | - | 152 | W |
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 8.8 | 10.9 | mΩ |
| | | $V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 100\text{ °C}$; Fig. 13 | - | 13.9 | 17.7 | mΩ |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 20\text{ A}$; $V_{DS} = 50\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 14 ; Fig. 15 | - | 8.1 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | - | 34.3 | - | nC |
| Avalanche ruggedness | | | | | | |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---------------------------|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|-----|------|
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D = 27\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped; Fig. 4 | [1] | - | - | 173 | mJ |
| Source-drain diode | | | | | | | |
| Q_r | recovered charge | $I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 50\text{ V}$; Fig. 18 | | - | 36.5 | - | nC |

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|----------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------|
| 1 | S | source |  <p>LPAK56; Power-SO8 (SOT669)</p> |  <p><i>mbb076</i></p> |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|----------------|-------------------|------------------------------------------------------------|---------|
| | Name | Description | Version |
| PSMN011-100YSF | LPAK56; Power-SO8 | plastic, single-ended surface-mounted package; 4 terminals | SOT669 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|----------------|--------------|
| PSMN011-100YSF | 11FS10Y |

8. Limiting values

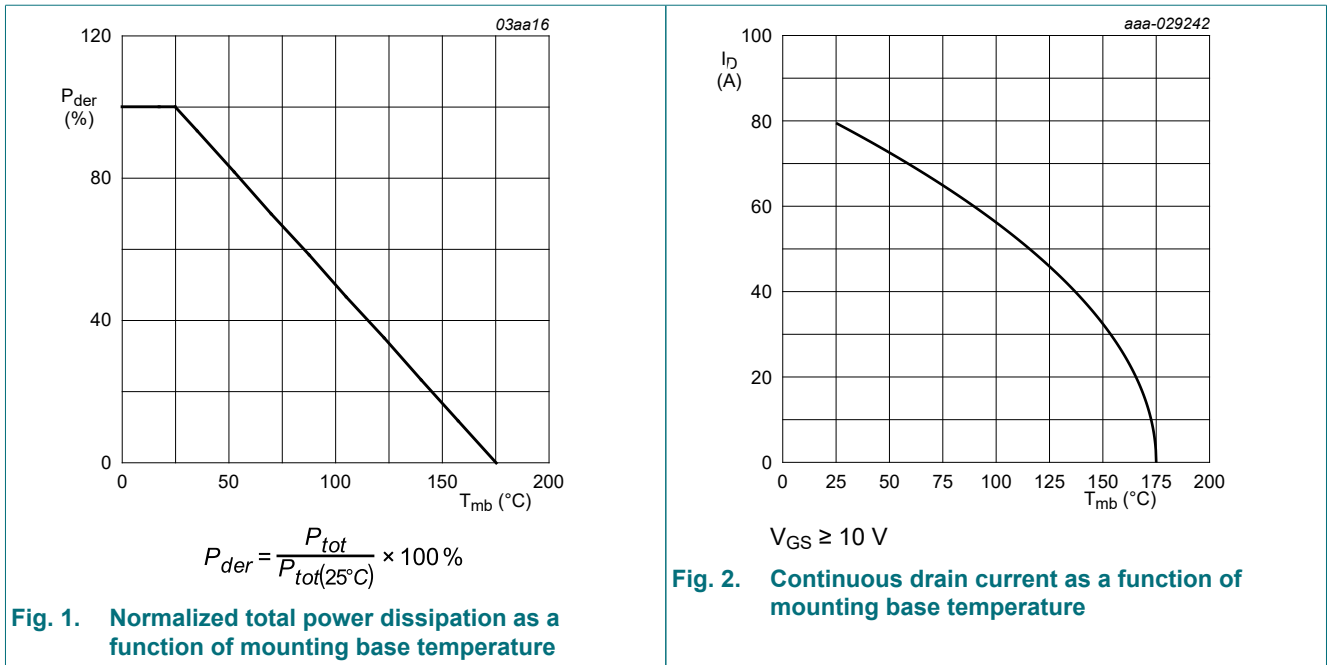
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|-----------|-------------------------|---------------------------------------------------------------------------------------------------|--|-----|------|------|
| V_{DS} | drain-source voltage | $25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$ | | - | 100 | V |
| V_{DGR} | drain-gate voltage | $25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$ | | - | 100 | V |
| V_{GS} | gate-source voltage | | | -20 | 20 | V |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1 | | - | 152 | W |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2 | | - | 79.5 | A |
| | | $V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^\circ\text{C}$; Fig. 2 | | - | 56.2 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\ \mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 3 | | - | 318 | A |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|----------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|--------|
| T _{stg} | storage temperature | | -55 | 175 | °C |
| T _j | junction temperature | | -55 | 175 | °C |
| T _{slid(M)} | peak soldering temperature | | - | 260 | °C |
| Source-drain diode | | | | | |
| I _S | source current | T _{mb} = 25 °C | - | 79.5 | A |
| I _{SM} | peak source current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C | - | 318 | A |
| Avalanche ruggedness | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | I _D = 27 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4 | [1] | - | 173 mJ |
| I _{AS} | non-repetitive avalanche current | V _{sup} = 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω | [1] | - | 27 A |

[1] Protected by 100% test



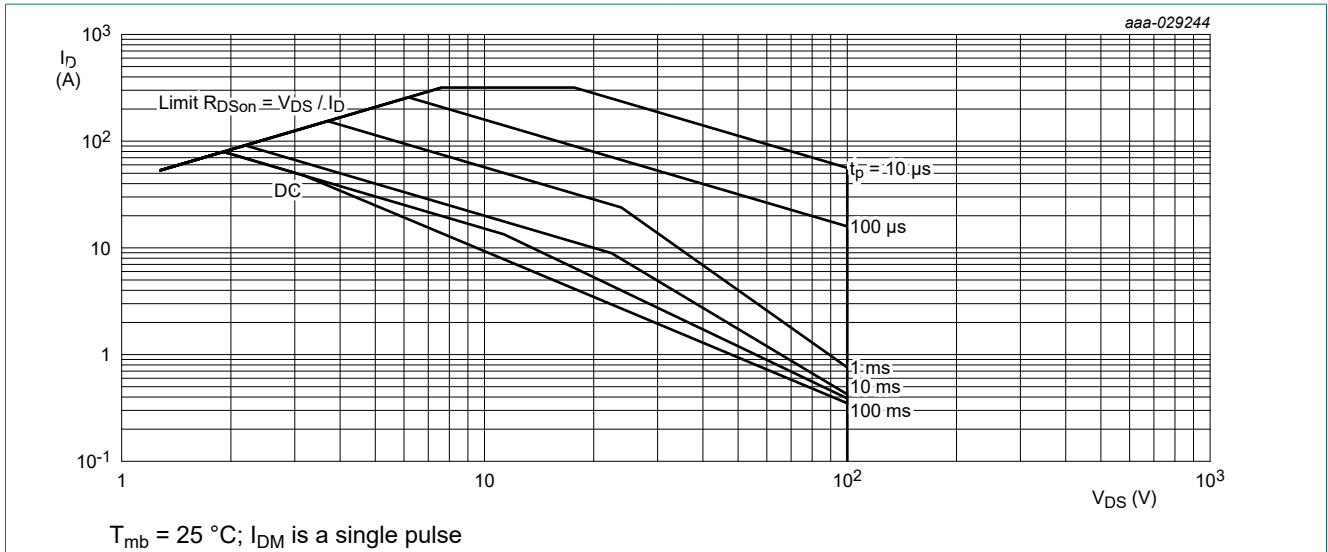


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

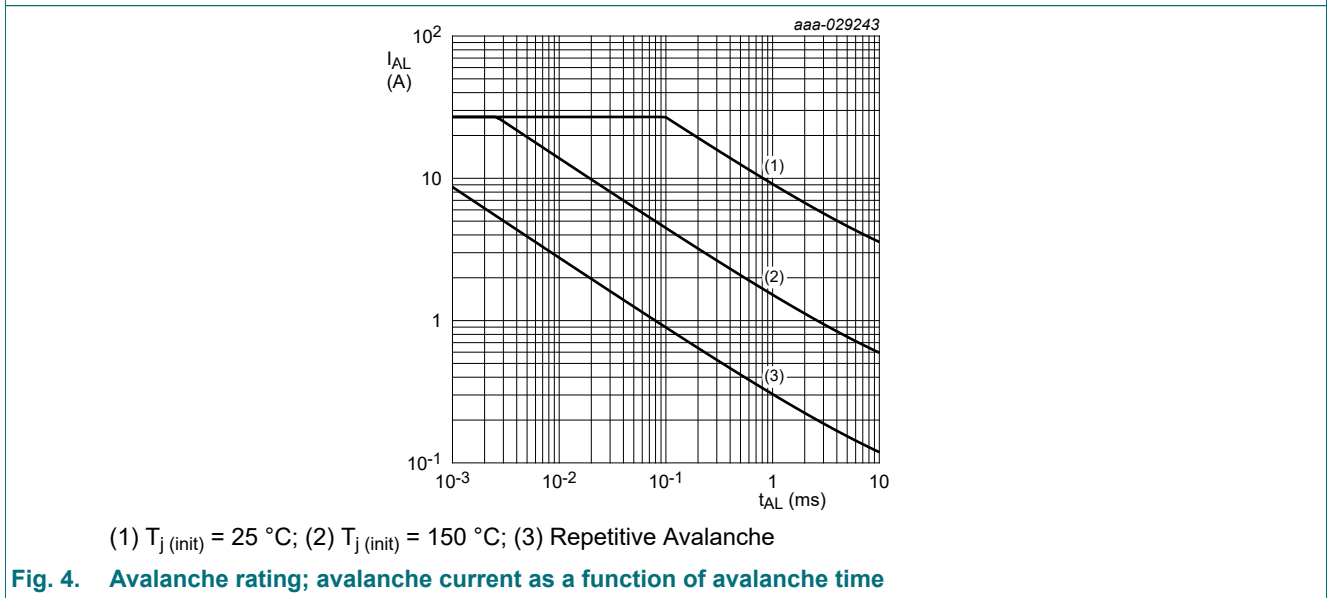


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---------------------------------------------------|------------------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | 0.87 | 0.99 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Fig. 6 | - | 42 | - | K/W |
| | | Fig. 7 | - | 85 | - | K/W |

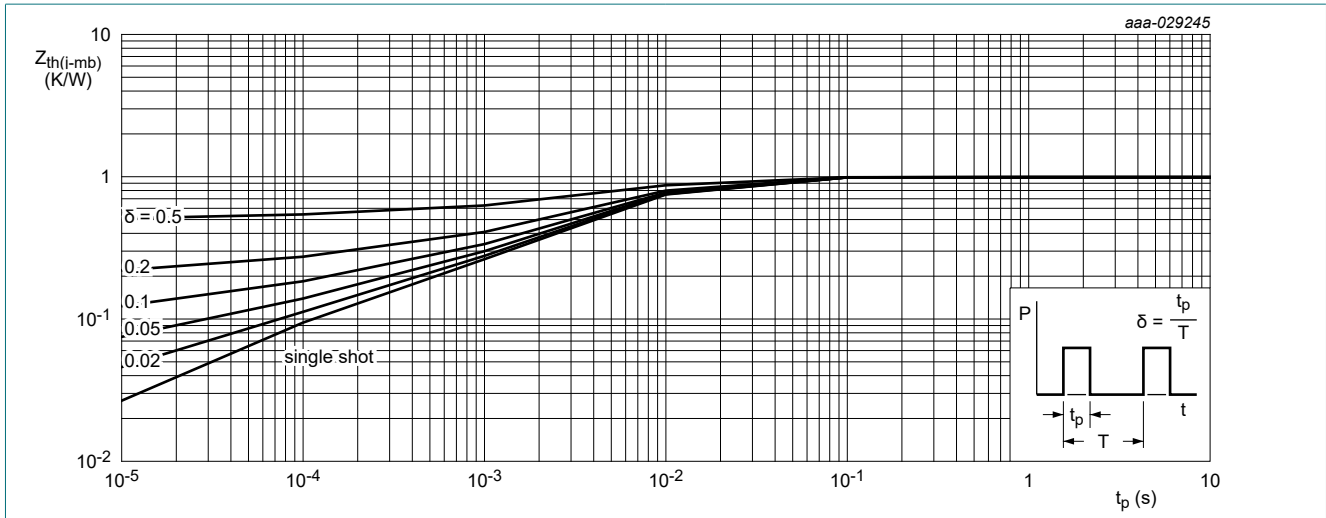


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-027933

Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

aaa-027935

70 μm thick copper on FR4 board

Fig. 6. PCB layout for resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------------------------------|---------------------------------------------------------------------------------|-----|------|-----|------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 100 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 90 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$ | - | 3.6 | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$ | - | 1.9 | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$ | 2 | 3.1 | 4 | V |
| $\Delta V_{GS(th)}/\Delta T$ | gate-source threshold voltage variation with temperature | $25 \text{ }^\circ C \leq T_j \leq 175 \text{ }^\circ C$ | - | -7.9 | - | mV/K |
| I_{DSS} | drain leakage current | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 5 | μA |
| | | $V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$ | - | - | 100 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 5 | 100 | nA |
| | | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$ | - | 5 | 100 | nA |

NextPower 100V, 10.9 mΩ N-channel MOSFET in LPAK56 package

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-----|------|------|------|
| R _{DSon} | drain-source on-state resistance | V _{GS} = 10 V; I _D = 20 A; T _J = 25 °C; Fig. 12 | - | 8.8 | 10.9 | mΩ |
| | | V _{GS} = 7 V; I _D = 20 A; T _J = 25 °C; Fig. 12 | - | 10.2 | 15.2 | mΩ |
| | | V _{GS} = 10 V; I _D = 20 A; T _J = 100 °C; Fig. 13 | - | 13.9 | 17.7 | mΩ |
| | | V _{GS} = 10 V; I _D = 20 A; T _J = 175 °C; Fig. 13 | - | 20 | 25.5 | mΩ |
| R _G | gate resistance | f = 1 MHz; T _J = 25 °C | - | 1.8 | - | Ω |
| Dynamic characteristics | | | | | | |
| Q _{G(tot)} | total gate charge | I _D = 20 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15 | - | 34.3 | - | nC |
| | | I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V | - | 16.4 | - | nC |
| Q _{GS} | gate-source charge | I _D = 20 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15 | - | 10.6 | - | nC |
| Q _{GS(th)} | pre-threshold gate-source charge | | - | 6.4 | - | nC |
| Q _{GS(th-pl)} | post-threshold gate-source charge | | - | 4.2 | - | nC |
| Q _{GD} | gate-drain charge | | - | 8.1 | - | nC |
| V _{GS(pl)} | gate-source plateau voltage | I _D = 20 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15 | - | 4.9 | - | V |
| C _{iss} | input capacitance | V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 16 | - | 2258 | - | pF |
| C _{oss} | output capacitance | | - | 395 | - | pF |
| C _{rss} | reverse transfer capacitance | | - | 21 | - | pF |
| t _{d(on)} | turn-on delay time | V _{DS} = 50 V; R _L = 2.5 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C | - | 10.2 | - | ns |
| t _r | rise time | | - | 12.1 | - | ns |
| t _{d(off)} | turn-off delay time | | - | 21.3 | - | ns |
| t _f | fall time | | - | 12.8 | - | ns |
| Source-drain diode | | | | | | |
| V _{SD} | source-drain voltage | I _S = 20 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17 | - | 0.85 | 1.2 | V |
| t _{rr} | reverse recovery time | I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; Fig. 18 | - | 38.4 | - | ns |
| Q _r | recovered charge | | - | 36.5 | - | nC |

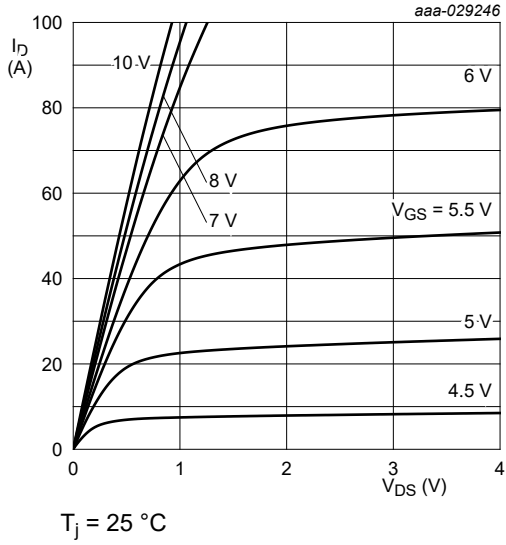


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

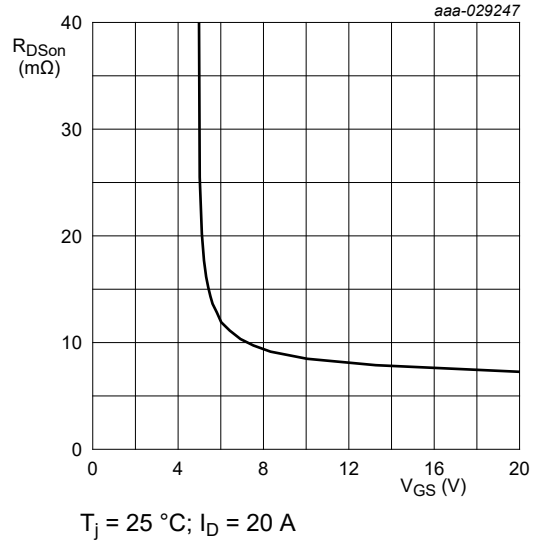


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

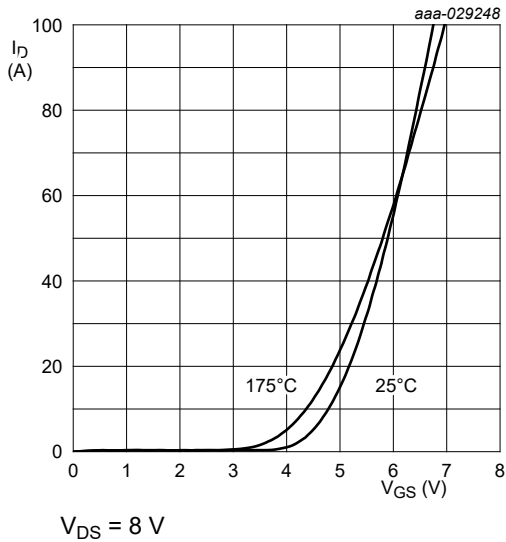


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

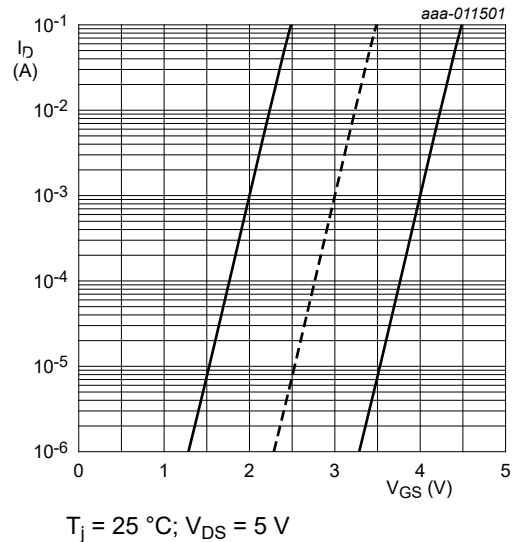


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

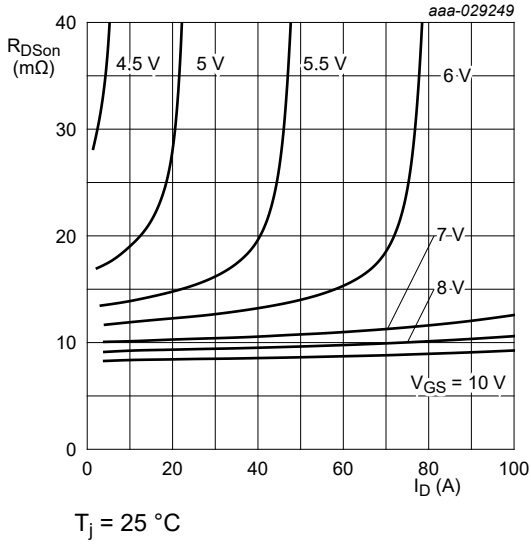
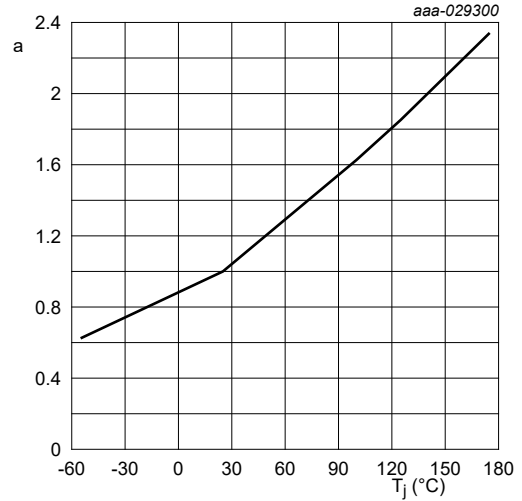


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

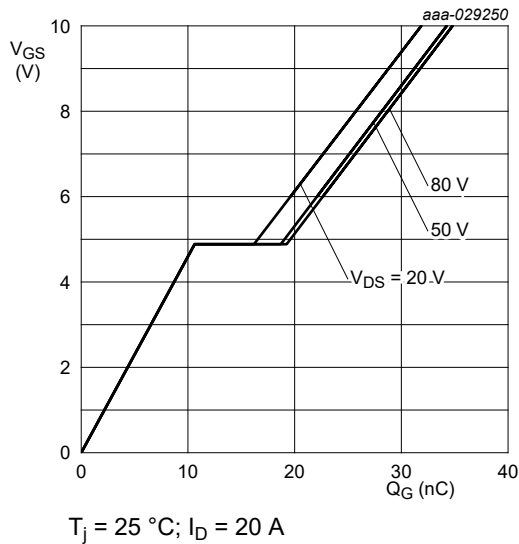


Fig. 14. Gate-source voltage as a function of gate charge; typical values

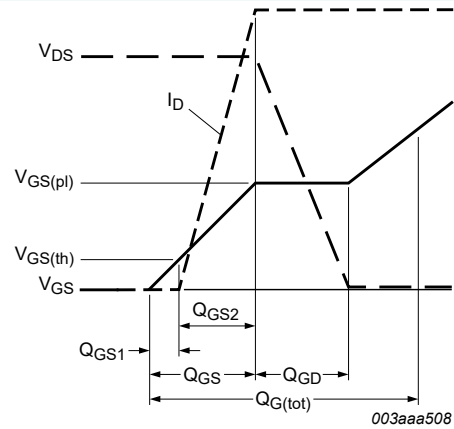


Fig. 15. Gate charge waveform definitions

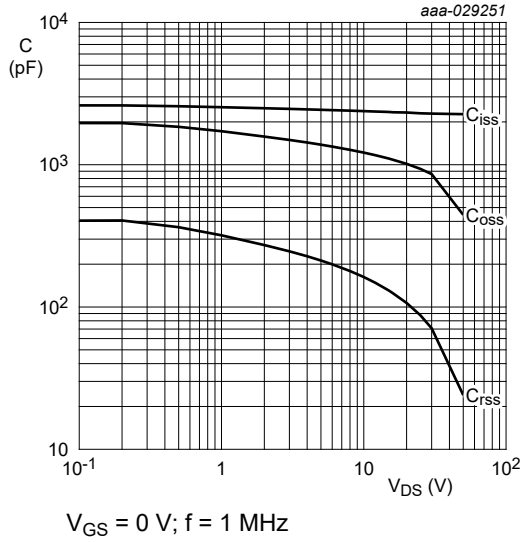


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

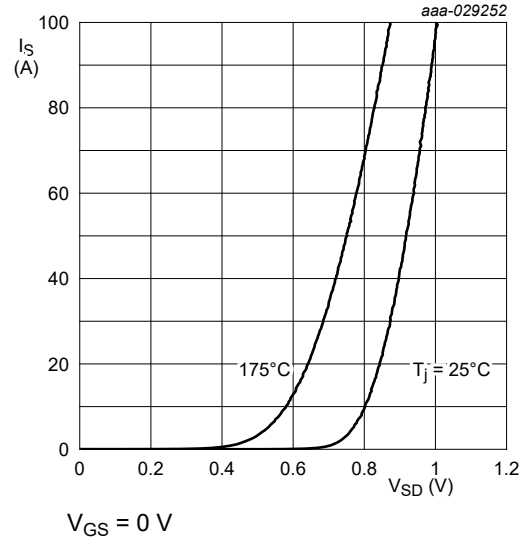


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

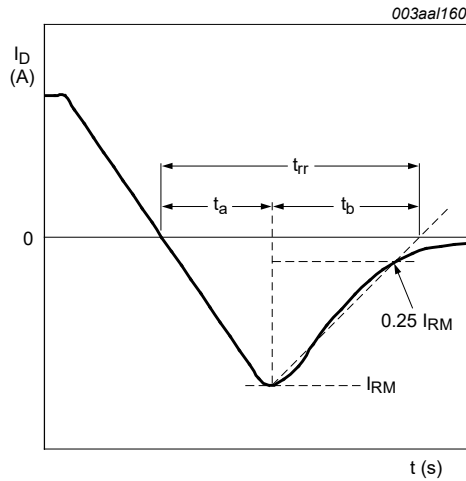


Fig. 18. Reverse recovery timing definition

11. Package outline

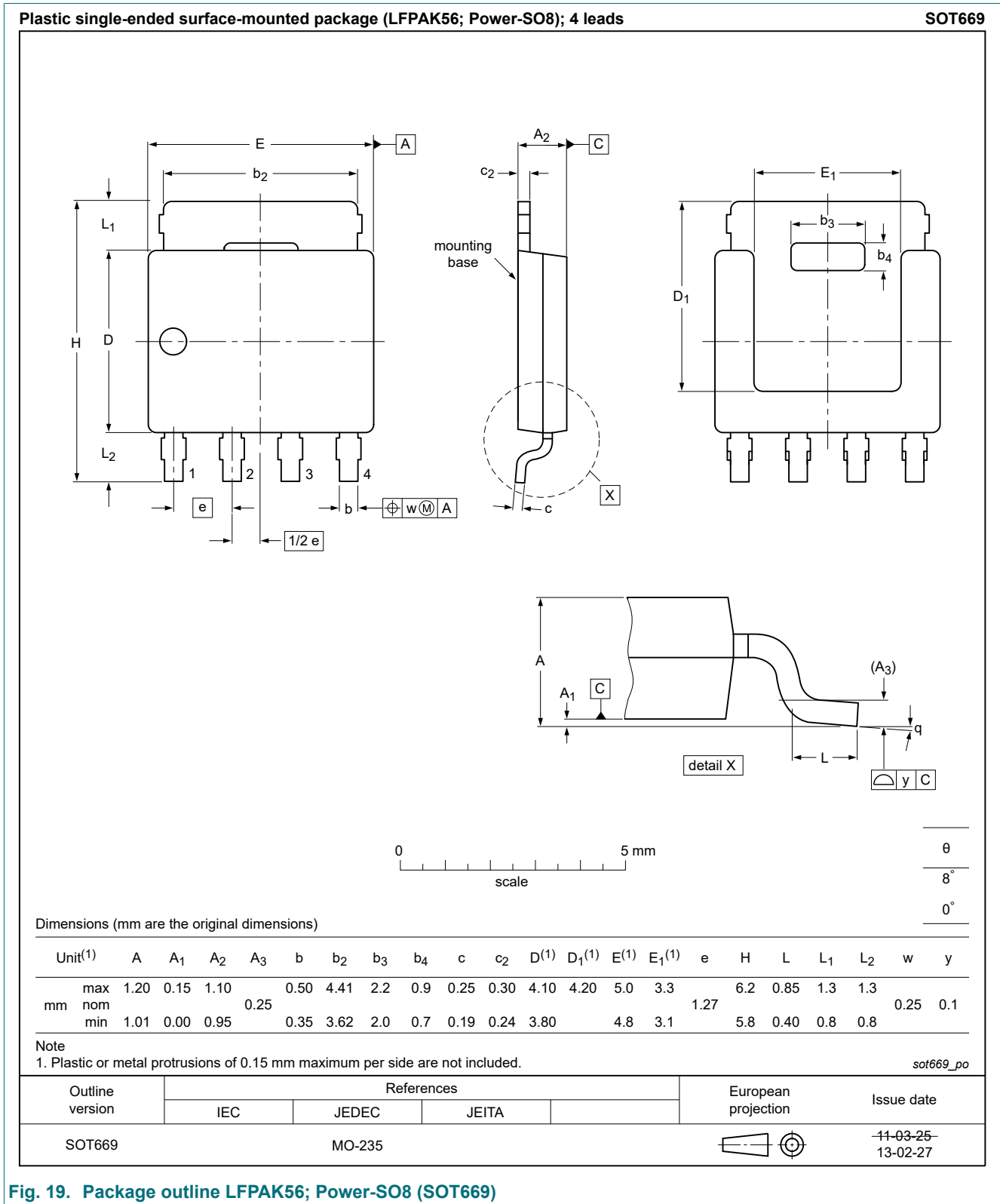


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering

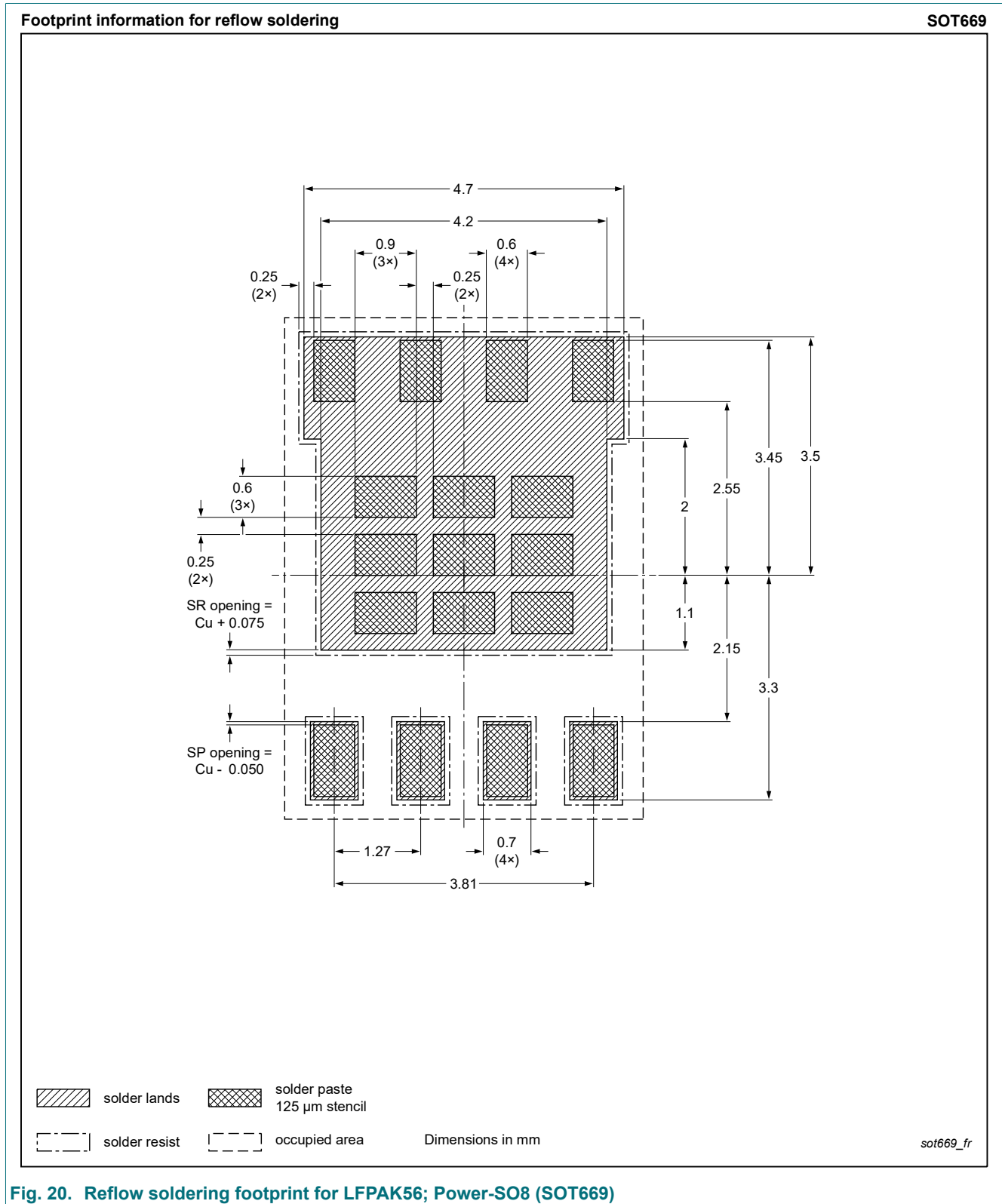
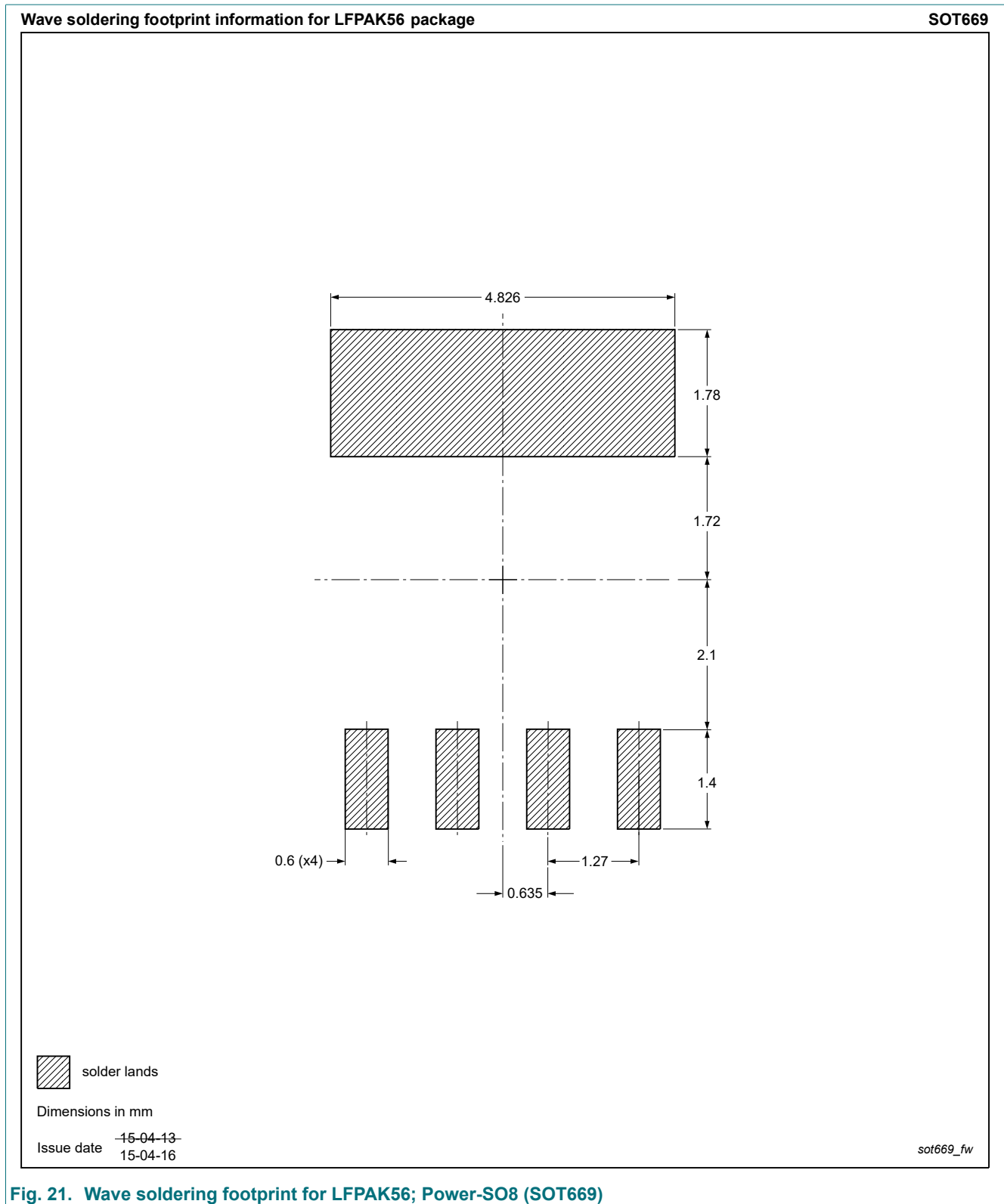


Fig. 20. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)



13. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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