



# PSMN012-100YS

N-channel 100V 12mΩ standard level MOSFET in LPAK

Rev. 04 — 23 February 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel MOSFET in LPAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power converters
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

### 1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

### 1.4 Quick reference data

Table 1. Quick reference

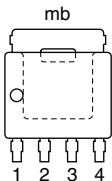
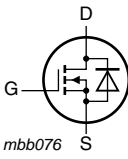
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	-	60	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	130	W
$T_j$	junction temperature		-55	-	175	°C
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; $I_D = 60\text{ A}$ ; $V_{sup} \leq 100\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped	-	-	170	mJ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}$ ; $I_D = 45\text{ A}$ ;	-	19	-	nC
$Q_{G(tot)}$	total gate charge	$V_{DS} = 50\text{ V}$ ; see <a href="#">Figure 14</a> and <a href="#">15</a>	-	64	-	nC

Table 1. Quick reference ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A};$ $T_j = 100\text{ °C};$ see <a href="#">Figure 12</a>	-	-	23	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 13</a>	-	10	12	mΩ

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK)

## 3. Ordering information

Table 3. Ordering information

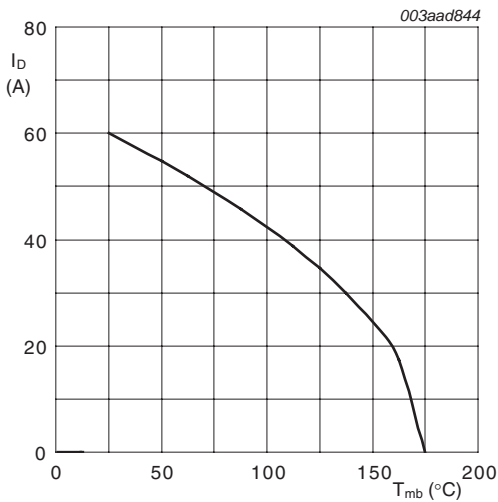
Type number	Package		Version
	Name	Description	
PSMN012-100YS	LPAK	plastic single-ended surface-mounted package (LPAK); 4 leads	SOT669

### 4. Limiting values

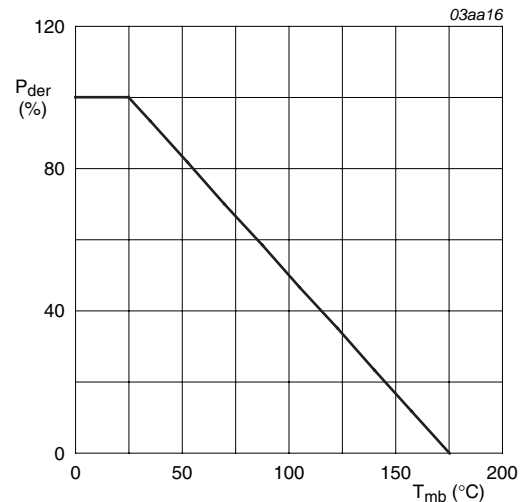
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	100	V
V <sub>DGR</sub>	drain-gate voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	100	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>	-	43	A
		T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a>	-	60	A
I <sub>DM</sub>	peak drain current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 3</a>	-	242	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	130	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	60	A
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>mb</sub> = 25 °C	-	242	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 60 A; V <sub>sup</sub> ≤ 100 V; R <sub>GS</sub> = 50 Ω; unclamped	-	170	mJ

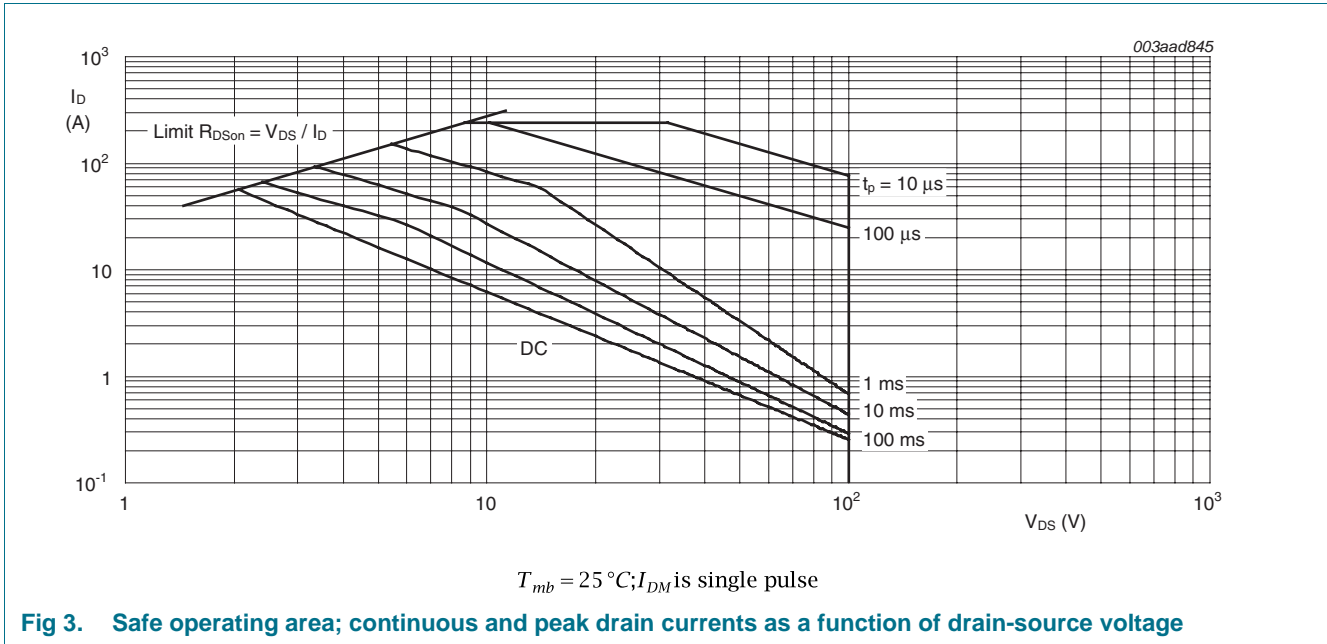


**Fig 1. Continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	0.5	1.1	K/W

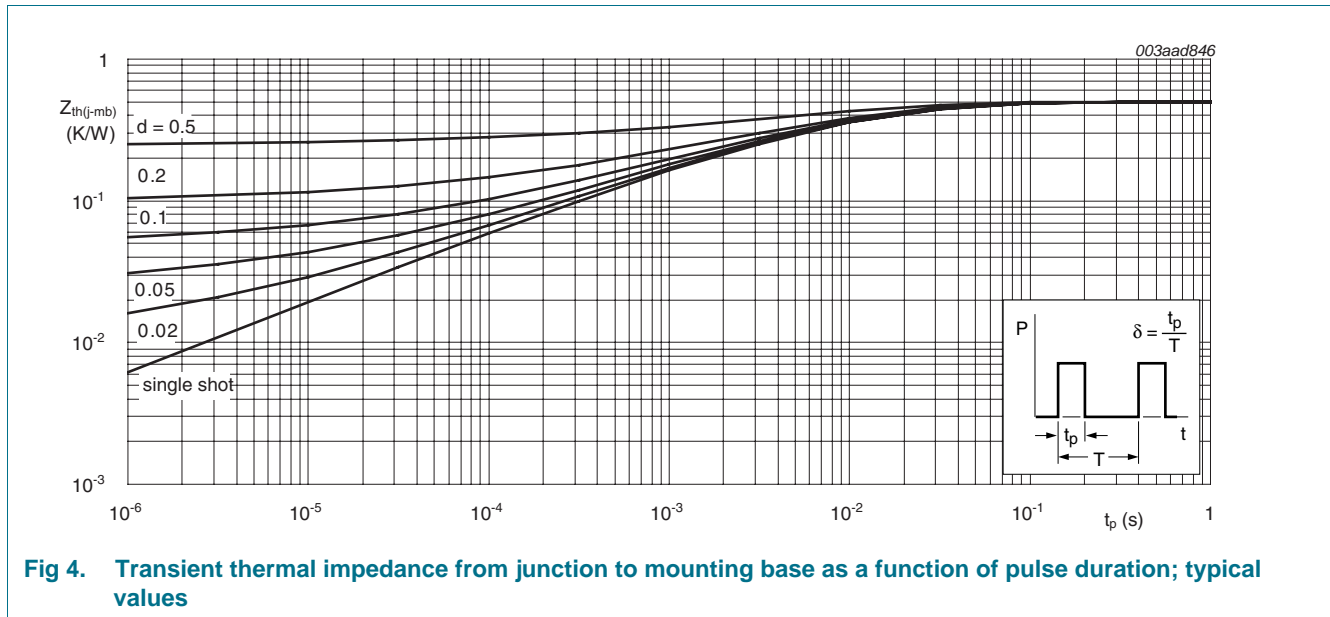


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration; typical values

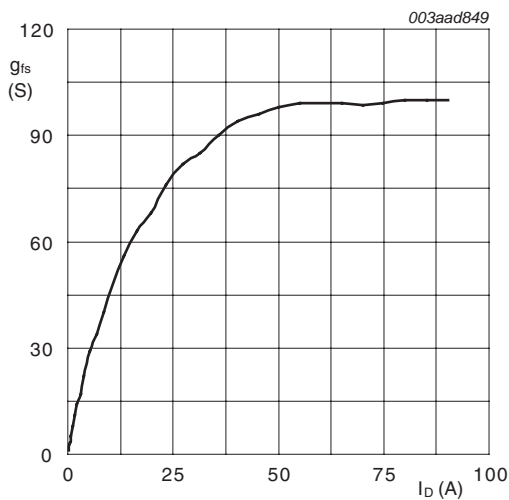
## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	90	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	0.95	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> and <a href="#">10</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	-	-	4.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	-	100	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.06	5	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	-	23	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a>	-	27	35.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a>	-	10	12	mΩ
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	0.7	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	51	-	nC
		$I_D = 45 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> and <a href="#">15</a>	-	64	-	nC
$Q_{GS}$	gate-source charge		-	14.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 45 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a>	-	10.2	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	4.7	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 45 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ see <a href="#">Figure 14</a> and <a href="#">15</a>	-	19	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50 \text{ V};$ see <a href="#">Figure 14</a> and <a href="#">15</a>	-	4.4	-	V
$C_{iss}$	input capacitance	$V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 16</a>	-	3500	-	pF
$C_{oss}$	output capacitance		-	246	-	pF
$C_{rss}$	reverse transfer capacitance		-	149	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 1.1 \text{ }^\circ\Omega; V_{GS} = 10 \text{ V};$	-	23	-	ns
$t_r$	rise time	$R_{G(ext)} = 4.7 \text{ }^\circ\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	31	-	ns
$t_{d(off)}$	turn-off delay time		-	52.5	-	ns
$t_f$	fall time		-	25	-	ns

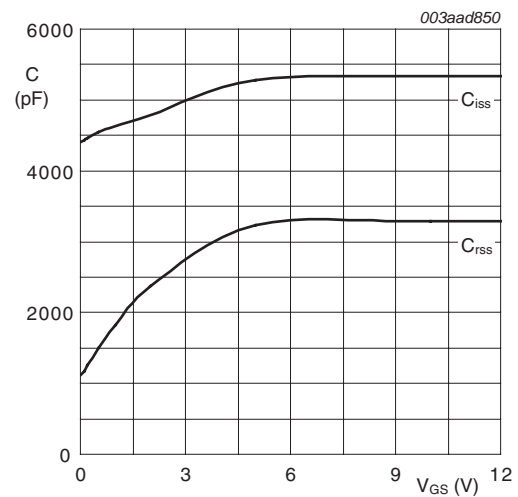
Table 6. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.8	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 15\text{ A}$ ; $di_S/dt = 100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	56	-	ns
$Q_r$	recovered charge	$V_{DS} = 50\text{ V}$	-	129	-	nC



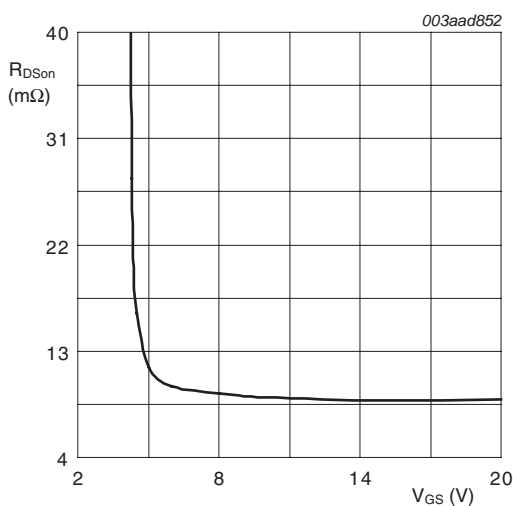
$T_j = 25\text{ °C}$ ;  $V_{DS} = 20\text{ V}$

Fig 5. Forward transconductance as a function of drain current; typical values



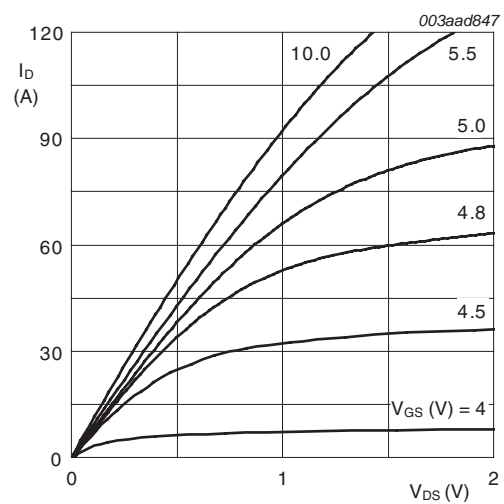
$V_{DS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

Fig 6. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



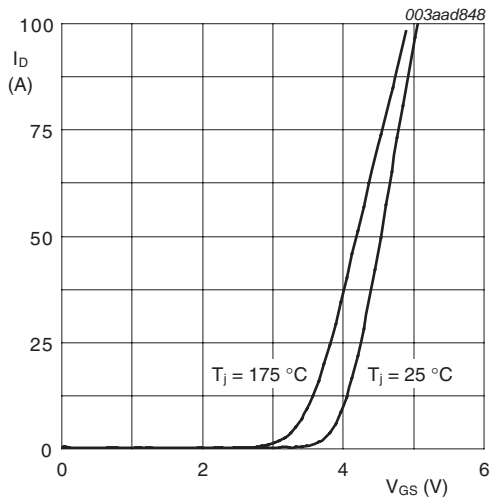
$T_j = 25\text{ °C}$ ;  $I_D = 15\text{ A}$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



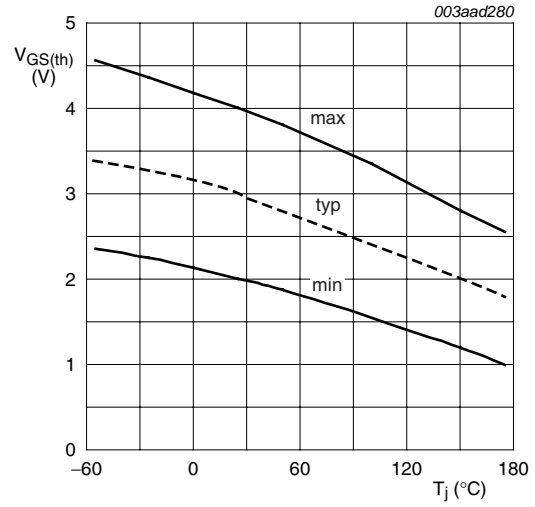
$T_j = 25\text{ °C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



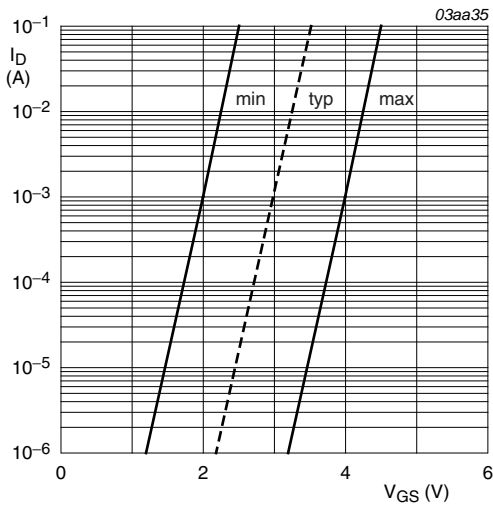
$$V_{DS} > I_D \times R_{DSon}$$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



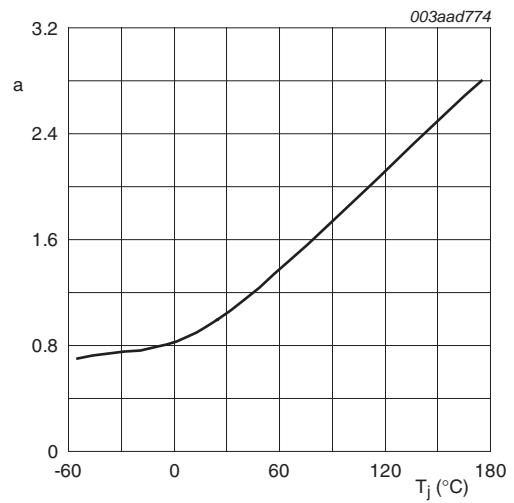
$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$$T_j = 25 \text{ °C}; V_{DS} = 5 \text{ V}$$

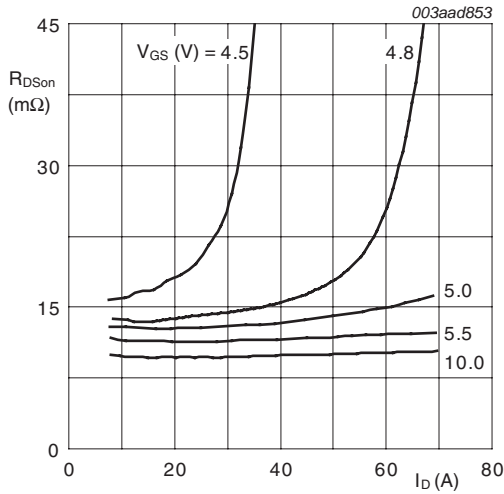
Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25 \text{ °C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature





$T_j = 25^\circ C$

Fig 13. Drain-source on-state resistance as a function of drain current; typical values

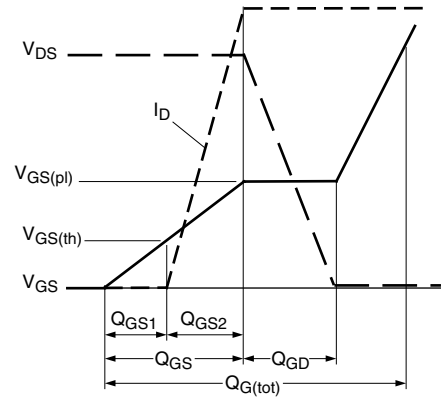
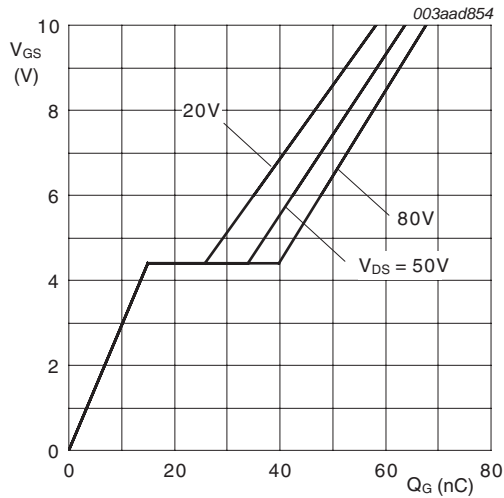
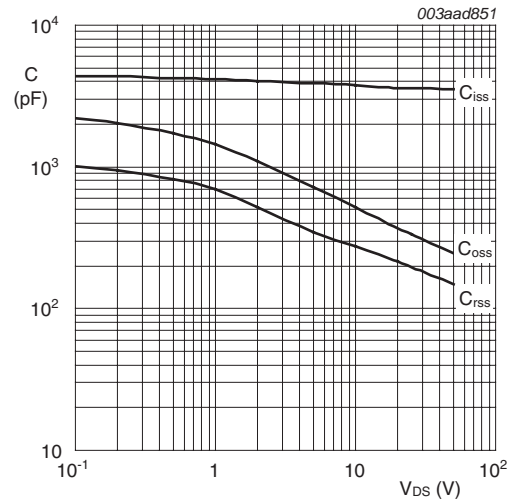


Fig 14. Gate charge waveform definitions



$T_j = 25^\circ C; I_D = 45A$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

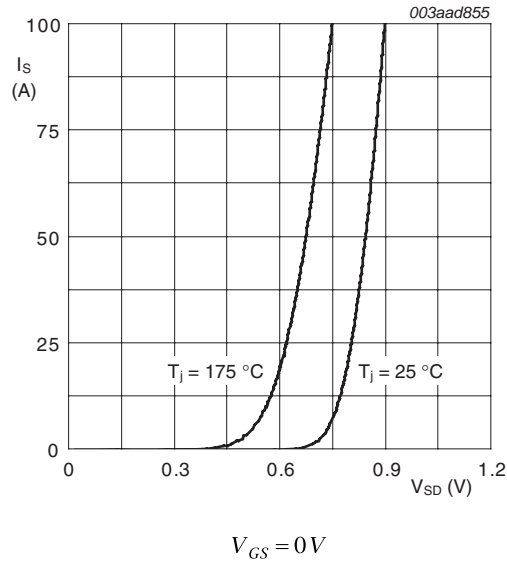
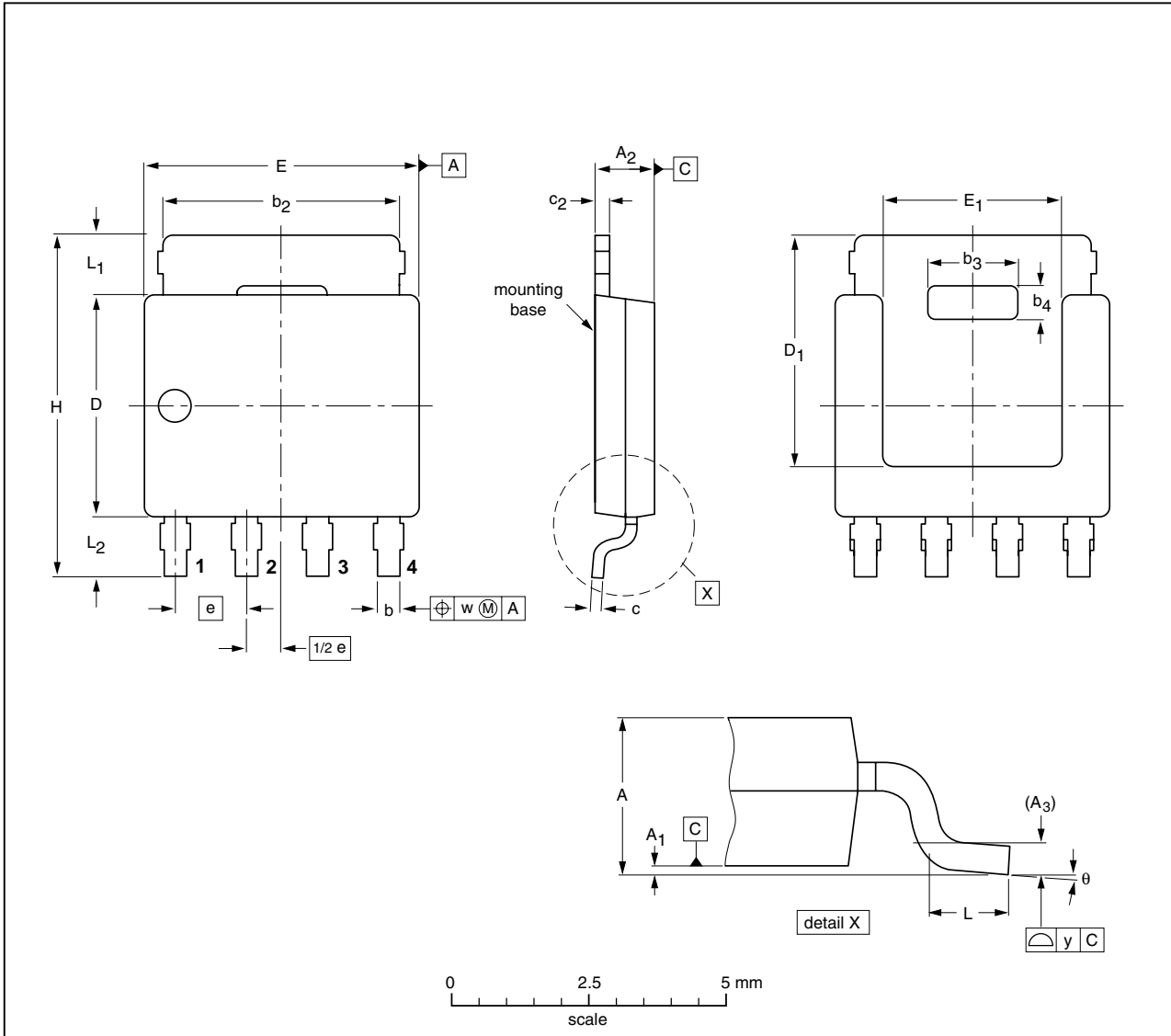


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup> <sub>max</sub>	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				04-10-13 06-03-16

Fig 18. Package outline SOT669 (LPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN012-100YS_4	20100223	Product data sheet	-	PSMN012-100YS_3
Modifications:	• Status changed from objective to product.			
PSMN012-100YS_3	20100107	Product data sheet	-	PSMN012-100YS_2
PSMN012-100YS_2	20091214	Objective data sheet	-	PSMN012-100YS_1
PSMN012-100YS_1	20091022	Objective data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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## 11. Contents

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