

1. Description

SiliconMAX^{TM1} products use the latest Philips TrenchMOS^{TM2} technology to achieve the lowest possible on-state resistance in a SOT96-1 (SO8) package.

Product availability:

PSMN038-100K in SOT96-1 (SO8).

2. Features

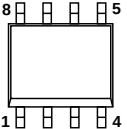
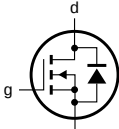
- Very low on-state resistance
- Fast switching
- TrenchMOSTM technology.

3. Applications

- DC to DC convertor
- Computer motherboards
- Switch mode power supplies.

4. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	 Top view MBK187	 MBB076
4	gate (g)		
5,6,7,8	drain (d)		

SOT96-1 (SO8)

1. SiliconMAX is a trademark of Royal Philips Electronics.
2. TrenchMOS is a trademark of Royal Philips Electronics.

5. Quick reference data

Table 2: Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to $150\text{ }^{\circ}\text{C}$	–	100	V
I_D	drain current (DC)	$T_{sp} = 80\text{ }^{\circ}\text{C}$; Figure 2 and 3	–	6.3	A
P_{tot}	total power dissipation	$T_{sp} = 80\text{ }^{\circ}\text{C}$; Figure 1	–	3.5	W
T_j	junction temperature		–	150	$^{\circ}\text{C}$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 5.2\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$	33	38	m Ω

6. Limiting values

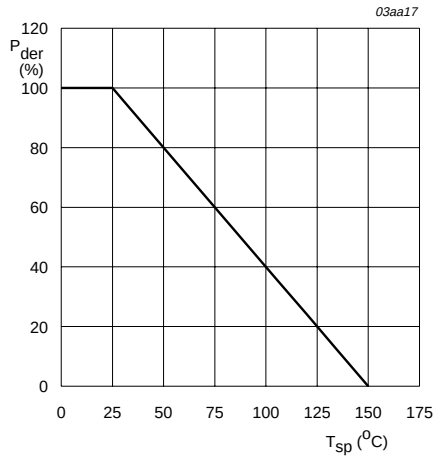
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to $150\text{ }^{\circ}\text{C}$	–	100	V
V_{GS}	gate-source voltage (DC)		–	± 20	V
I_D	drain current (DC)	$T_{sp} = 80\text{ }^{\circ}\text{C}$	–	6.3	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	50	A
P_{tot}	total power dissipation	$T_{sp} = 80\text{ }^{\circ}\text{C}$	–	3.5	W
T_{stg}	storage temperature		–55	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–55	+150	$^{\circ}\text{C}$

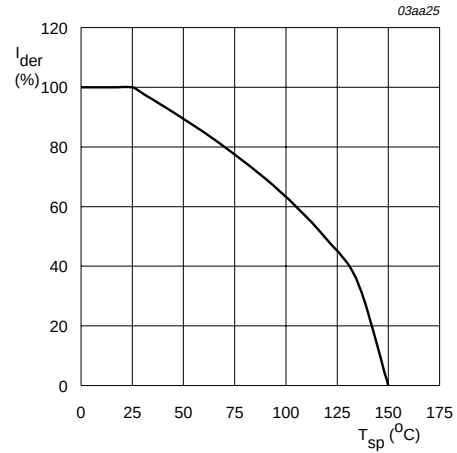
Source-drain diode

I_S	source (diode forward) current (DC)	$T_{sp} = 80\text{ }^{\circ}\text{C}$	–	3.1	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	–	50	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

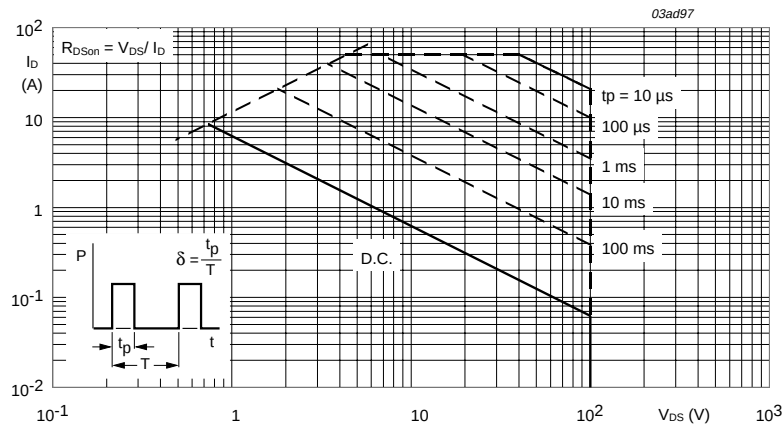
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$V_{GS} \geq 5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}\text{C}$; I_{DM} is single pulse

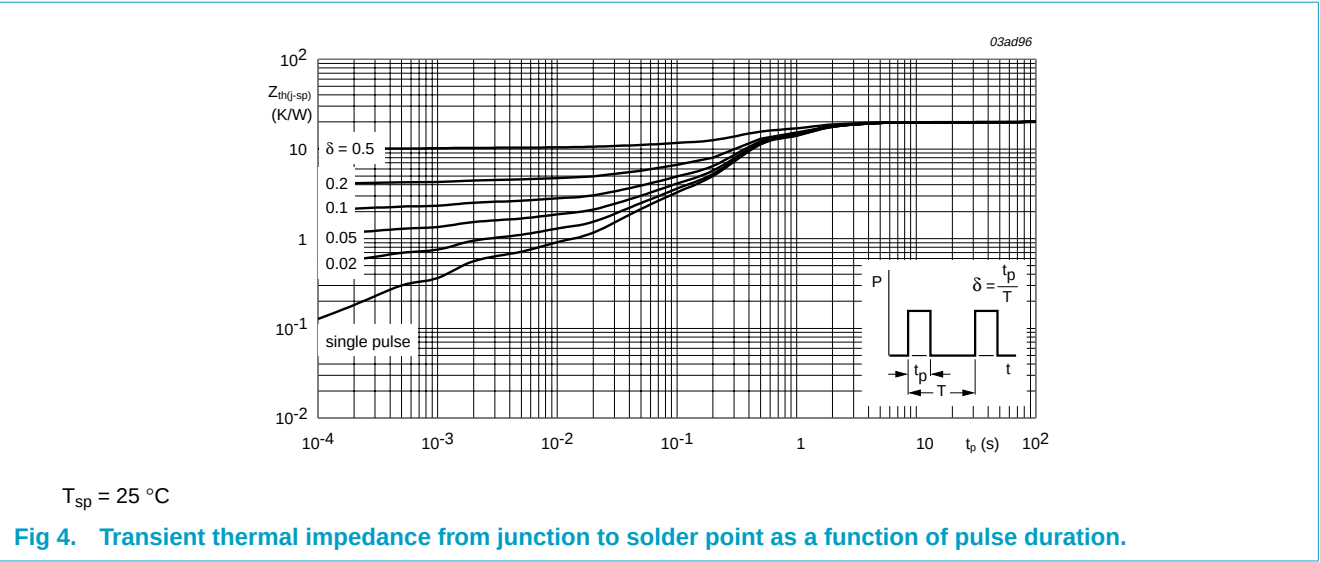
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; Figure 4	20	K/W

7.1 Transient thermal impedance

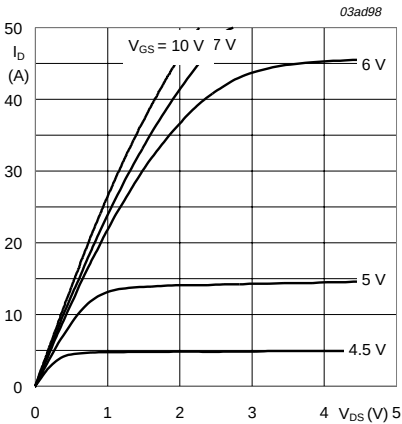


8. Characteristics

Table 5: Characteristics

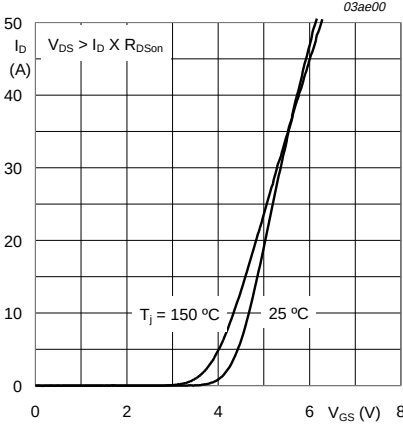
$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	100	130	–	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9				
		T _j = 25 °C	2	–	4	V
		T _j = 150 °C	1.2	–	–	V
		T _j = –55 °C	–	–	6	V
I _{DSS}	drain-source leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C	–	–	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 150 °C	–	–	0.5	mA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	–	–	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 5.2 A; Figure 7 and 8				
		T _j = 25 °C	–	33	38	mΩ
		T _j = 150 °C	–	76	88	mΩ
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 15 V; I _D = 6.3 A; Figure 11	–	20	–	S
Q _{g(tot)}	total gate charge	I _D = 6.3 A; V _{DD} = 50 V; V _{GS} = 10 V; Figure 14	–	43	–	nC
Q _{gs}	gate-source charge		–	6.5	–	nC
Q _{gd}	gate-drain (Miller) charge		–	16	21.5	nC
C _{iss}	input capacitance		V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 12	–	1740	–
C _{oss}	output capacitance	–		220	–	pF
C _{rss}	reverse transfer capacitance	–		135	–	pF
t _{d(on)}	turn-on delay time	V _{DD} = 50 V; I _D = 1 A; V _{GS} = 10 V; R _G = 6 Ω	–	15	30	ns
t _r	rise time		–	13	25	ns
t _{d(off)}	turn-off delay time		–	50	80	ns
t _f	fall time		–	25	40	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 2.3 A; V _{GS} = 0 V; Figure 13	–	0.7	1.1	V
t _{rr}	reverse recovery time	I _S = 6.3 A; dI _S /dt = –100 A/μs; V _{GS} = 0 V	–	85	–	ns
Q _r	recovery charge		–	0.3	–	μC



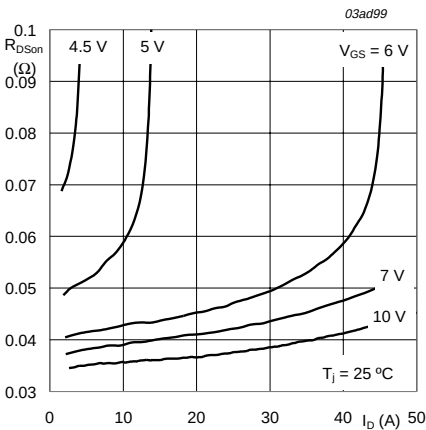
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



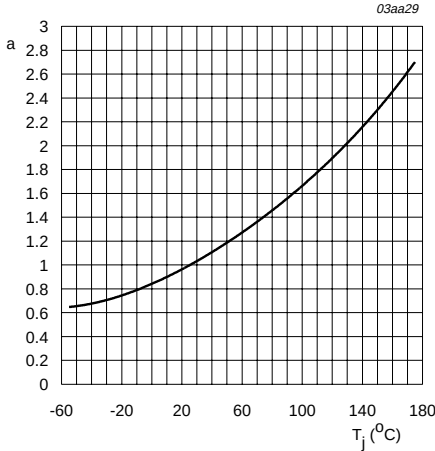
T_j = 25 °C and 150 °C; V_{DS} > I_D × R_{DS(on)}

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



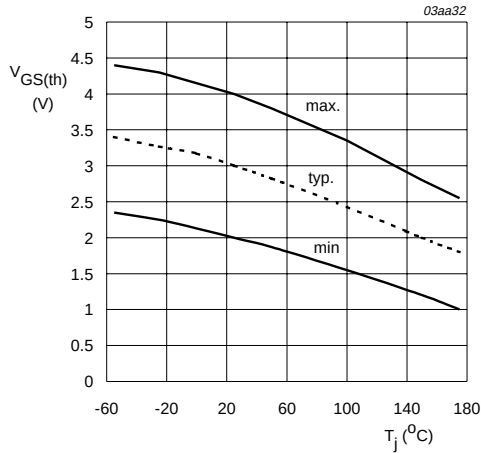
T_j = 25 °C

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



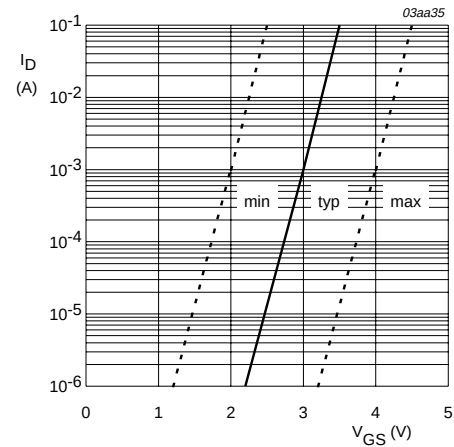
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^{\circ}C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



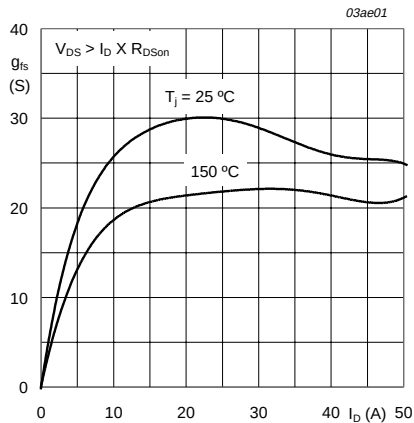
$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



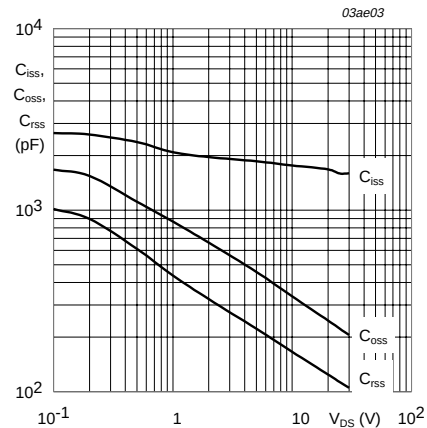
$T_j = 25 \text{ }^{\circ}C$; $V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



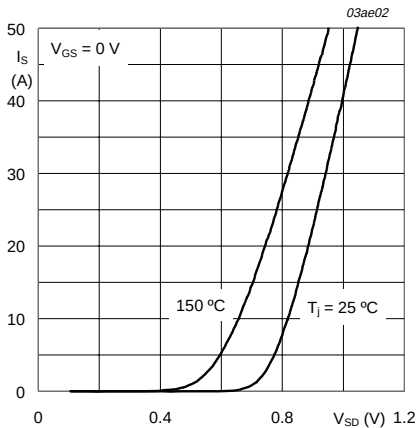
$T_j = 25 \text{ }^{\circ}C$ and $150 \text{ }^{\circ}C$; $V_{DS} > I_D \times R_{DS(on)}$

Fig 11. Forward transconductance as a function of drain current; typical values.



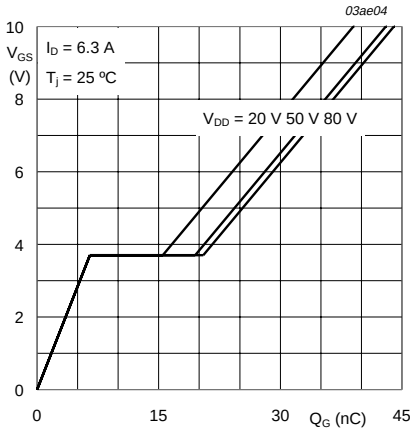
$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_J = 25\text{ °C}$ and 150 °C ; $V_{GS} = 0\text{ V}$

Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 6.3\text{ A}$; $V_{DD} = 20\text{ V}, 50\text{ V}$ and 80 V

Fig 14. Gate-source voltage as a function of gate charge; typical values.

9. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

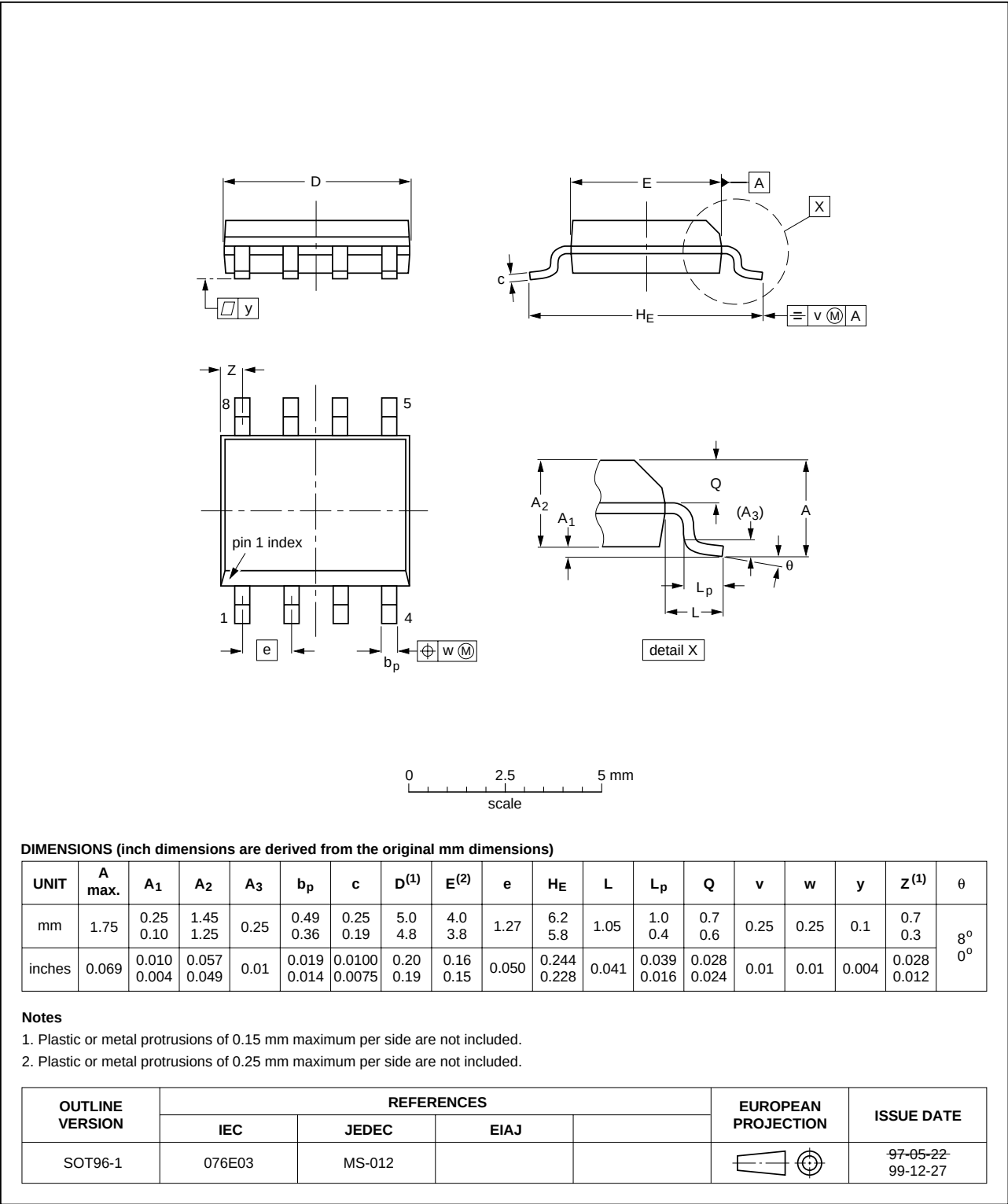


Fig 15. SOT96-1 (SO8).

10. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
01	20010116	-	Product specification; initial version

11. Data sheet status

Datasheet status	Product status	Definition ^[1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

12. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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