



PSMN1R5-40PS

N-channel 40 V 1.6 m Ω standard level MOSFET in TO220

15 July 2013

Product data sheet

1. General description

Standard level N-channel MOSFET in SOT78 (TO220) using TrenchMOS technology. Product design and manufacture has been optimized for use in battery operated power tools.

2. Features and benefits

- High efficiency due to low switching and conduction losses
- Robust construction for demanding applications
- Standard level gate

3. Applications

- Battery-powered tools
- Load switching
- Motor control
- Uninterruptible power supplies

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^\circ\text{C}$; $T_j \leq 175\text{ }^\circ\text{C}$		-	-	40	V
I_D	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1	[1]	-	-	150	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2		-	-	338	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 100\text{ }^\circ\text{C}$; Fig. 13		-	1.9	2.3	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 14	[2]	-	1.3	1.6	m Ω
Dynamic characteristics							
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 75\text{ A}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15 ; Fig. 16		-	32	-	nC
$Q_{G(tot)}$	total gate charge			-	136	-	nC



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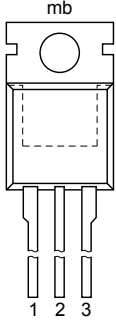
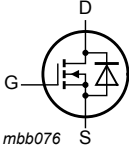


Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 150\text{ A}$; $V_{\text{sup}} \leq 40\text{ V}$; unclamped; $R_{GS} = 50\text{ }\Omega$; $t_p = 0.1\text{ ms}$; Fig. 3	-	-	1.1	J

- [1] Continuous current is limited by package
- [2] Measured 3 mm from package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p style="text-align: center;">TO-220AB (SOT78)</p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	D	drain		
3	S	source		
mb	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN1R5-40PS	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R5-40PS	PSMN1R5-40PS

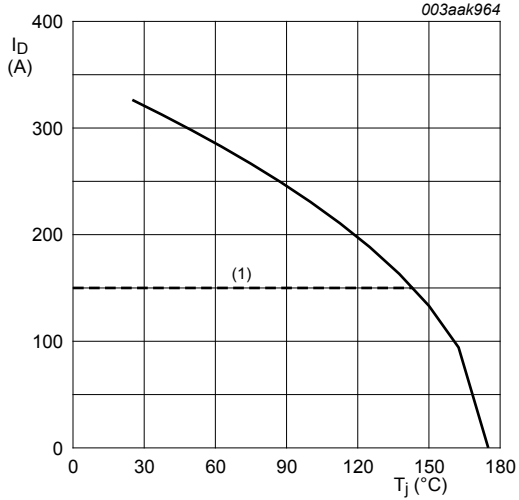
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$		-	40	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}; \text{Fig. 1}$	[1]	-	150	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	[1]	-	150	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}; \text{Fig. 4}$		-	1301	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$		-	338	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	150	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$		-	1301	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 150\text{ A}; V_{sup} \leq 40\text{ V}; \text{unclamped}; R_{GS} = 50\text{ }\Omega; t_p = 0.1\text{ ms}; \text{Fig. 3}$		-	1.1	J

[1] Continuous current is limited by package



(1) Capped at 150A due to package

Fig. 1. Normalized continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

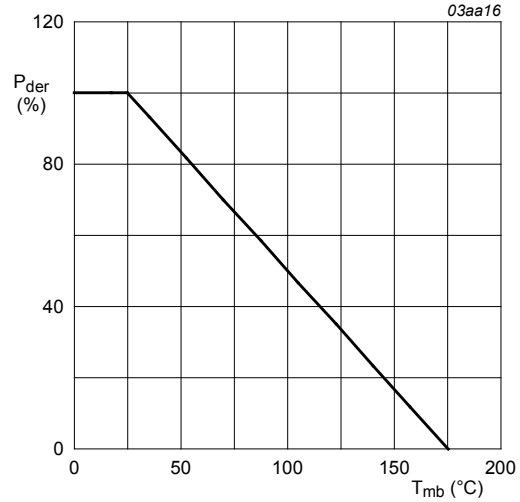


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

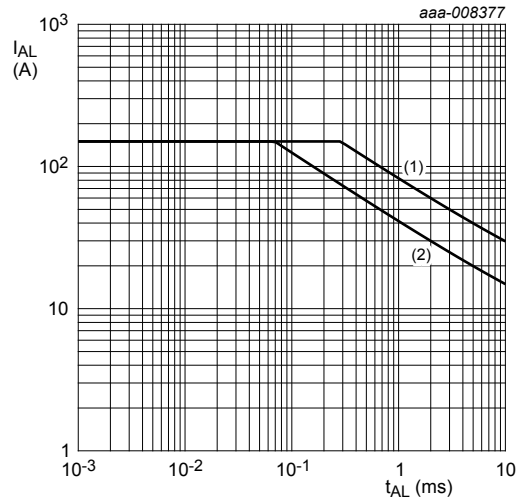
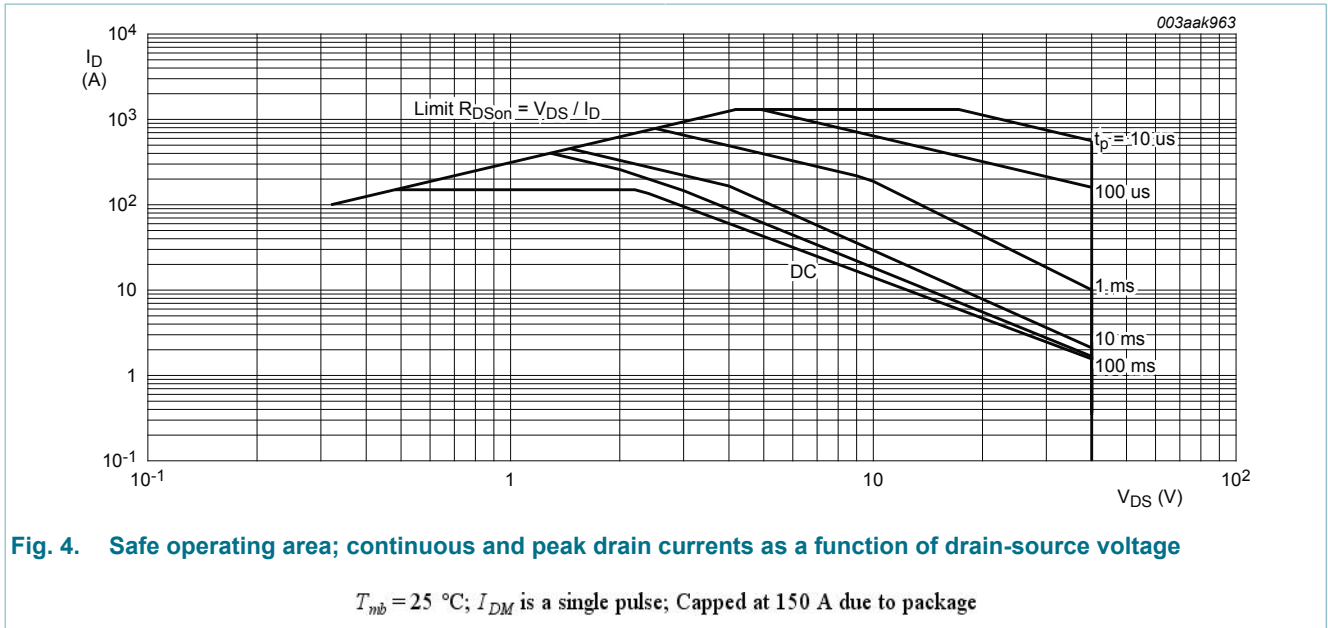


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

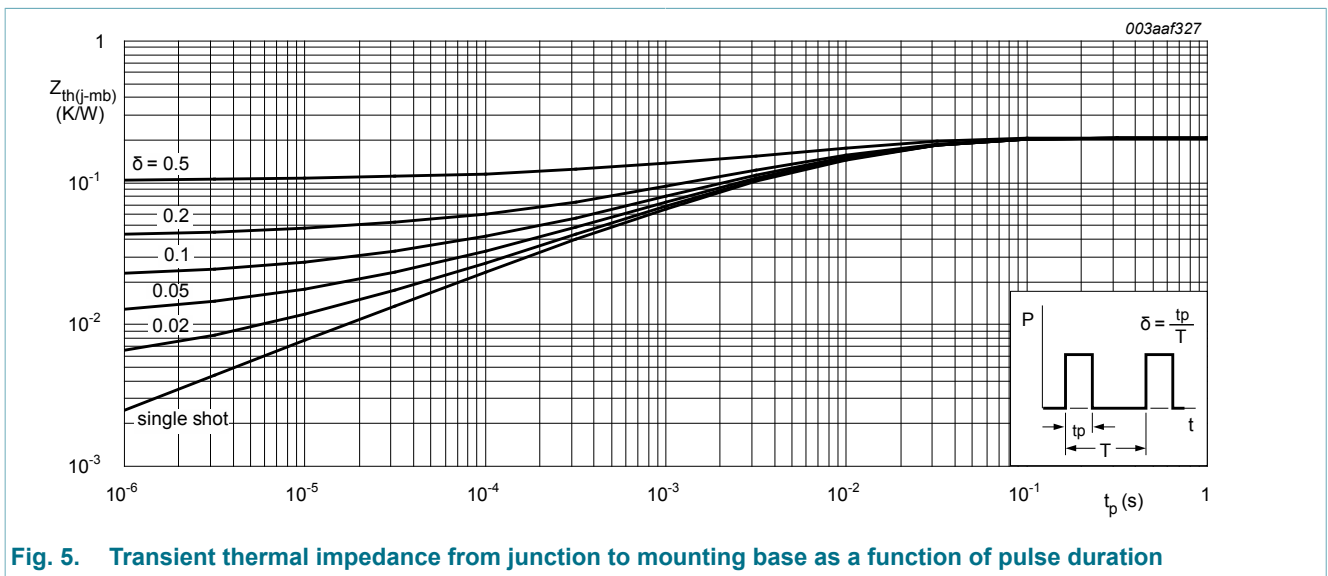
(1) $T_{j(int)} = 25^{\circ}C$; (2) $T_{j(int)} = 100^{\circ}C$



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.22	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Vertical in free air	-	60	-	K/W



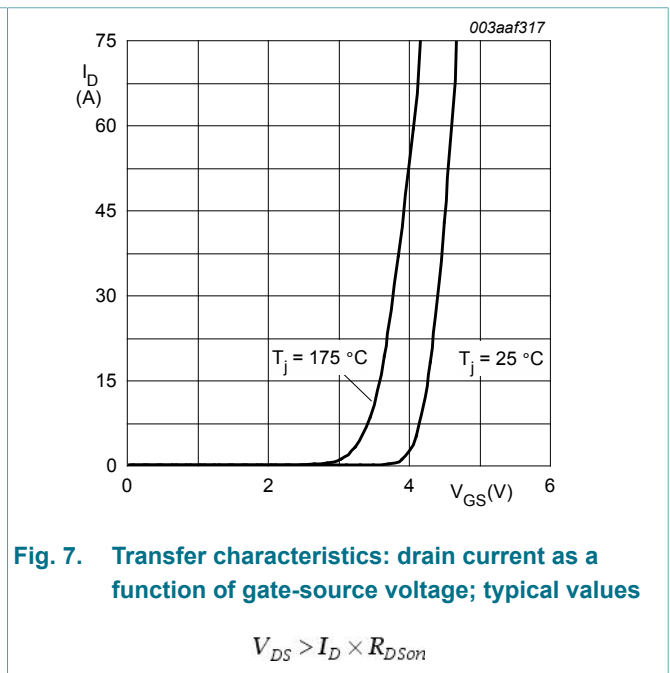
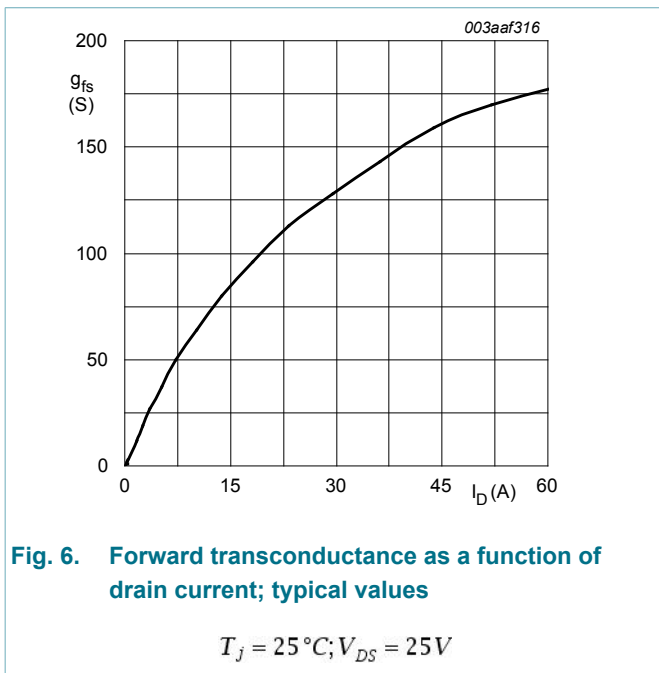
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 11	-	-	4.6	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 11	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 12; Fig. 11	2	3	4	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	10	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	250	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 100 \text{ }^\circ C;$ Fig. 13	-	1.9	2.3	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175 \text{ }^\circ C;$ Fig. 13	-	2.6	3.2	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ Fig. 14	[1]	-	1.3	1.6
R_G	internal gate resistance (AC)	$f = 1 \text{ MHz}$	-	1.1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	133	-	nC
		$I_D = 75 A; V_{DS} = 20 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C;$ Fig. 15; Fig. 16	-	136	-	nC
Q_{GS}	gate-source charge		-	52	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	30	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	22.5	-	nC
Q_{GD}	gate-drain charge		-	32	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		$I_D = 75 A; V_{DS} = 20 V; T_j = 25 \text{ }^\circ C;$ Fig. 15; Fig. 16	-	6.1	-
C_{iss}	input capacitance	$V_{DS} = 20 V; V_{GS} = 0 V; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ C;$ Fig. 17	-	9710	-	pF
C_{oss}	output capacitance		-	2042	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rSS}	reverse transfer capacitance		-	994	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20\text{ V}; R_L = 0.8\ \Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 4.7\ \Omega; T_j = 25\text{ }^\circ\text{C}$	-	45	-	ns
t_r	rise time		-	66	-	ns
$t_{d(off)}$	turn-off delay time		-	111	-	ns
t_f	fall time		-	53	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 18}$	-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	64	-	ns
Q_r	recovered charge	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	117	-	nC

[1] Measured 3 mm from package.



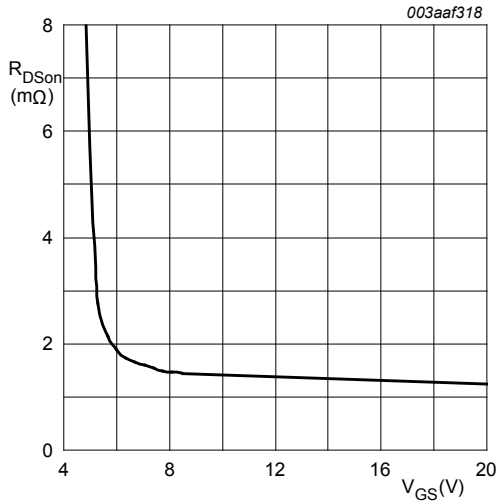


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values.

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

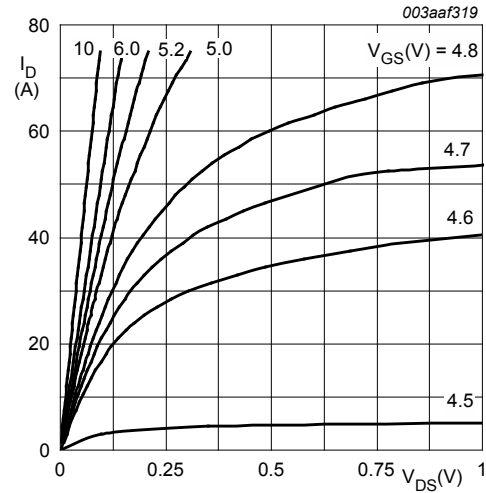


Fig. 9. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}$

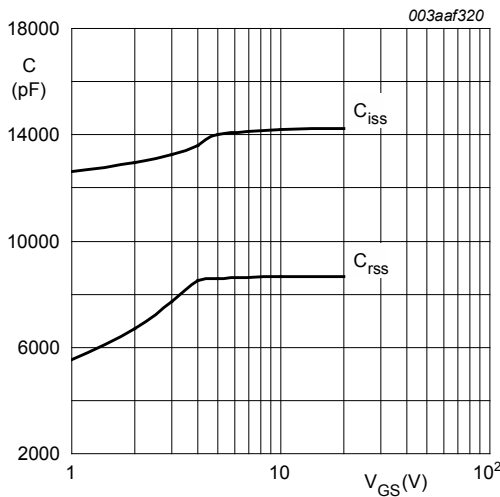


Fig. 10. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$

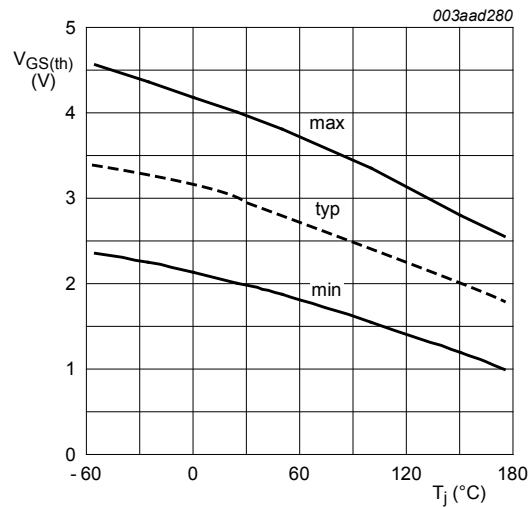


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

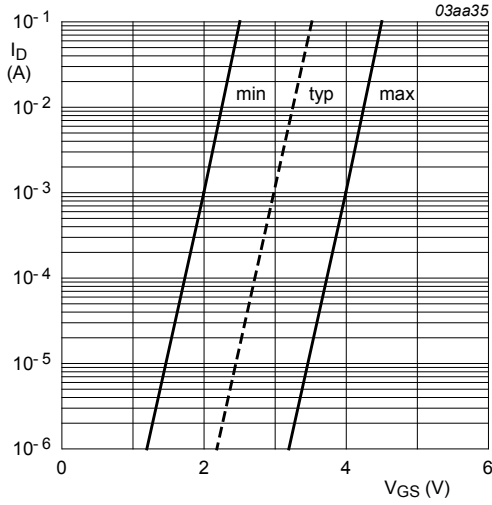


Fig. 12. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

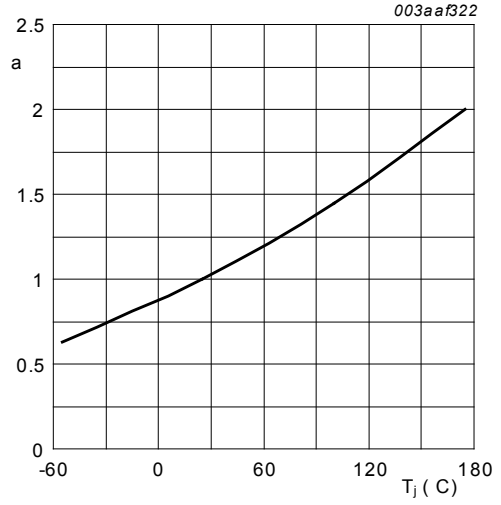


Fig. 13. Normalized drain-source on state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

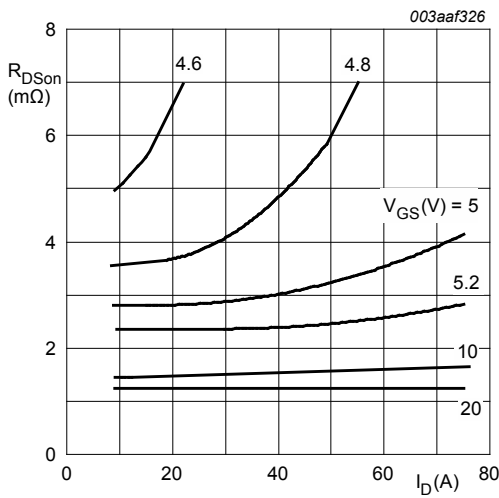


Fig. 14. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

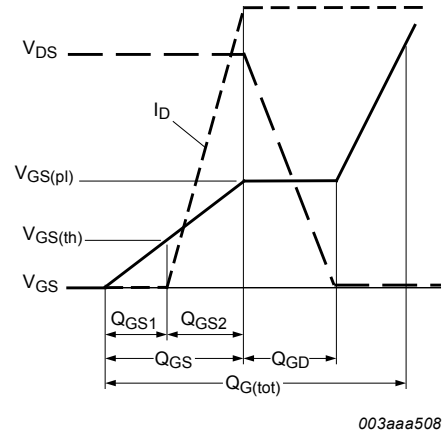


Fig. 15. Gate charge waveform definitions

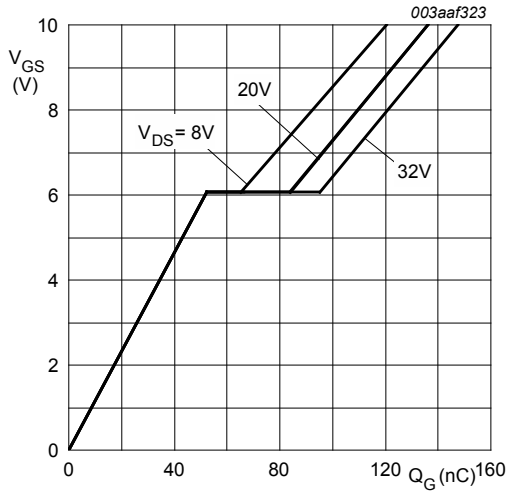


Fig. 16. Gate-source voltage as a function of gate charge; typical values

$$I_D = 75 A$$

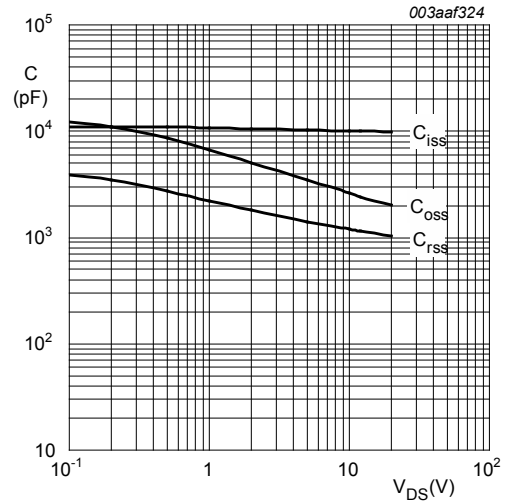


Fig. 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

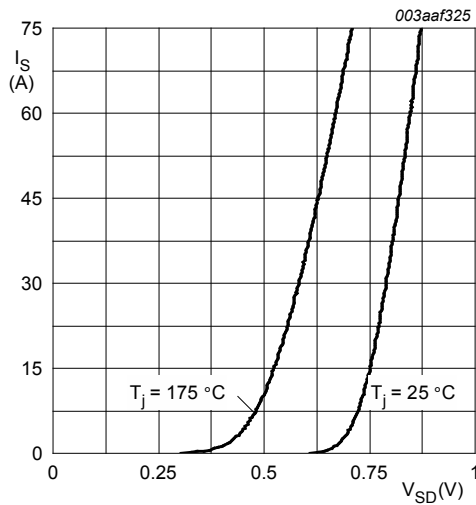


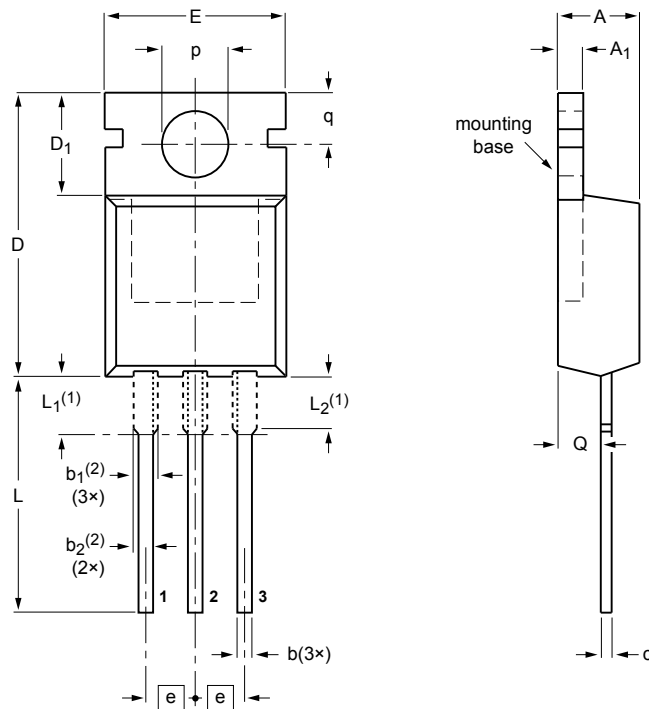
Fig. 18. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	b ₁ (2)	b ₂ (2)	c	D	D ₁	E	e	L	L ₁ (1)	L ₂ (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

- Lead shoulder designs may vary.
- Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig. 19. Package outline TO-220AB (SOT78)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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