PSMN1R6-40YLC

N-channel 40 V 1.55 mΩ logic level MOSFET in LFPAK using NextPower technology

22 August 2012 Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High reliability Power SO8 package, qualified to 150°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads
- Ultra low Rdson and low parasitic inductance

1.3 Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	-	40	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; Fig. 1	[1]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	-	288	W
T_j	junction temperature			-55	-	150	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.45	1.8	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.25	1.55	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 20 V; Fig. 14		-	15.3	-	nC

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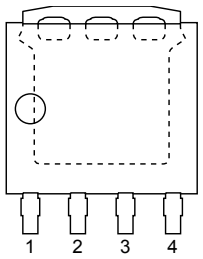
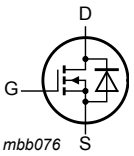
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	V_{GS} = 4.5 V; I_D = 25 A; V_{DS} = 20 V; Fig. 14		-	59	-	nC

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK; Power-SO8 (SOT1023)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R6-40YLC	LFPAK; Power-SO8	Plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT1023

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C		-	40	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 1	[1]	-	100	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 1	[1]	-	100	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 4		-	1304	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 2		-	288	W
T_{stg}	storage temperature			-55	150	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		1	-	kV
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10$ µs; T_{mb} = 25 °C		-	1304	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 100 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; unclamped; Fig. 3		-	391	mJ

[1] Continuous current is limited by package.

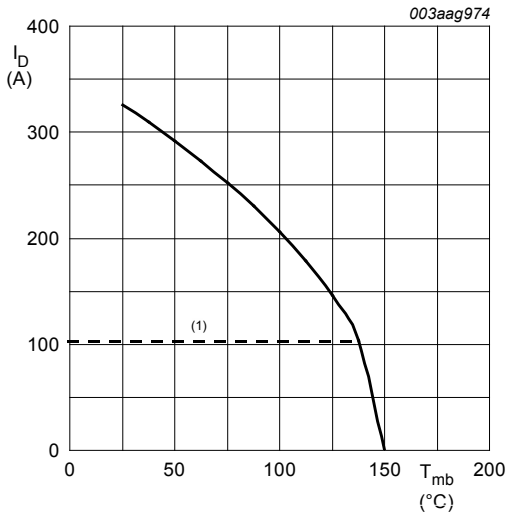


Fig. 1. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10\,V$

(1) Capped at 100 A due to package.

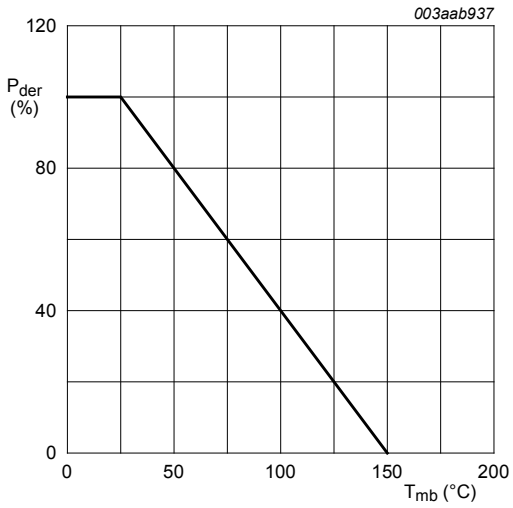


Fig. 2. Normalized total power dissipation as a function of solder point temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

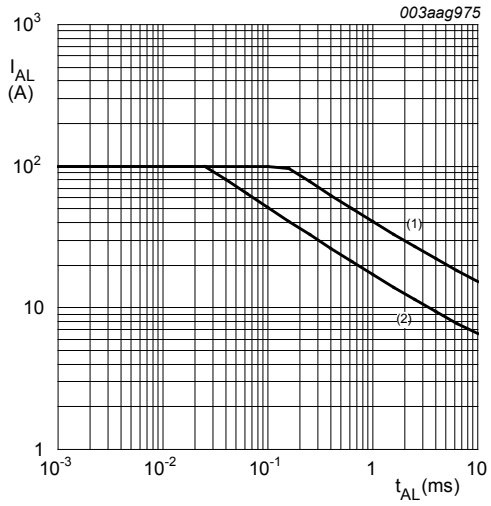


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25°C$; (2) $T_{j\ (init)} = 100°C$

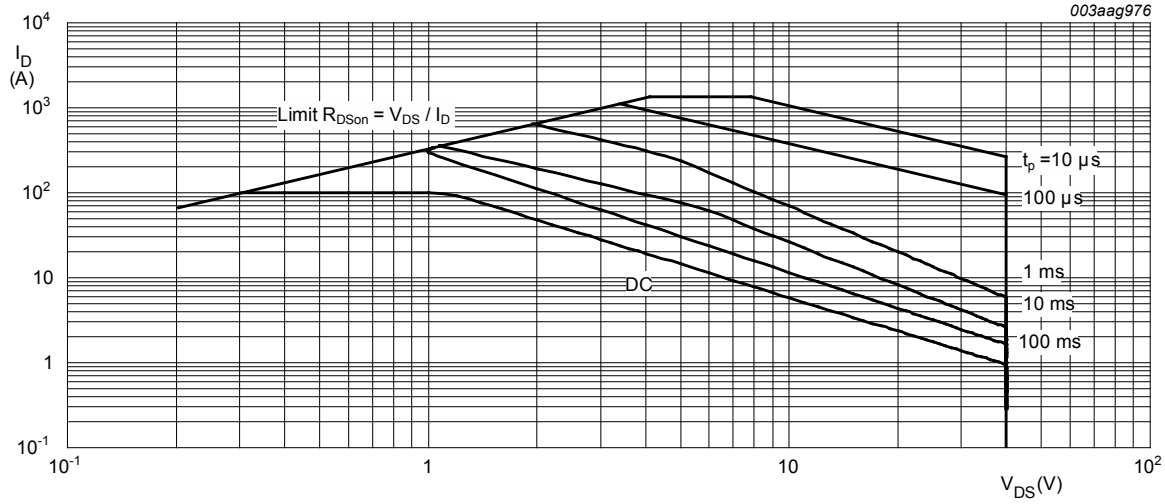


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25°C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.35	0.43	K/W

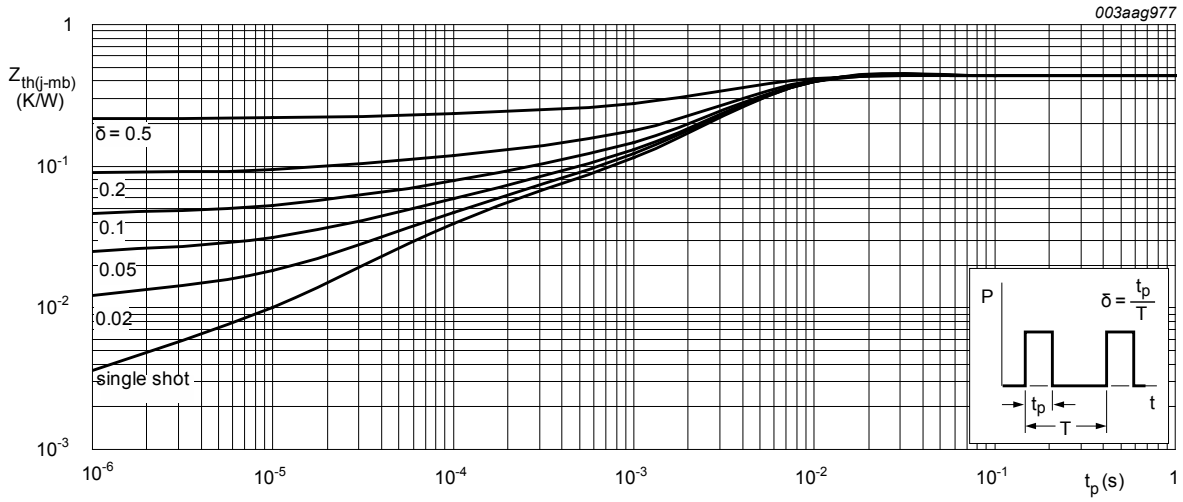


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		1.05	1.46	1.95	V
		I_D = 10 mA; V_{DS} = V_{GS}; T_j = 150 °C		0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C		-	-	2.25	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 150 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.45	1.8	mΩ
		V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 °C; Fig. 12; Fig. 13		-	-	3.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	1.25	1.55	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 150 °C; Fig. 12; Fig. 13		-	-	2.7	mΩ
R_G	gate resistance	f = 1 MHz		-	1.17	2.34	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	126	-	nC
		I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 14		-	59	-	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	115	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V; Fig. 14		-	17.7	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	12.5	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	5.2	-	nC
Q_{GD}	gate-drain charge			-	15.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 20 V; Fig. 14		-	2.4	-	V
C_{iss}	input capacitance	V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	7790	-	pF
C_{oss}	output capacitance			-	1063	-	pF
C_{rss}	reverse transfer capacitance			-	409	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 0.8 Ω; V_{GS} = 4.5 V; $R_{G(ext)}$ = 4.7 Ω		-	41	-	ns
t_r	rise time			-	48	-	ns
$t_{d(off)}$	turn-off delay time			-	86	-	ns
t_f	fall time			-	42	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz; T_j = 25 °C		-	38.7	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.77	1.1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 18		-	44	-	ns
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V		-	62	-	nC
t_a	reverse recovery rise time	V_{GS} = 0 V; I_S = 25 A; dI_S/dt = -100 A/µs; V_{DS} = 20 V; Fig. 18		-	26	-	ns
t_b	reverse recovery fall time			-	18	-	ns

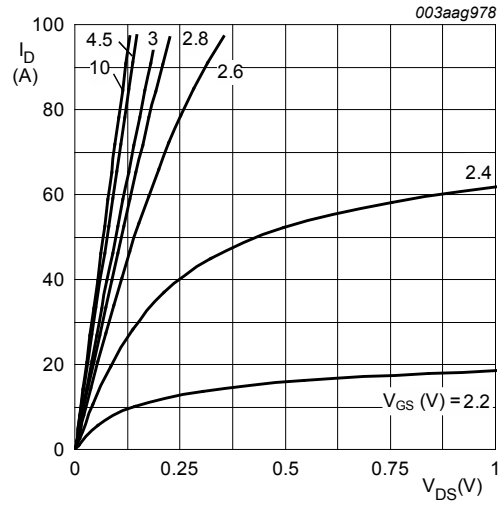


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25°C$

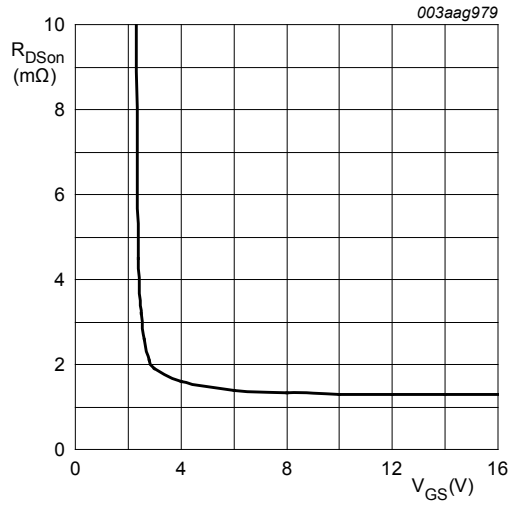


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25°C;\ I_D = 25A$

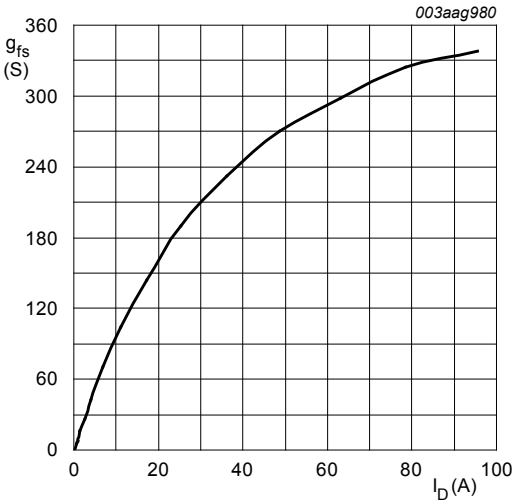


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25°C;\ V_{DS} = 10V$

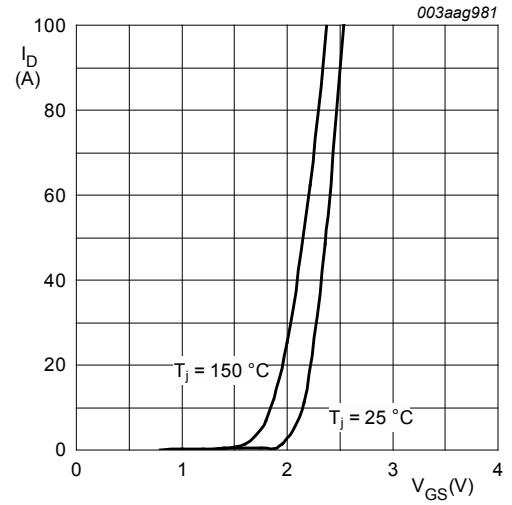


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

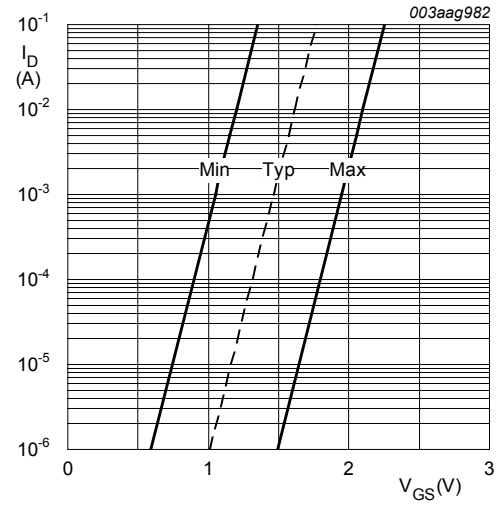


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25°C;\ V_{DS} = 5V$

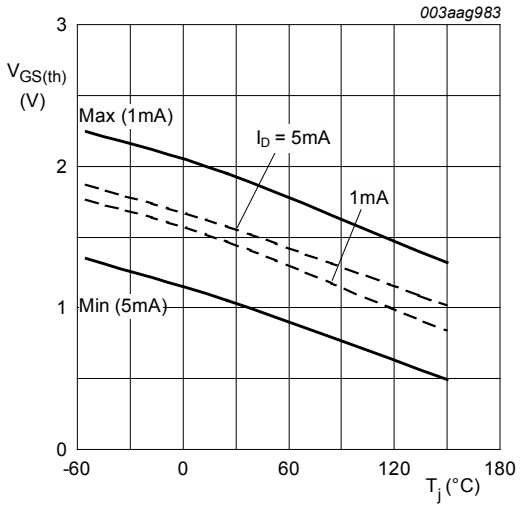


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$V_{DS} = V_{GS}$

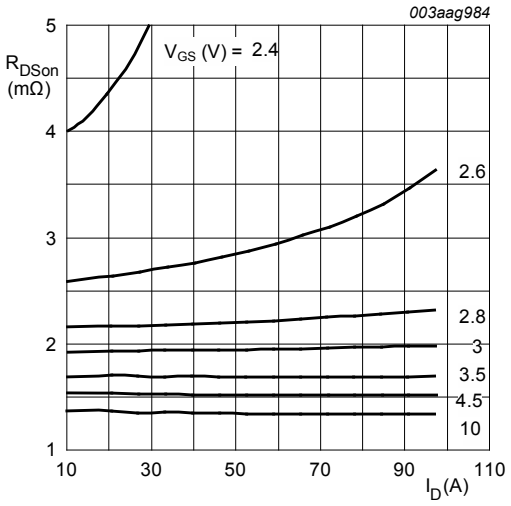


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25°C$

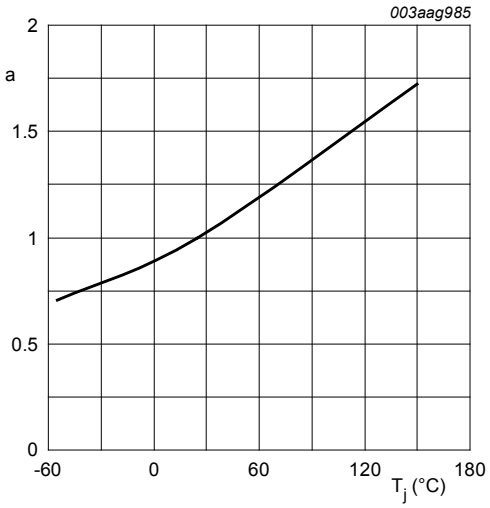


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$a = \frac{R_{DSon}}{R_{DSon\ (25°C)}};\ V_{GS} \leq 10V$

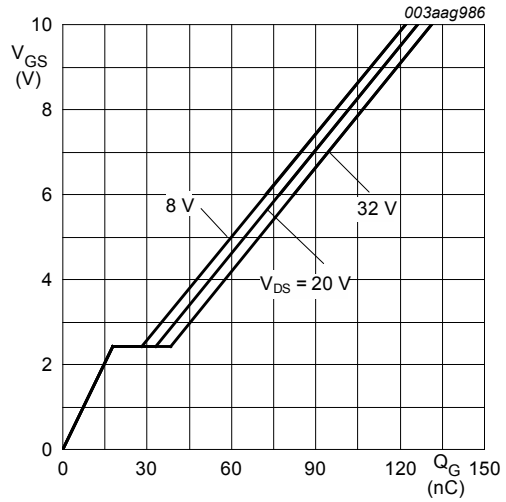


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$T_j = 25°C;\ I_D = 25A$

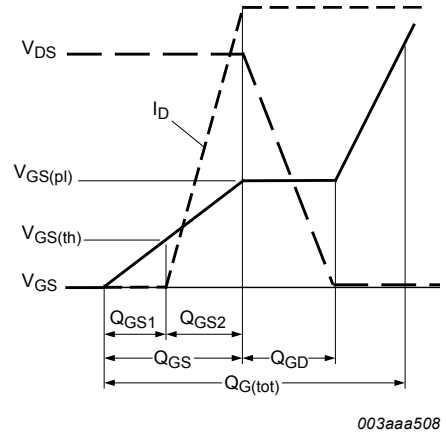


Fig. 15. Gate charge waveform definitions

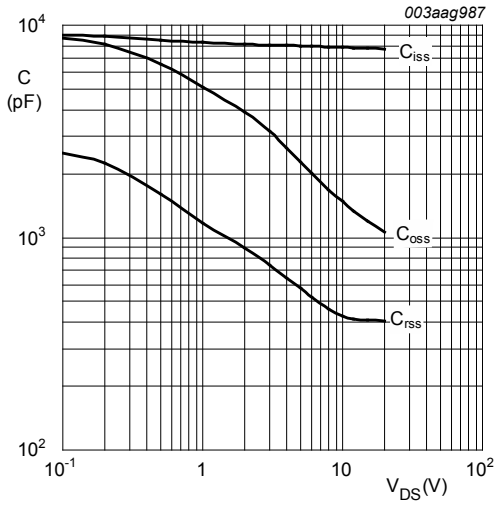


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V;\ f = 1MHz$

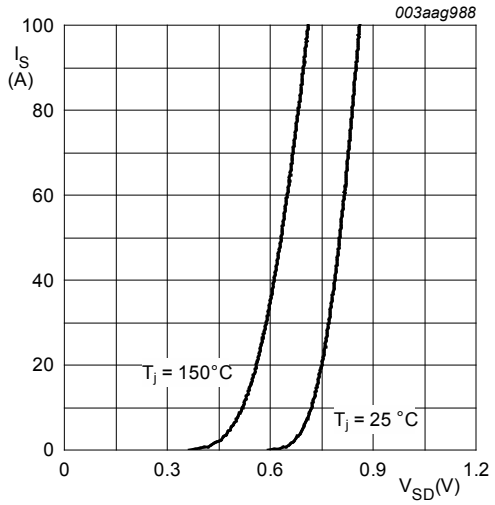


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

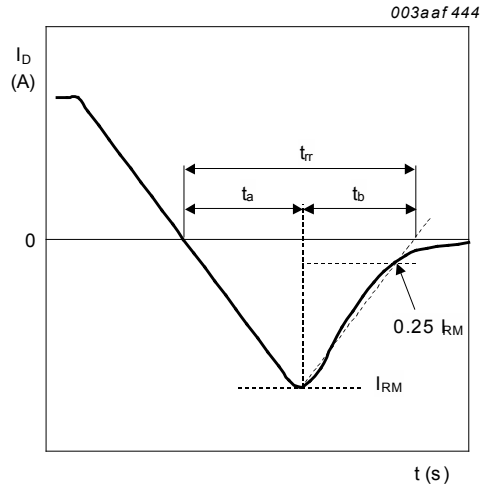
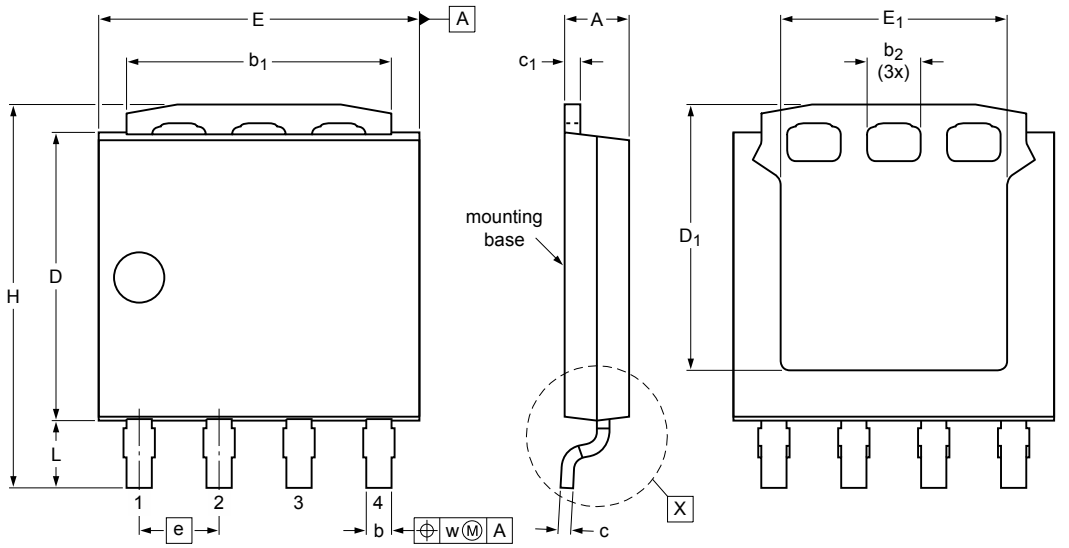


Fig. 18. Reverse recovery timing definition

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT1023**



Dimensions

Unit		A	A_1	b	b_1	b_2	c	c_1	$D^{(1)}$	$D_1{}^{(1)}$	$E^{(1)}$	$E_1{}^{(1)}$	e	H	L	L_p	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~09-05-26~~ 11-12-09

Fig. 19. Package outline LFPAK; Power-SO8 (SOT1023)

8. Legal information

8.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 22 August 2012