PSMN1R9-40YSD

40 V standard level MOSFET

17 June 2019 **Preliminary data sheet**

1. General description

Standard level gate drive N-channel enhancement mode MOSFET.

2. Quick reference data

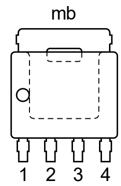
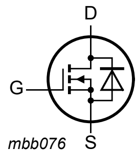
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	120	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	194	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 8		-	1.6	1.9	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 10; Fig. 11		-	8.2	16	nC
$Q_{G(tot)}$	total gate charge			-	57	80	nC

[1] 120A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

3. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 **LFPAK56; Power-SO8 (SOT669)**	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

4. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R9-40YSD	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

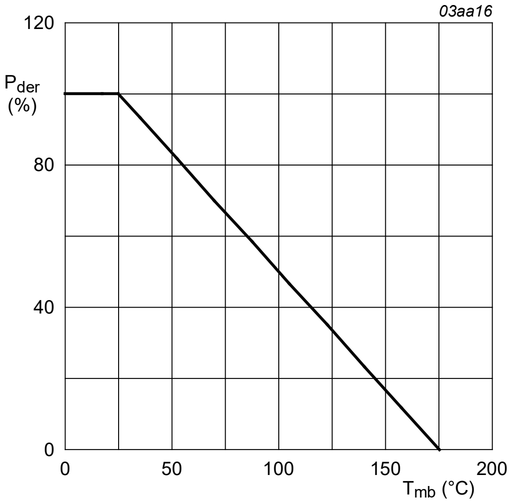
5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

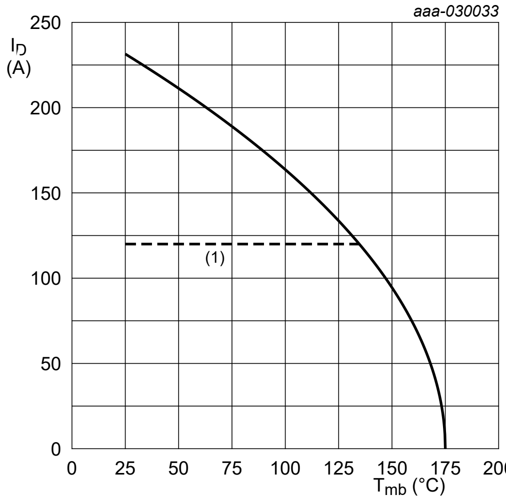
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{DSM}	peak drain-source voltage	t_p ≤ 20 ns; f ≤ 500 kHz; $E_{DS(AL)}$ ≤ 200 nJ; pulsed		-	45	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage	T_j ≤ 175 °C		-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	194	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	120	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	120	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	926	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	120	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	926	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 60.8 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 202 µs	[2]	-	319	mJ
		I_D = 25 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 1.4 ms	[2]	-	905	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[2]	-	126	A

[1] 120A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



$V_{GS} \geq 10$ V

(1) 120A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 3		-	0.69	0.77	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 4		-	42	-	K/W
		Fig. 5		-	85	-	K/W

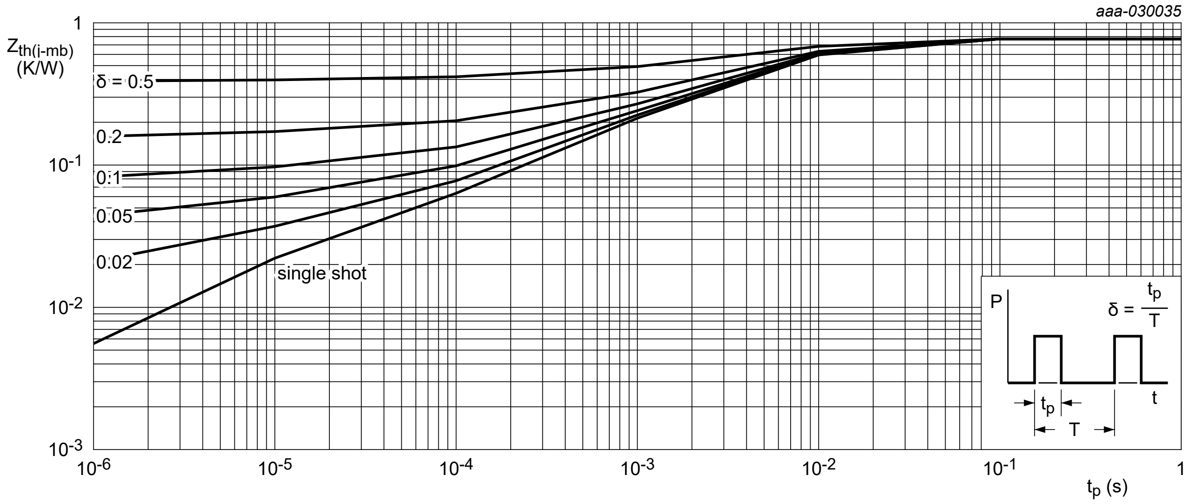
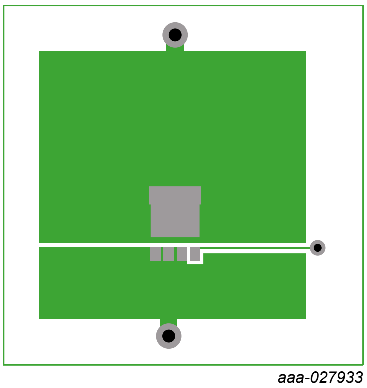
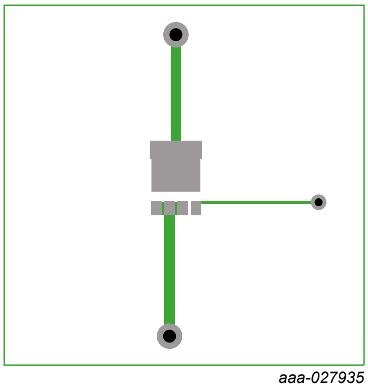


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration



Copper area 25.4 mm square; 70 µm thick on FR4 board

Fig. 4. PCB layout for thermal resistance from junction to ambient



70 µm thick copper on FR4 board

Fig. 5. PCB layout with minimum footprint for thermal resistance from junction to ambient

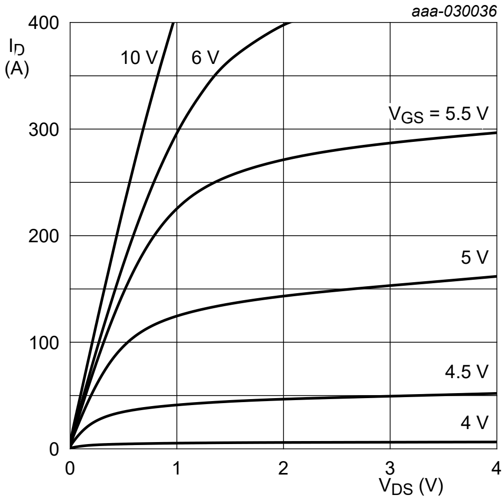
7. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2.4	3	3.6	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-6.3	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25 °C		-	0.01	1	µA
		V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125 °C		-	[tbd]	-	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 8		-	1.6	1.9	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 9		-	-	3.7	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.4	1	2.5	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 10; Fig. 11		-	57	80	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	[tbd]	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V; Fig. 10; Fig. 11		-	18	27	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	12	18	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	5.8	8.7	nC
Q_{GD}	gate-drain charge			-	8.2	16	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 20 V; Fig. 10; Fig. 11		-	4.4	-	V

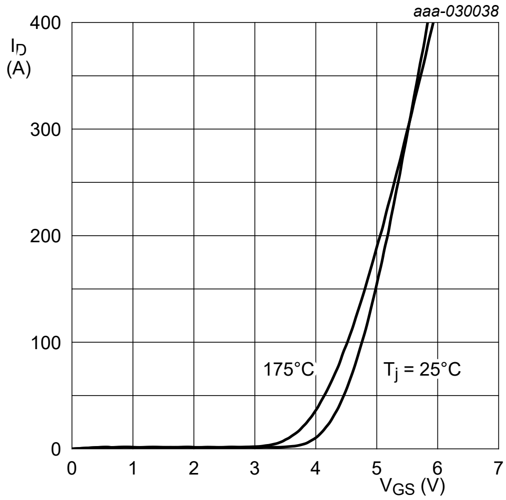
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{DS} = 20 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 12		-	4427	6198	pF
C_{oss}	output capacitance			-	1115	1561	pF
C_{rss}	reverse transfer capacitance			-	188	414	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 20 V; R_L = 0.86 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	15	-	ns
t_r	rise time			-	11	-	ns
$t_{d(off)}$	turn-off delay time			-	34	-	ns
t_f	fall time			-	13	-	ns
Q_{oss}	output charge	V_{GS} = 0 V; V_{DS} = 20 V; f = 1 MHz; T_j = 25 °C		-	37	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 13		-	33	-	ns
Q_r	recovered charge		[1]	-	27	-	nC
t_a	reverse recovery rise time			-	18	-	ns
t_b	reverse recovery fall time			-	15	-	ns

[1] includes capacitive recovery



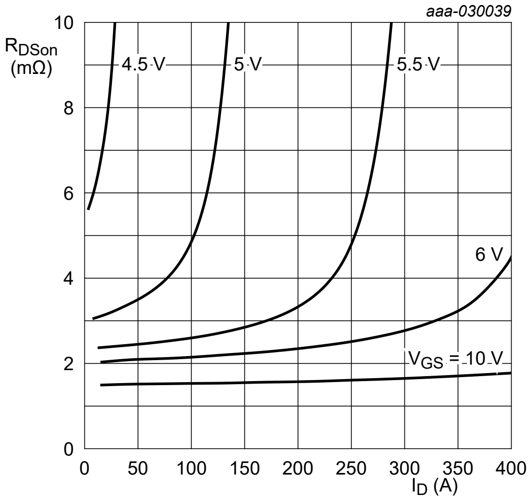
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



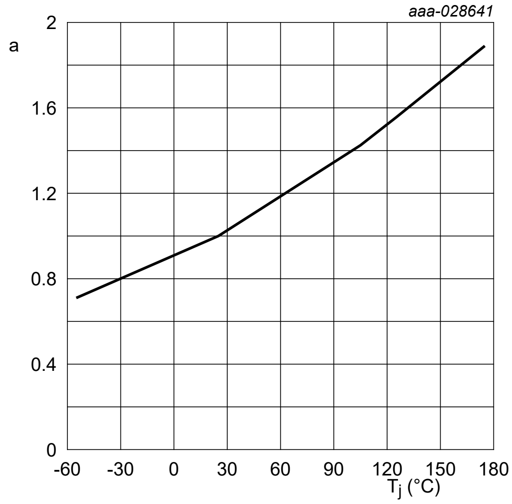
V_{DS} = 8 V

Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values



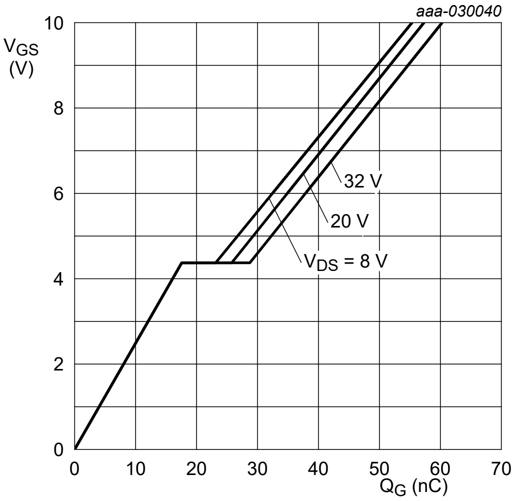
T_j = 25 °C

Fig. 8. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\,(25^{\circ}C)}}$$

Fig. 9. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 10. Gate-source voltage as a function of gate charge; typical values

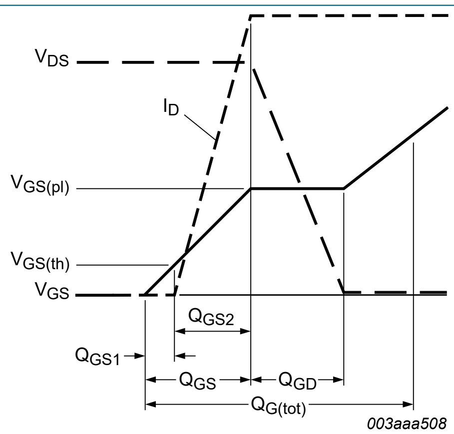
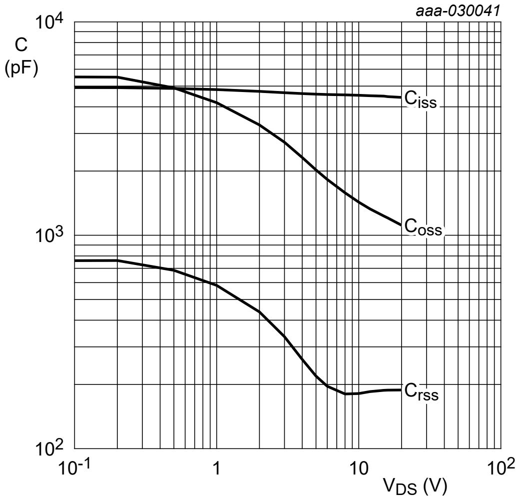


Fig. 11. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

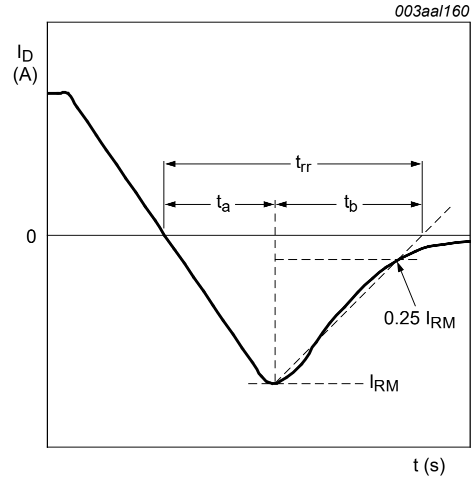
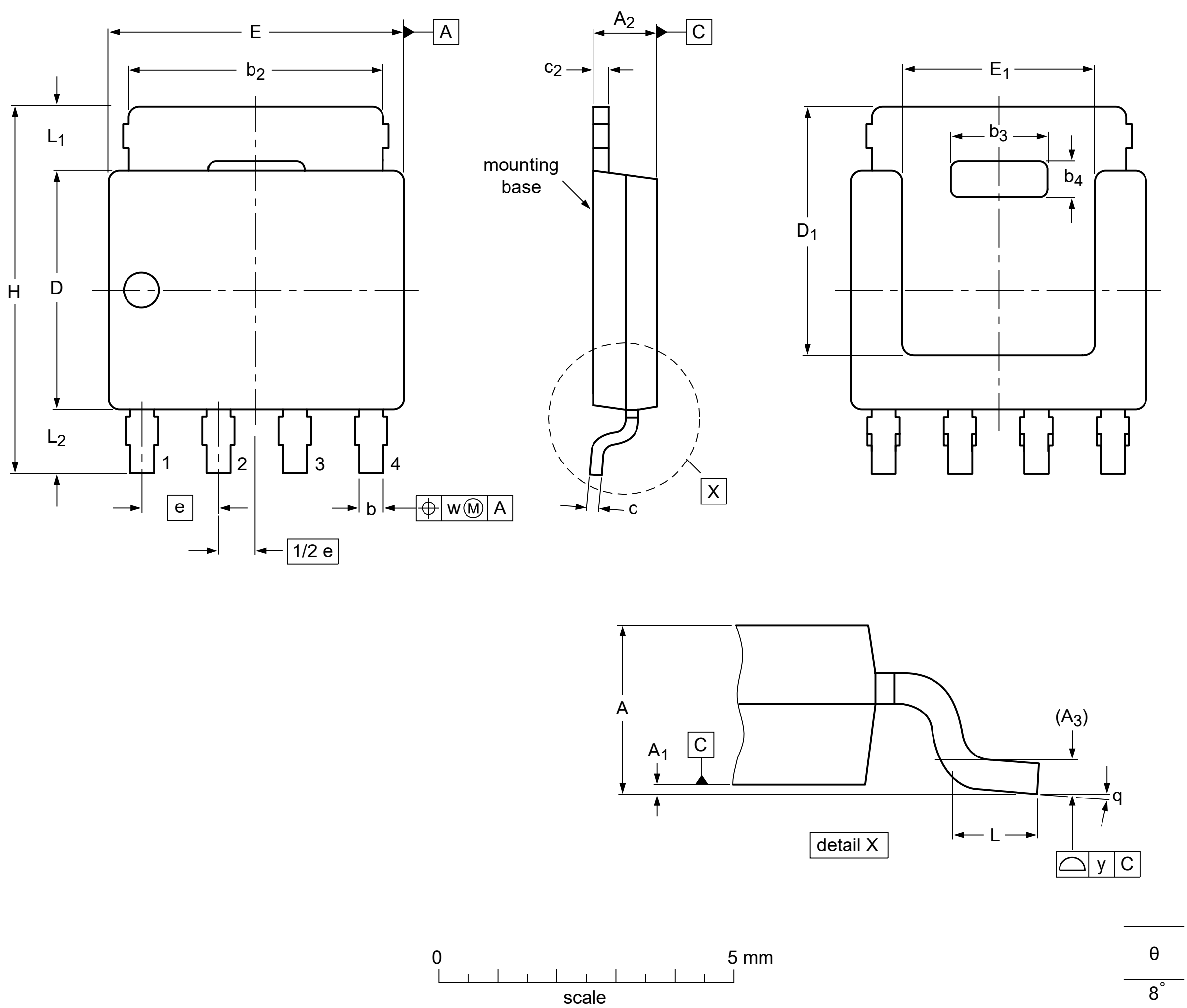


Fig. 13. Reverse recovery timing definition

8. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads **SOT669**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3			8°
	nom				0.25											1.27					0.25	0.1	
	min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8			0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~11-03-25~~ 13-02-27

Fig. 14. Package outline LFPAK56; Power-SO8 (SOT669)

9. Soldering

Footprint information for reflow soldering **SOT669**

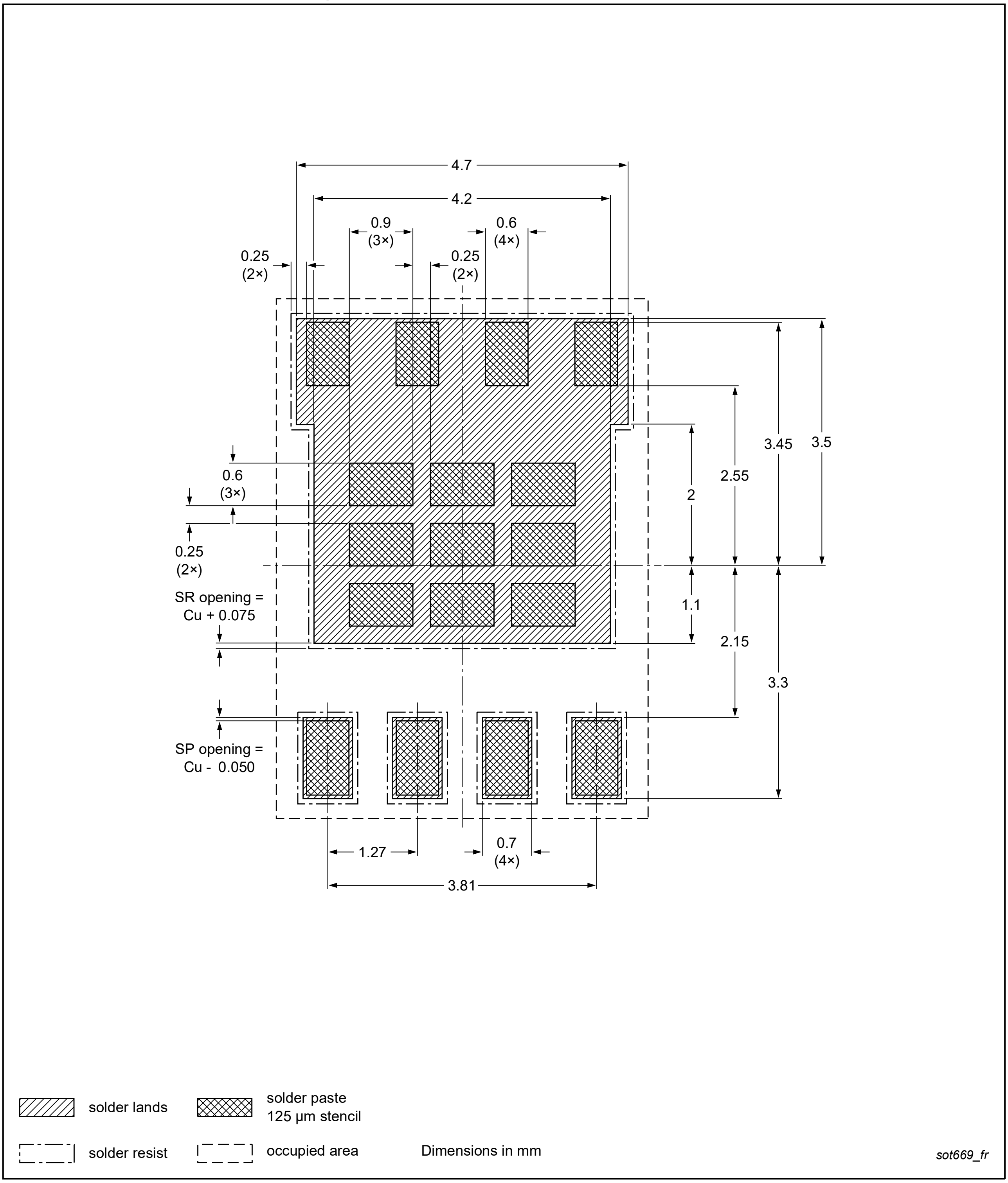


Fig. 15. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)

Wave soldering footprint information for LFPAK56 package **SOT669**

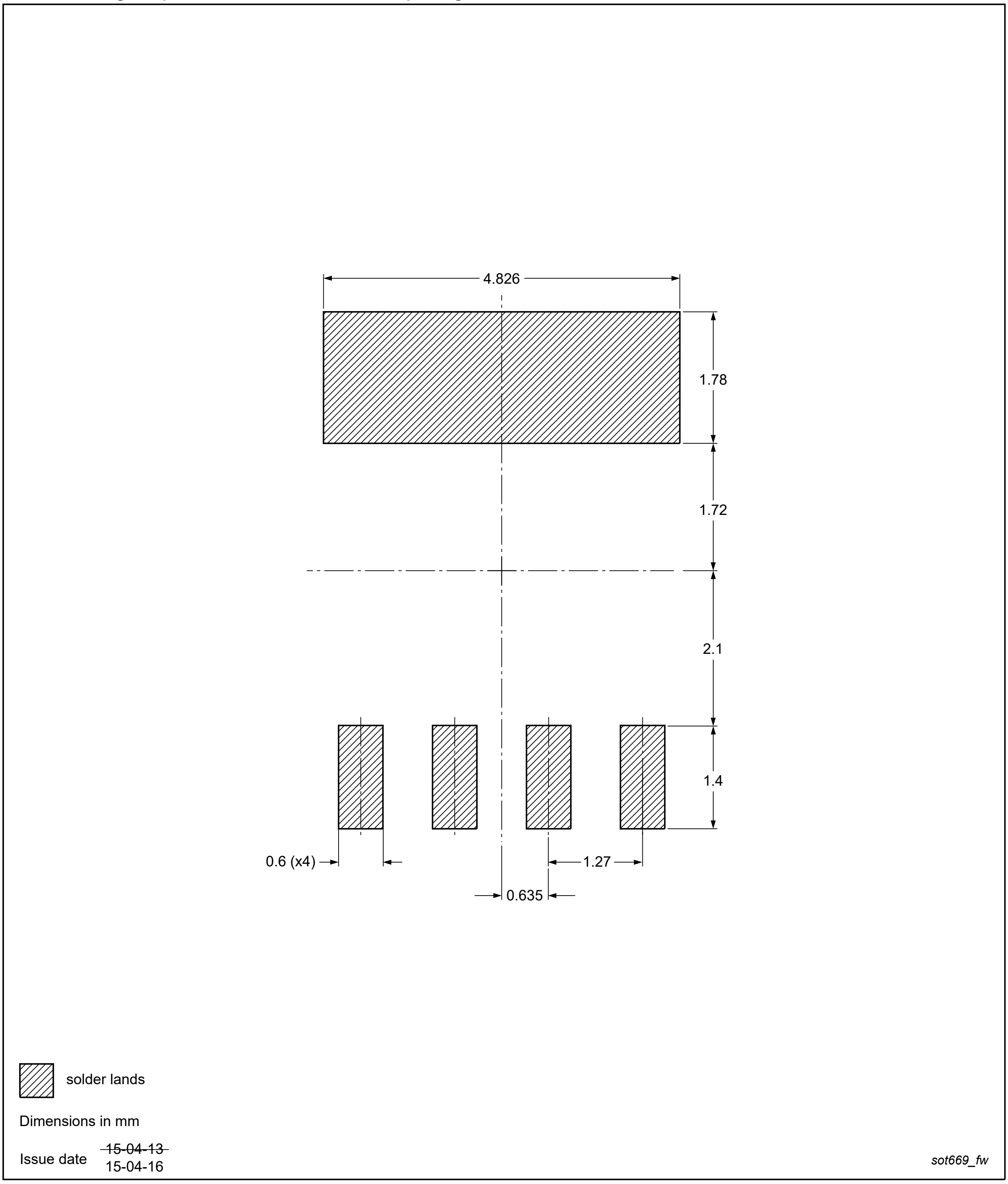


Fig. 16. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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