



# PSMN2R4-30YLD

N-channel 30 V, 2.4 mΩ logic level MOSFET in LPAK56 using NextPowerS3 Technology

7 February 2014

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LPAK56 package. NextPowerS3 portfolio utilising NXP's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

## 2. Features and benefits

- Ultra low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1μA leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

## 3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	25 °C ≤ $T_j$ ≤ 175 °C		-	-	30	V
$I_D$	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; <a href="#">Fig. 2</a>	[1]	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb}$ = 25 °C; <a href="#">Fig. 1</a>		-	-	106	W



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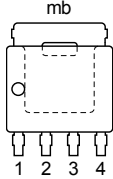
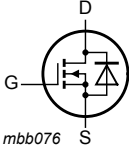
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NextPowerS3 Technology

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T <sub>j</sub>	junction temperature			-55	-	175	°C
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	2.7	3.1	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>		-	2	2.4	mΩ
Dynamic characteristics							
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	4.3	-	nC
Q <sub>G(tot)</sub>	total gate charge	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; V <sub>DS</sub> = 15 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	16.2	-	nC
Source-drain diode							
S	softness factor	I <sub>S</sub> 25 A; V <sub>GS</sub> = 0 V; dI <sub>S</sub> /dt = -100 A/s; V <sub>DS</sub> = 15 V; <a href="#">Fig. 15</a>		-	1	-	

[1] Continuous current is limited by package

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LPAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R4-30YLD	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R4-30YLD	2D430L

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$		-	30	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$		-	30	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	106	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	<a href="#">[1]</a>	-	100	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>	<a href="#">[1]</a>	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 3</a>		-	625	A
$T_{stg}$	storage temperature			-55	175	°C
$T_J$	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
$V_{ESD}$	electrostatic discharge voltage	HBM (JEDEC JESD22-A114)		750	-	V
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$		-	88	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$		-	625	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{J(\text{init})} = 25\text{ °C}$ ; $I_D = 25\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; $t_p = 446\text{ }\mu\text{s}$	<a href="#">[2]</a>	-	217	mJ

[1] Continuous current is limited by package

[2] Protected by 100% test

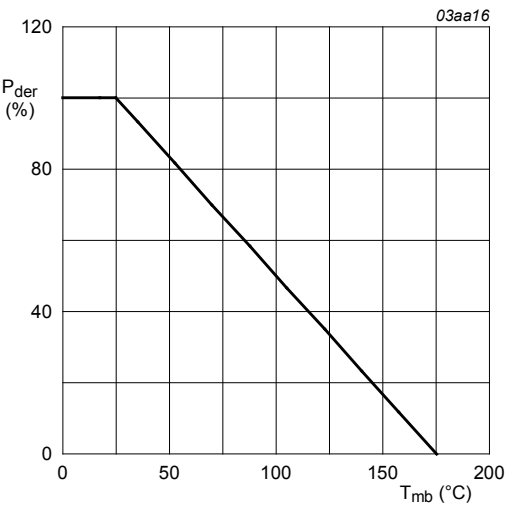
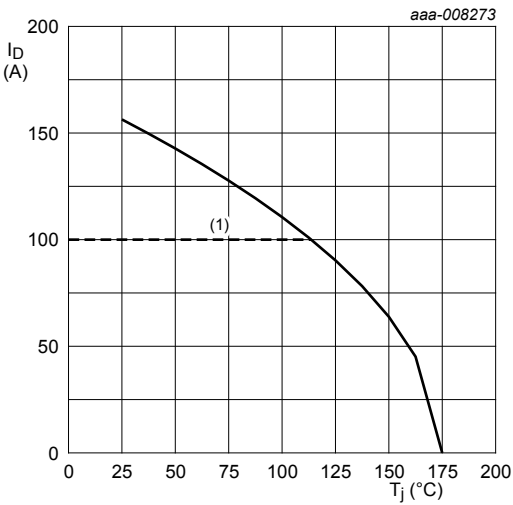


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$



(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

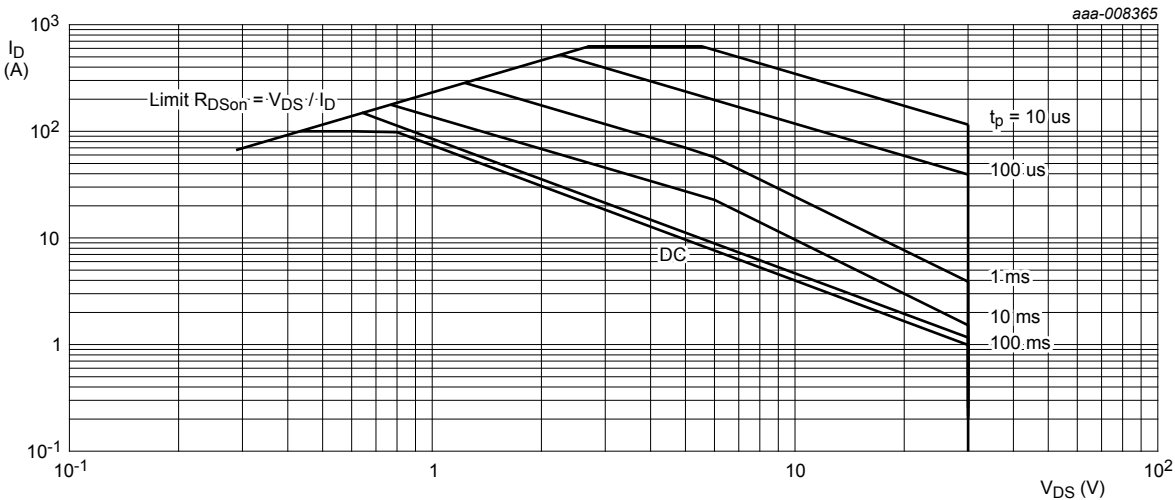


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$$T_{mb} = 25^{\circ}C; I_{DM} \text{ is a single pulse}$$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.25	1.42	K/W

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	Fig. 5	-	50	-	K/W
		Fig. 6	-	125	-	K/W

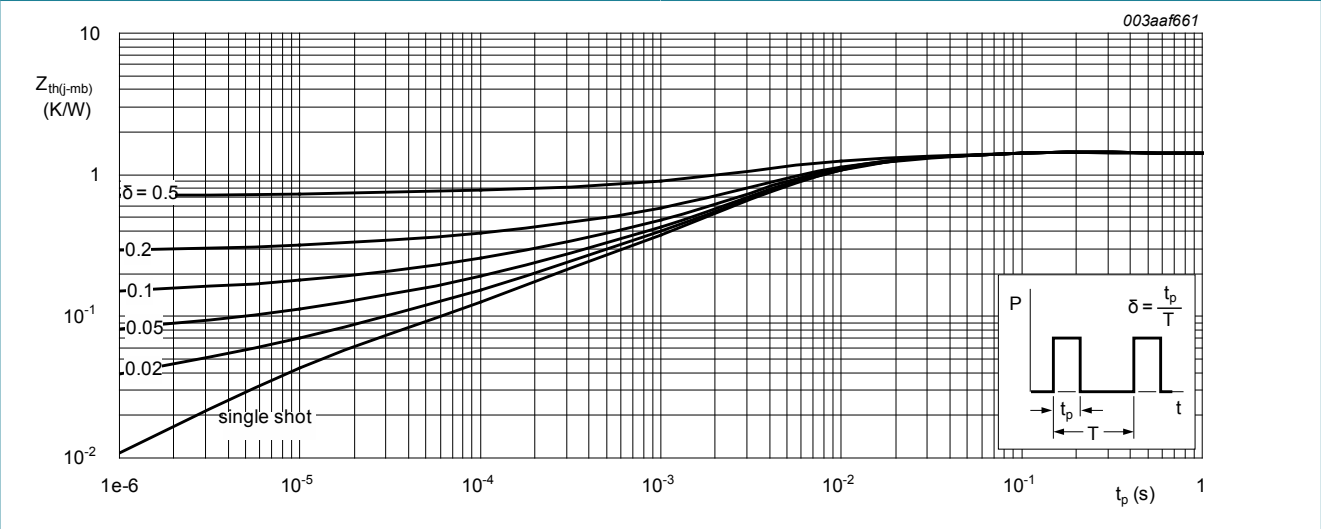
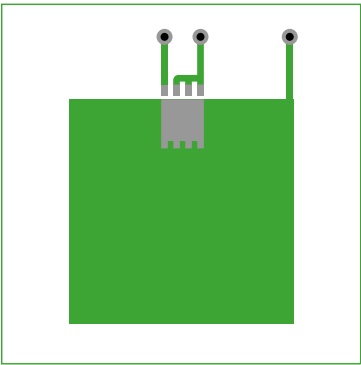
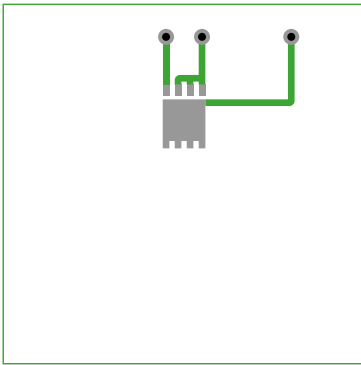


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration



aaa-005750

Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper



aaa-005751

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	30	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C	27	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 25 °C	1.2	1.7	2.2	V

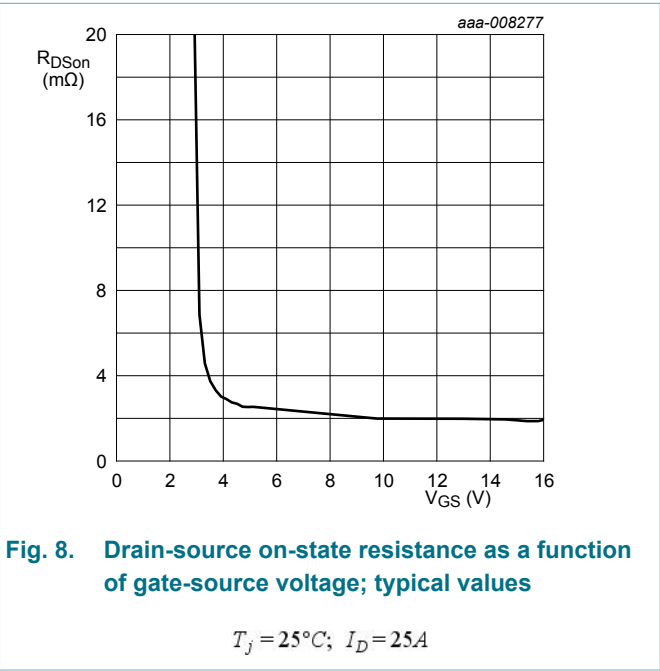
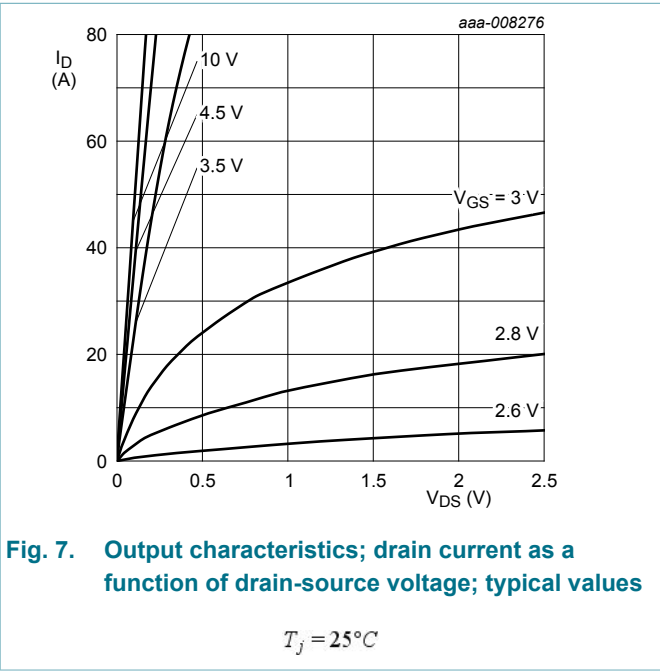
## N-channel 30 V, 2.4 mΩ logic level MOSFET in LPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$	-	-4.5	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 24\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 24\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ }^{\circ}\text{C}$	-	0.92	-	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 16\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	-	100	nA
		$V_{GS} = -16\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 10</a>	-	2.7	3.1	mΩ
		$V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; T_j = 150\text{ }^{\circ}\text{C};$ <a href="#">Fig. 11; Fig. 10</a>	-	-	5.1	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 10</a>	-	2	2.4	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 150\text{ }^{\circ}\text{C};$ <a href="#">Fig. 11; Fig. 10</a>	-	-	4	mΩ
$R_G$	gate resistance	$f = 1\text{ MHz}$	-	0.78	-	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 10\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	31.3	-	nC
		$I_D = 25\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	16.2	-	nC
		$I_D = 0\text{ A}; V_{DS} = 0\text{ V}; V_{GS} = 10\text{ V}$	-	29.3	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25\text{ A}; V_{DS} = 15\text{ V}; V_{GS} = 4.5\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	4.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.8	-	nC
$Q_{GD}$	gate-drain charge		-	4.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}; V_{DS} = 15\text{ V};$ <a href="#">Fig. 12; Fig. 13</a>	-	2.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^{\circ}\text{C};$ <a href="#">Fig. 14</a>	-	2256	-	pF
$C_{oss}$	output capacitance		-	1175	-	pF
$C_{rss}$	reverse transfer capacitance		-	155	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 0.6\text{ } \Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ } \Omega$	-	16.3	-	ns
$t_r$	rise time		-	27.5	-	ns
$t_{d(off)}$	turn-off delay time		-	17.4	-	ns
$t_f$	fall time		-	13.9	-	ns

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$		-	24.8	-	nC
Source-drain diode							
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 15</a>		-	0.81	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A/s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 15</a>		-	30.3	-	ns
$Q_r$	recovered charge		<a href="#">[1]</a>	-	20	-	nC
$t_a$	reverse recovery rise time			-	15	-	ns
$t_b$	reverse recovery fall time			-	15	-	ns
S	softness factor			-	1	-	

[1] Includes capacitive recovery



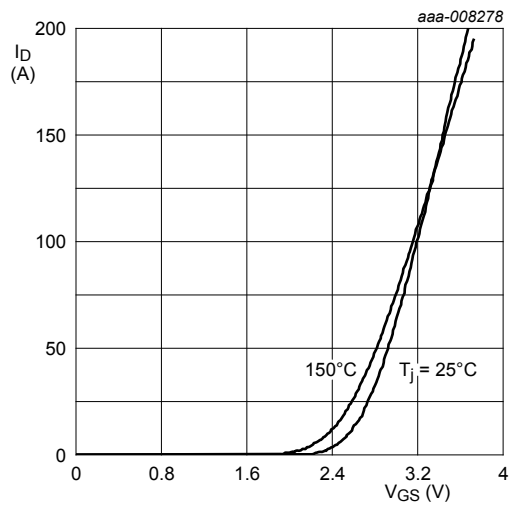


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

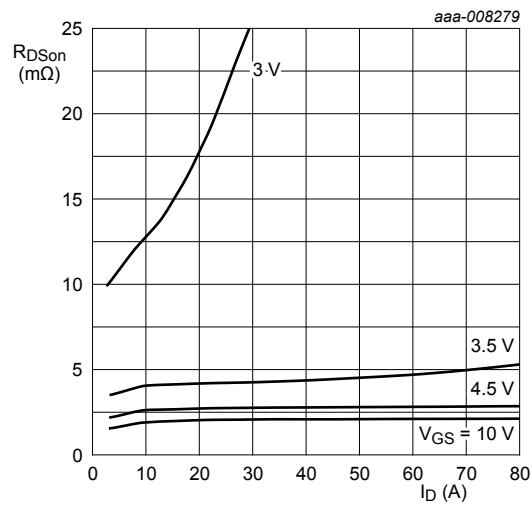


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

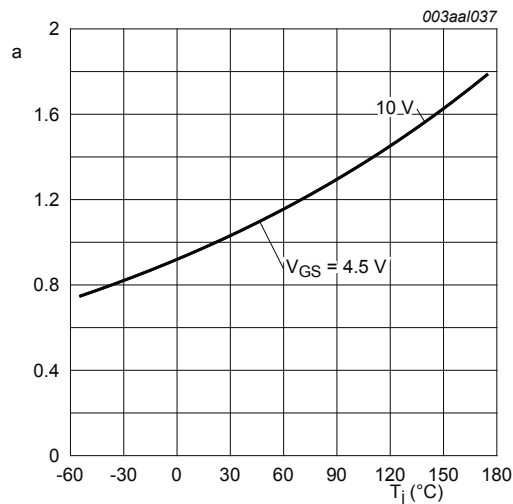


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$\alpha = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

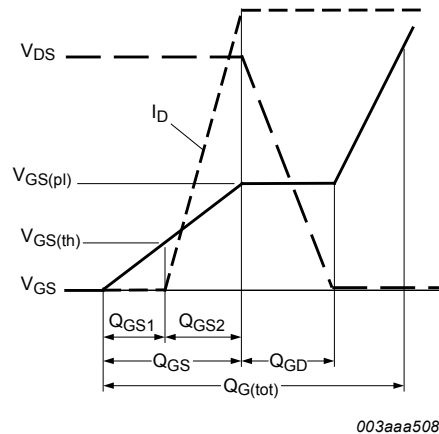


Fig. 12. Gate charge waveform definitions



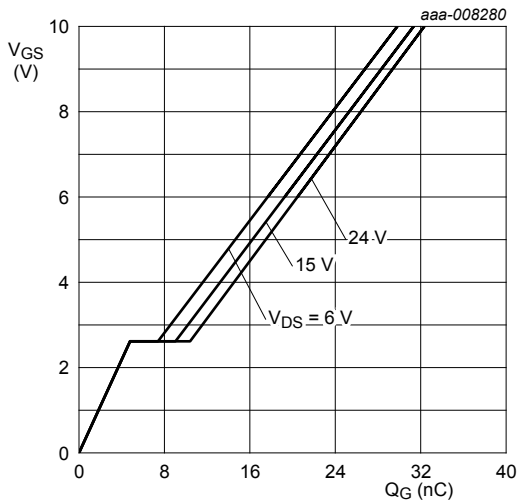


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}\text{C}; I_D = 25\text{ A}$

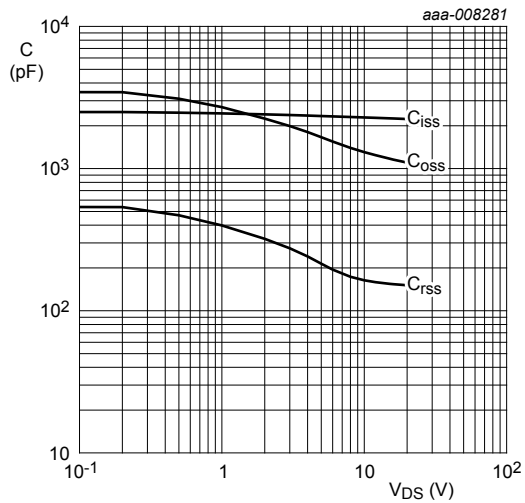


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

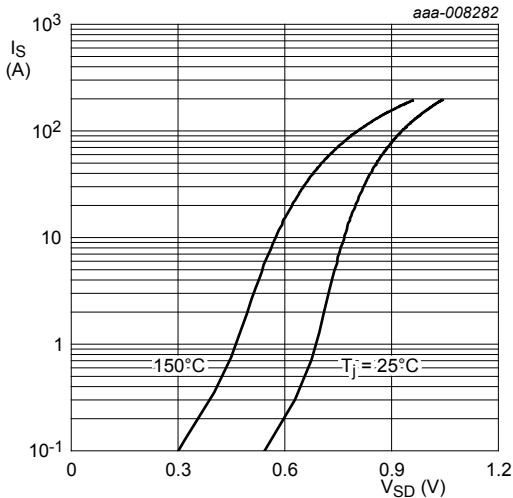


Fig. 15. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{ V}$

11. Package outline

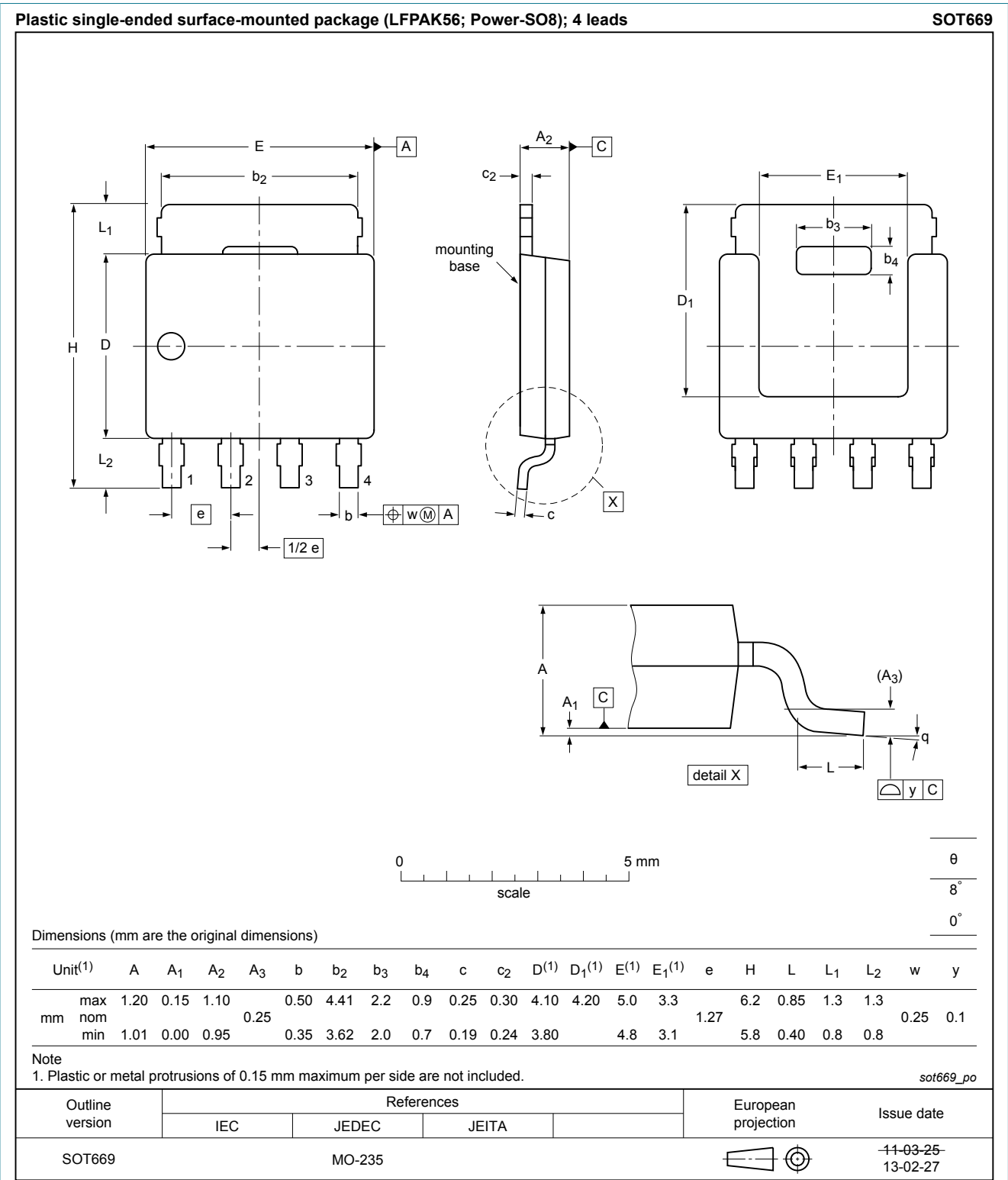


Fig. 16. Package outline LPAK56; Power-SO8 (SOT669)

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### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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