

N-channel 60 V, 4.1 mΩ logic level MOSFET in LFPAK56

20 October 2016

Product data sheet

### 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

### 2. Features and benefits

- Advanced TrenchMOS provides low R<sub>DSon</sub> and low gate charge
- Logic level gate operation
- Avalanche rated, 100% tested
- LFPAK provides maximum power density in a Power SO8 package

### 3. Applications

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- Synchronous rectifier in LLC topology
- Chargers & adaptors with V<sub>out</sub> < 10 V</li>
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

### 4. Quick reference data

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	60	V
ID	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	-	100	А
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	238	W
Static chara	acteristics				_		
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>		-	3.3	4.8	mΩ
Dynamic cl	naracteristics						
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>		-	18.1	-	nC

[1] Continuous current is limited by package.

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### N-channel 60 V, 4.1 mΩ logic level MOSFET in LFPAK56

# 5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	q	G-UFA
4	G	gate	មុប្បូប្	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

# 6. Ordering information

Table 3. Ordering information							
Type number	Package						
	Name	Description	Version				
PSMN4R1-60YL	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669				

# 7. Limiting values

#### Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	60	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ		-	60	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	238	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	[1]	-	100	А
		V <sub>GS</sub> = 5 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>	[1]	-	100	А
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^\circ C$ ; Fig. 3		-	593	А
T <sub>stg</sub>	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-dra	in diode					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	100	А
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \ \mu s$ ; $T_{mb} = 25 \ ^{\circ}C$		-	593	А

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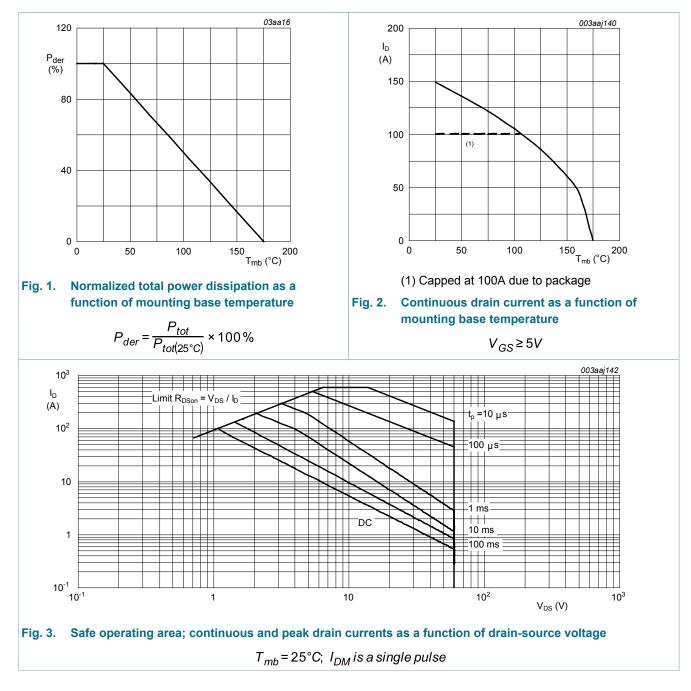
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Symbol	Parameter	Conditions		Min	Мах	Unit
Avalanche rug	gedness					-
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$I_D$ = 100 A; $V_{sup} \le 60$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[2][3]	-	199	mJ

[1]

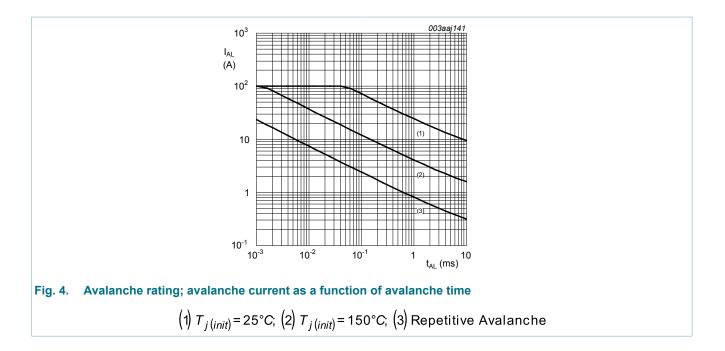
Continuous current is limited by package. Single-pulse avalanche rating limited by maximum junction temperature of 175 °C. [2]

[3] Refer to application note AN10273 for further information.



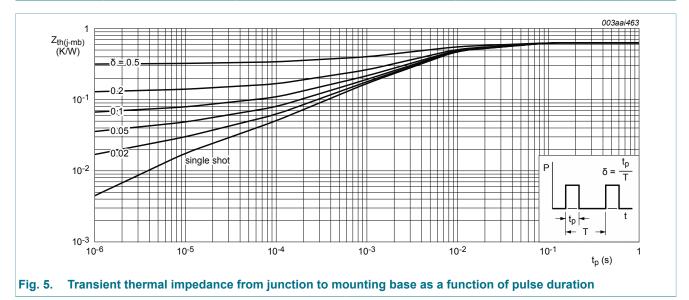
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#### N-channel 60 V, 4.1 mΩ logic level MOSFET in LFPAK56



### 8. Thermal characteristics

Table 5. Thermal characteristics							
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	Fig. <u>5</u>		-	-	0.63	K/W



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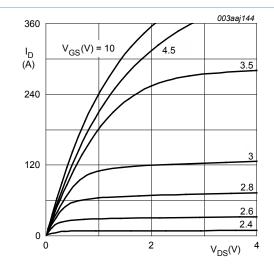
### 9. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	60	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	54	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <u>Fig. 9</u> ; <u>Fig. 10</u>	1.4	1.7	2.1	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; <u>Fig. 9</u>	-	-	2.45	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; <u>Fig. 9</u>	0.5	-	-	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C	-	-	500	μA
		V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.12	10	μA
I <sub>GSS</sub>	gate leakage current	$V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
R <sub>DSon</sub>	drain-source on-state	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <u>Fig. 11</u>	-	3.3	4.8	mΩ
resistance	resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; Fig. 11	-	2.9	4.1	mΩ
	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 175 °C; Fig. 11; Fig. 12	-	-	10.8	mΩ	
Dynamic ch	aracteristics		I			
Q <sub>G(tot)</sub>	total gate charge	$I_{D} = 25 \text{ A}; \text{ V}_{DS} = 48 \text{ V}; \text{ V}_{GS} = 10 \text{ V};$ $T_{j} = 25 ^{\circ}\text{C}; \text{ Fig. 13}; \text{ Fig. 14}$	-	103	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 5 V;	-	54.8	-	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C; <u>Fig. 13; Fig. 14</u>	-	13.6	-	nC
Q <sub>GD</sub>	gate-drain charge		-	18.1	-	nC
C <sub>iss</sub>	input capacitance	$V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz;	-	5890	7853	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 15</u>	-	506	607	pF
C <sub>rss</sub>	reverse transfer capacitance		-	276	378	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 45 V; R <sub>L</sub> = 1.8 Ω; V <sub>GS</sub> = 5 V;	-	28	-	ns
t <sub>r</sub>	rise time	R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C	-	53	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	80	-	ns
t <sub>f</sub>	fall time		-	47	-	ns
Source-dra	in diode	1	I			

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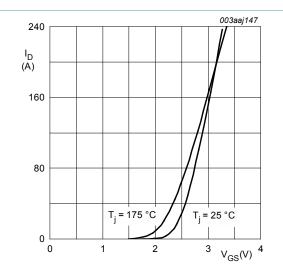
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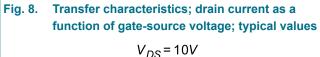
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
t <sub>rr</sub>	reverse recovery time	$I_{\rm S}$ = 20 A; dI_{\rm S}/dt = -100 A/µs; V_{\rm GS} = 0 V;	-	29	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V; T <sub>j</sub> = 25 °C	-	28	-	nC



T<sub>j</sub> = 25 °C; t<sub>p</sub> = 300 μs







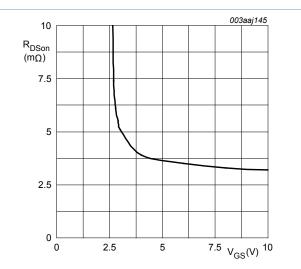


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

 $T_i = 25^{\circ}C; I_D = 25A$ 

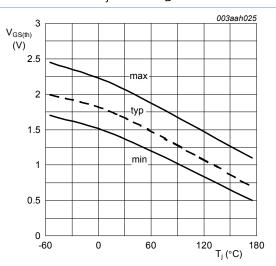


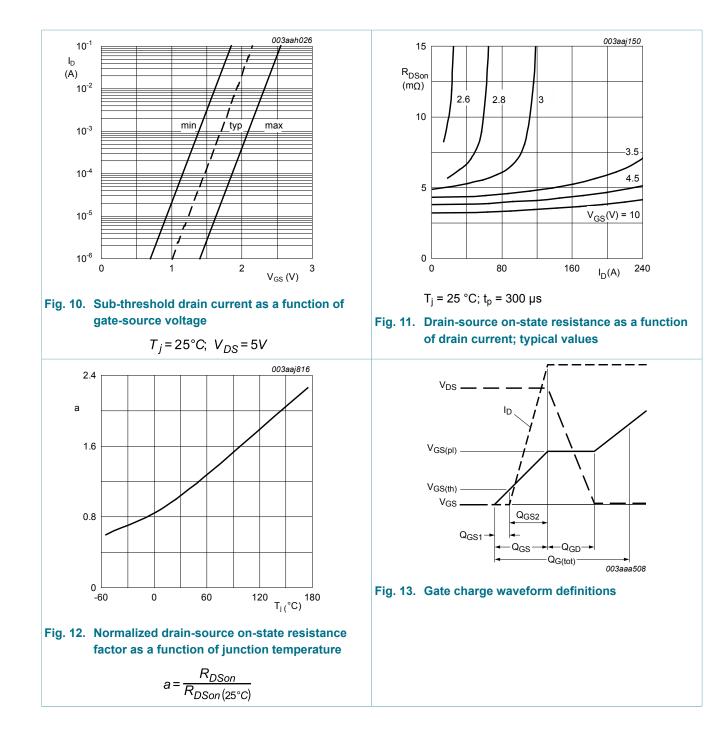
Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$

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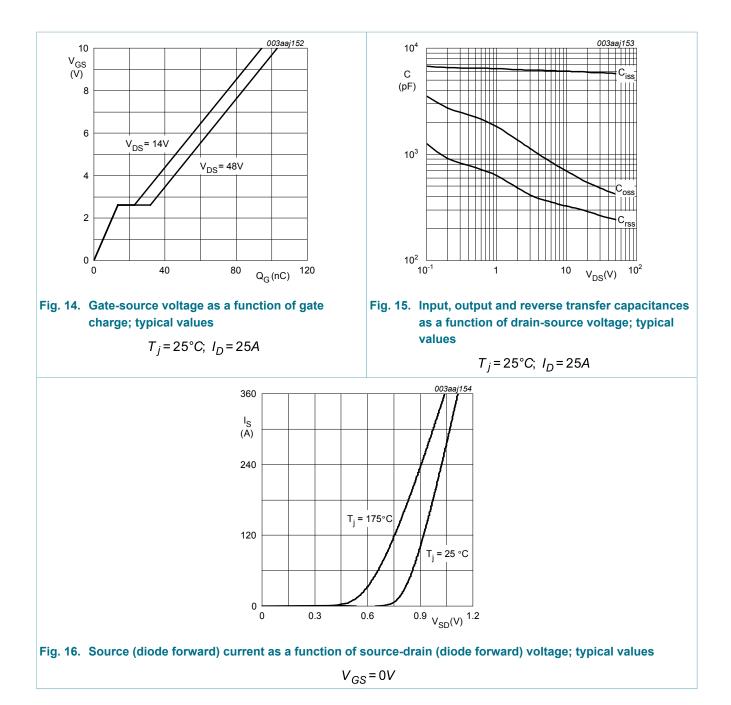
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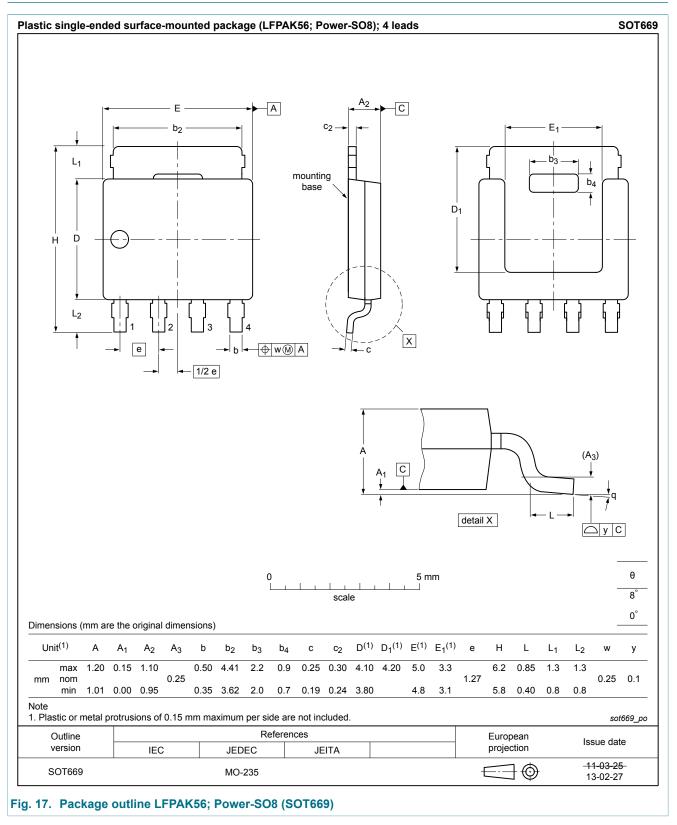
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#### N-channel 60 V, 4.1 mΩ logic level MOSFET in LFPAK56

### **10. Package outline**



PSMN4R1-60YL

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