



PSMN5R9-30YL

N-channel 6.1 mΩ 30 V TrenchMOS logic level FET in LPAK

Rev. 2 — 16 May 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in industrial and communications applications.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- Class-D amplifiers
- DC-to-DC converters
- Motor control
- Server power supplies

1.4 Quick reference data

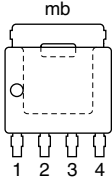
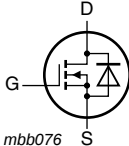
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	-	78	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	63	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$	-	5.2	6.1	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 60\text{ A}$; $V_{DS} = 15\text{ V}$; see Figure 14 ; see Figure 15	-	4.8	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 60\text{ A}$; $V_{DS} = 15\text{ V}$; see Figure 14 ; see Figure 15	-	10.5	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $I_D = 78\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ Ω}$; unclamped	-	-	28	mJ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

SOT669 (LPAK; Power-SO8)

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN5R9-30YL	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	30	V
V_{DSM}	peak drain-source voltage	$t_p \leq 25\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 90\text{ J}$; pulsed	-	35	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; see Figure 1	-	55	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1	-	78	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3	-	310	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	63	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	78	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	310	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 78\text{ A}$; $V_{sup} \leq 30\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped	-	28	mJ

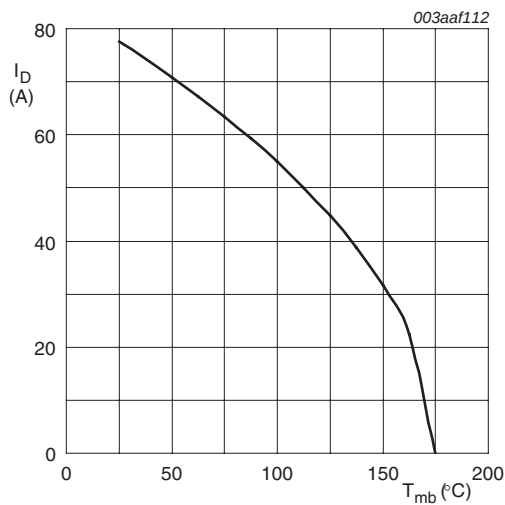
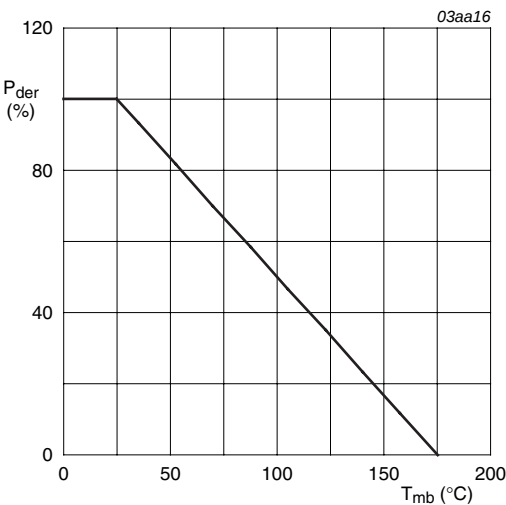
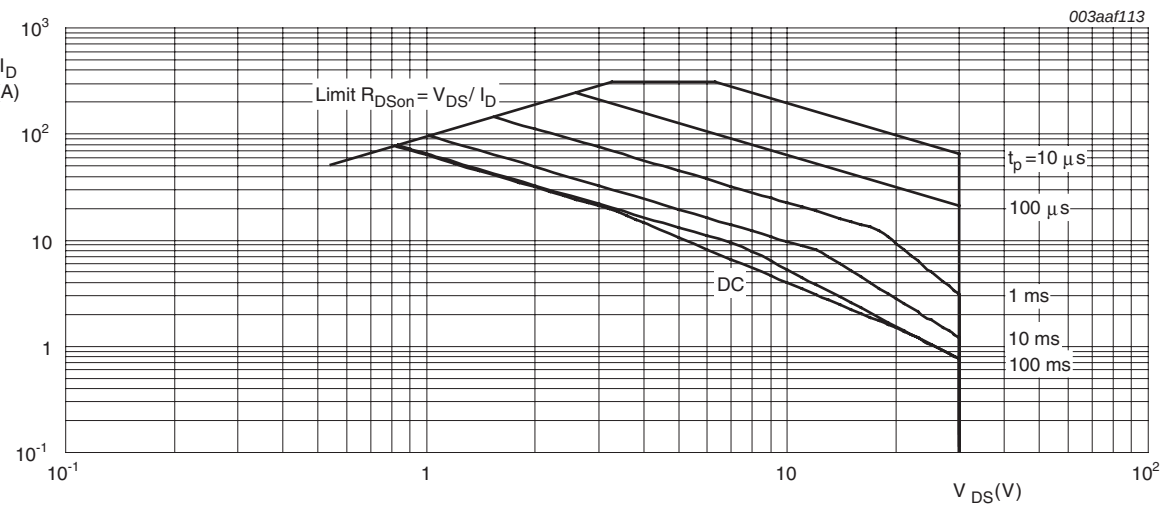


Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$$T_{mb} = 25^{\circ}\text{C}; I_{DM} \text{ is single pulse}$$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	1.17	2.37	K/W

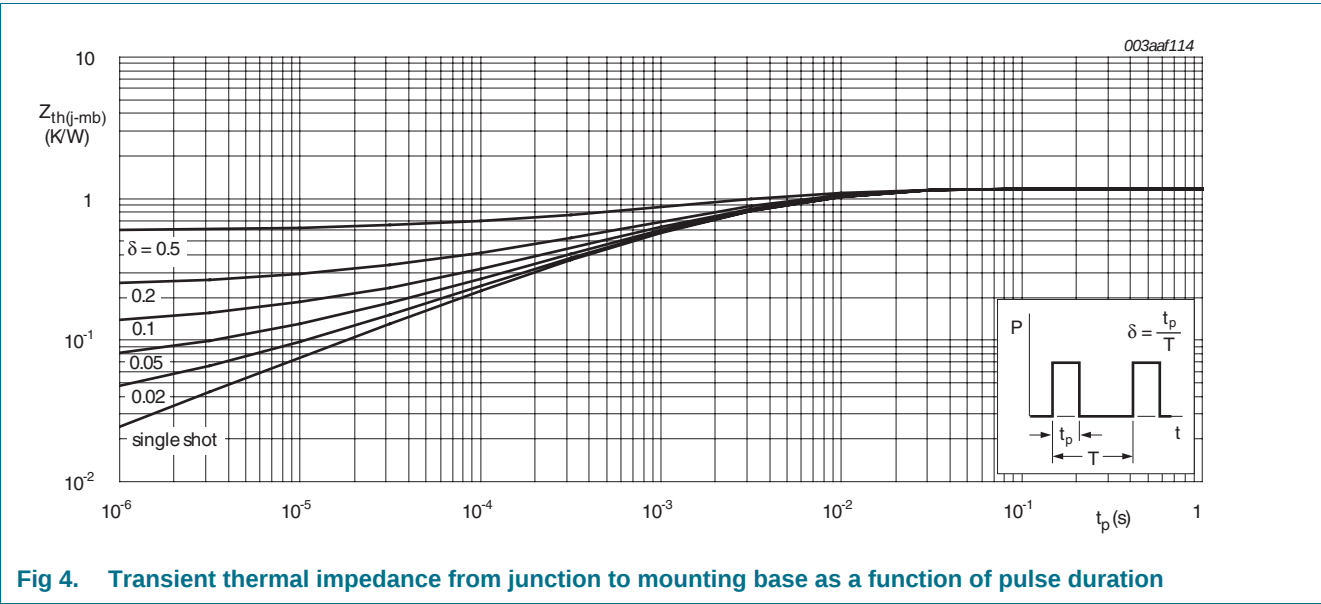


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 ^\circ C$; see Figure 11 ; see Figure 12	1.3	1.7	2.15	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 150 ^\circ C$; see Figure 12	0.5	-	-	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 ^\circ C$; see Figure 12	-	-	2.55	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 ^\circ C$	-	0.02	1	μA
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	10	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 20 A; T_j = 25 ^\circ C$	-	7.45	9	mΩ
		$V_{GS} = 10 V; I_D = 20 A; T_j = 150 ^\circ C$; see Figure 13	-	-	11	mΩ
		$V_{GS} = 10 V; I_D = 20 A; T_j = 25 ^\circ C$	-	5.2	6.1	mΩ
R_G	gate resistance	$f = 1 MHz$	-	2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 60 A; V_{DS} = 15 V; V_{GS} = 4.5 V$; see Figure 14 ; see Figure 15	-	10.5	-	nC
		$I_D = 60 A; V_{DS} = 15 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	21.3	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	19.5	-	nC
Q_{GS}	gate-source charge	$I_D = 60 A; V_{DS} = 15 V; V_{GS} = 10 V$; see Figure 14 ; see Figure 15	-	3.3	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	1.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.5	-	nC
Q_{GD}	gate-drain charge		-	4.8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 15 V$; see Figure 14 ; see Figure 15	-	3.2	-	V
C_{iss}	input capacitance	$V_{DS} = 15 V; V_{GS} = 0 V; f = 1 MHz$; $T_j = 25 ^\circ C$; see Figure 16	-	1226	-	pF
C_{oss}	output capacitance		-	254	-	pF
C_{rss}	reverse transfer capacitance		-	119	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V; R_L = 0.25 \Omega; V_{GS} = 4.5 V$; $R_{G(ext)} = 4.7 \Omega$	-	16	-	ns
t_r	rise time		-	31	-	ns
$t_{d(off)}$	turn-off delay time		-	24	-	ns
t_f	fall time		-	10	-	ns

Table 6. Characteristics ...continued
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 20\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A/}\mu\text{s}$;	-	32	-	ns
Q_r	recovered charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$	-	25	-	nC

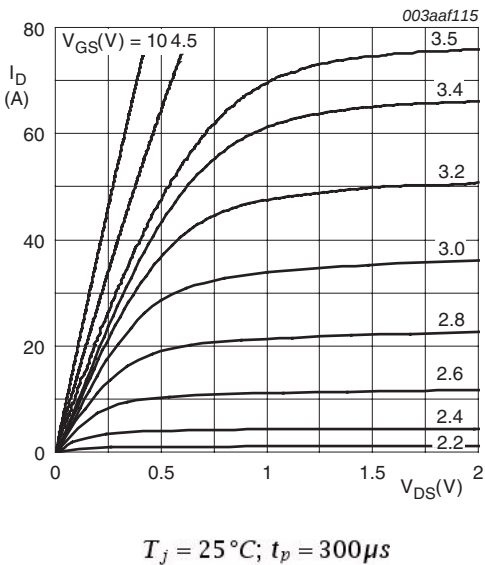


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

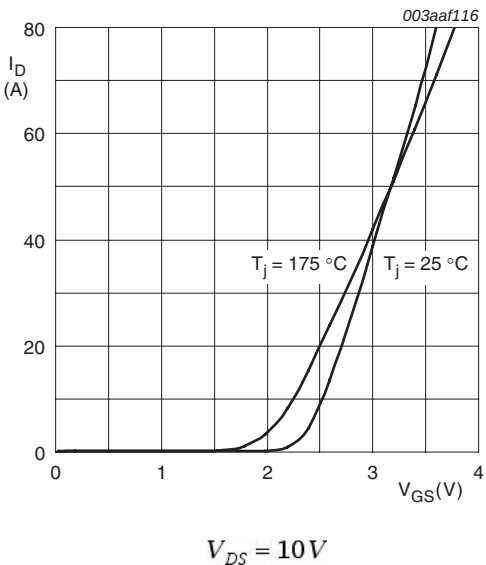


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

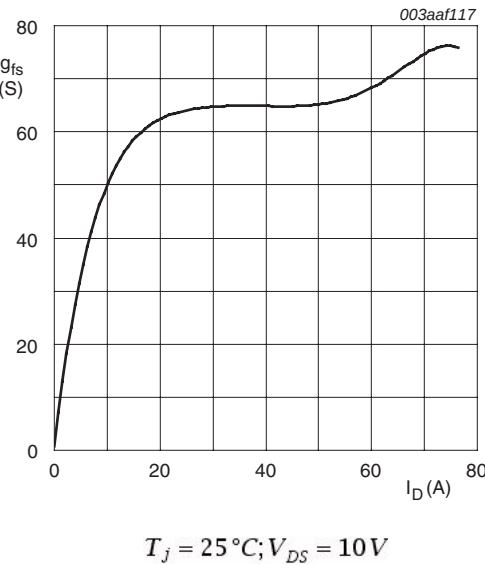


Fig 7. Forward transconductance as a function of drain current; typical values

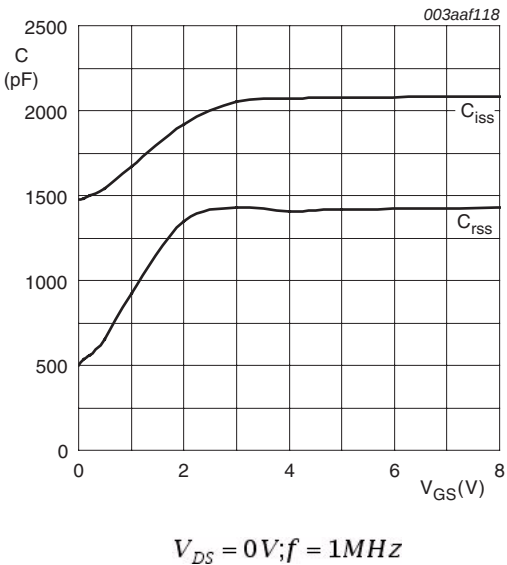
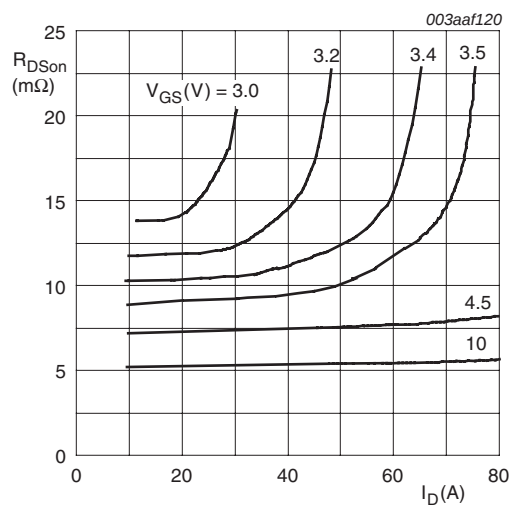
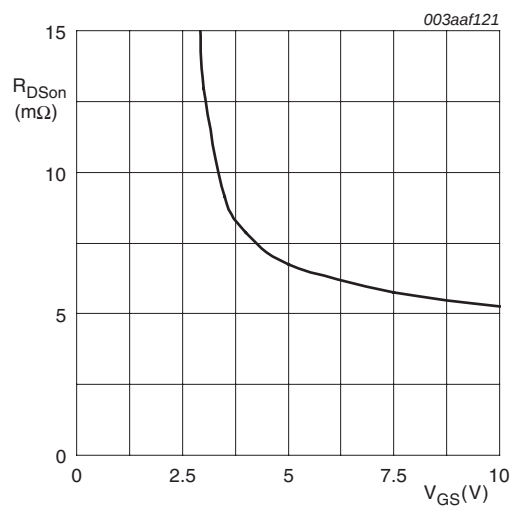


Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



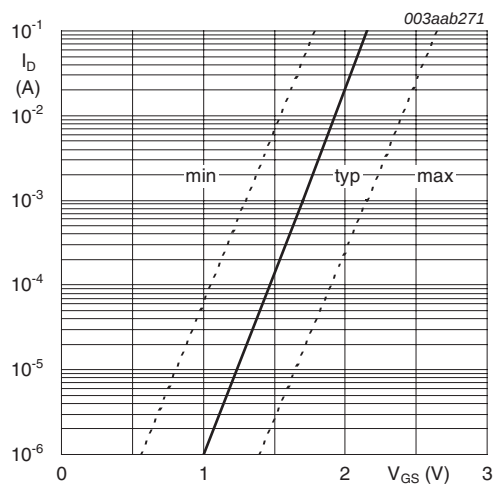
$T_j = 25^\circ\text{C}; t_p = 300\mu\text{s}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



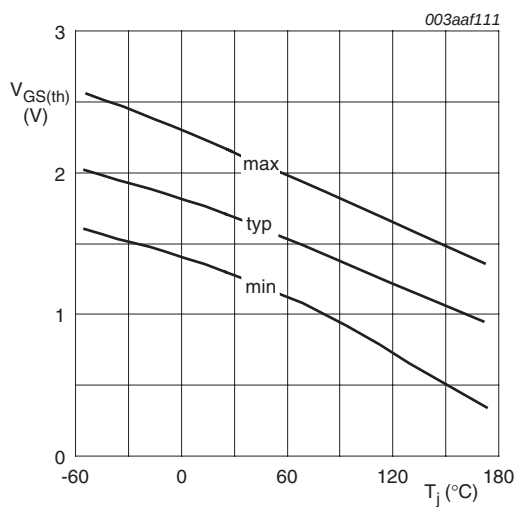
$T_j = 25^\circ\text{C}; I_D = 20\text{A}$

Fig 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\text{mA}; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature

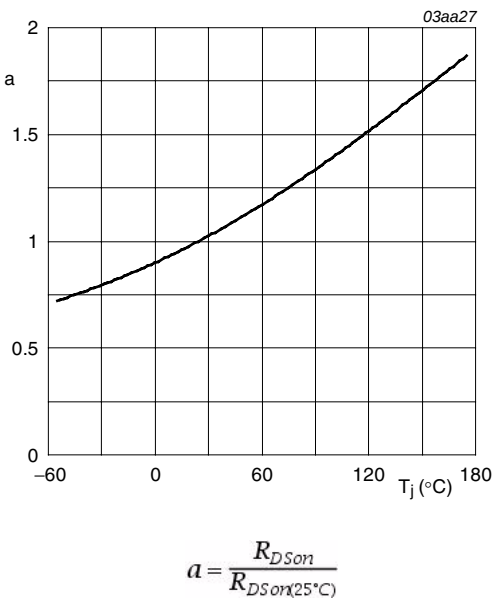


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

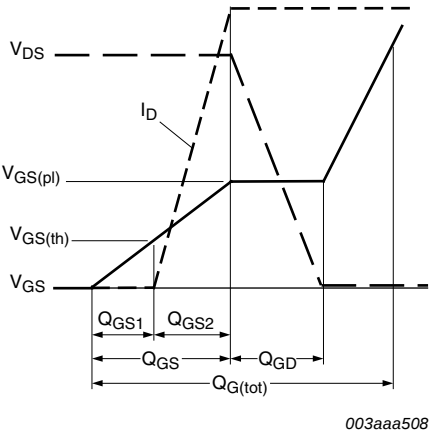


Fig 14. Gate charge waveform definitions

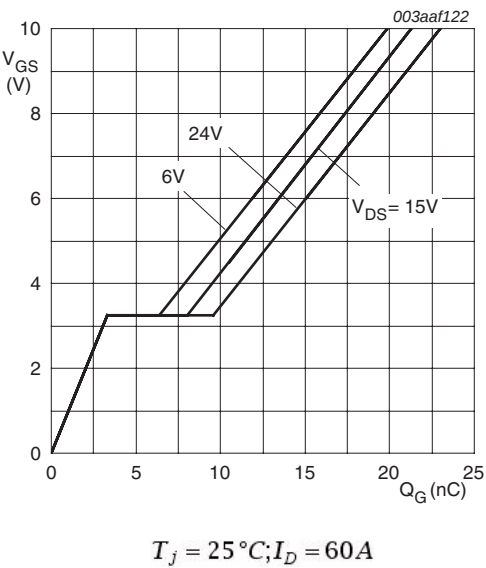


Fig 15. Gate-source voltage as a function of gate charge; typical values

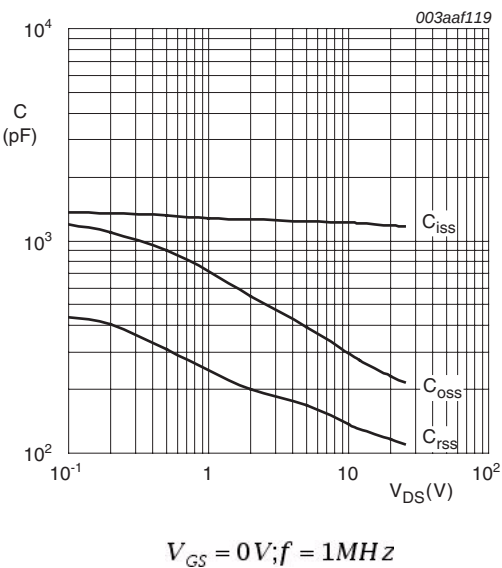


Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

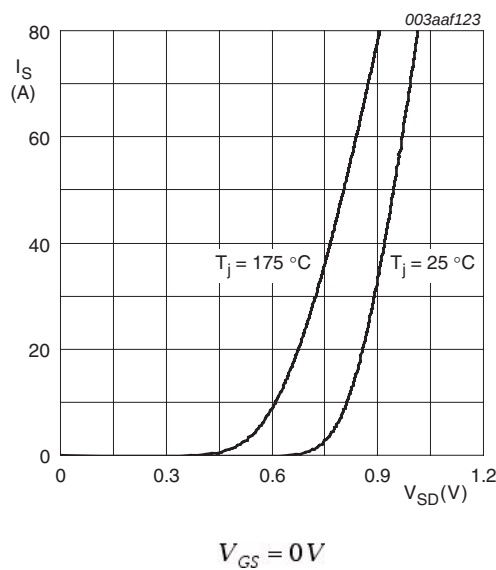


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads

SOT669

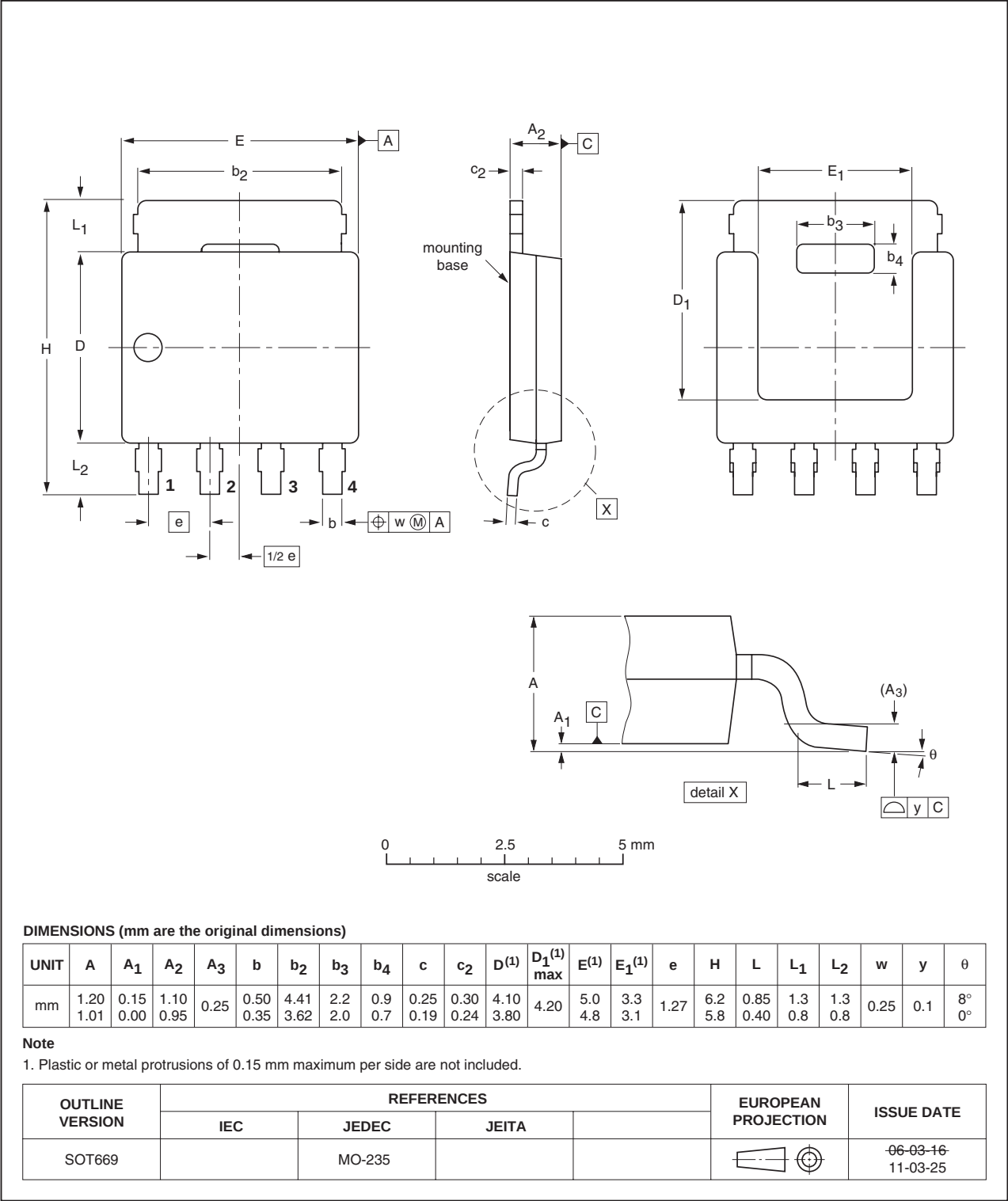


Fig 18. Package outline SOT669 (LPAK; Power-SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN5R9-30YL v.2	20110516	Product data sheet	-	PSMN5R9-30YL v.1
Modifications:	• Various changes to content.			
PSMN5R9-30YL v.1	20110217	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^[1] ^[2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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