



# PSMN6R5-30MLD

N-channel 30 V, 6.5 mΩ logic level MOSFET in LPAK33  
using NextPowerS3 Technology

5 July 2017

Product data sheet

## 1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LPAK33 package. NextPowerS3 portfolio utilising NXP's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETS with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

## 2. Features and benefits

- Ultra low  $Q_G$ ,  $Q_{GD}$  and  $Q_{OSS}$  for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with < 1 µA leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Mini Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Exposed leads for optimal visual solder inspection

## 3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

## 4. Quick reference data

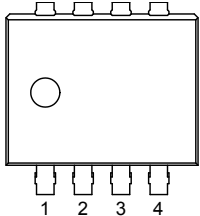
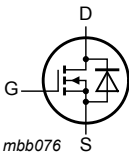
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	30	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	65	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	51	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>	-	7	8.6	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 15\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	1.7	-	nC

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK33 (SOT1210)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN6R5-30MLD	LPAK33	Plastic single ended surface mounted package (LPAK33); 8 leads	SOT1210

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN6R5-30MLD	6D530L

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	51	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	65	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; <a href="#">Fig. 2</a>	-	46	A

## N-channel 30 V, 6.5 mΩ logic level MOSFET in LPAK33 using NextPowerS3 Technology

Symbol	Parameter	Conditions		Min	Max	Unit
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25^\circ C$ ; Fig. 3		-	262	A
$T_{stg}$	storage temperature			-55	175	$^\circ C$
$T_j$	junction temperature			-55	175	$^\circ C$
$T_{sld(M)}$	peak soldering temperature			-	260	$^\circ C$
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25^\circ C$		-	42	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25^\circ C$		-	262	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 15 A$ ; $V_{sup} \leq 30 V$ ; $R_{GS} = 50 \Omega$ ; $V_{GS} = 10 V$ ; $T_{j(init)} = 25^\circ C$ ; unclamped; $t_p = 146 \mu s$	[1]	-	42.7	mJ

[1] Protected by 100% test

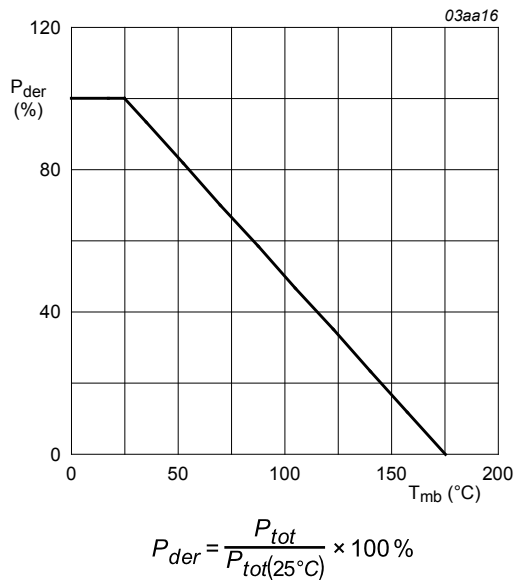


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

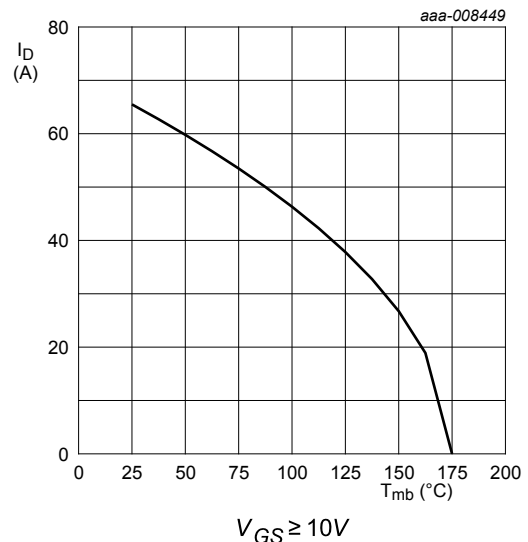
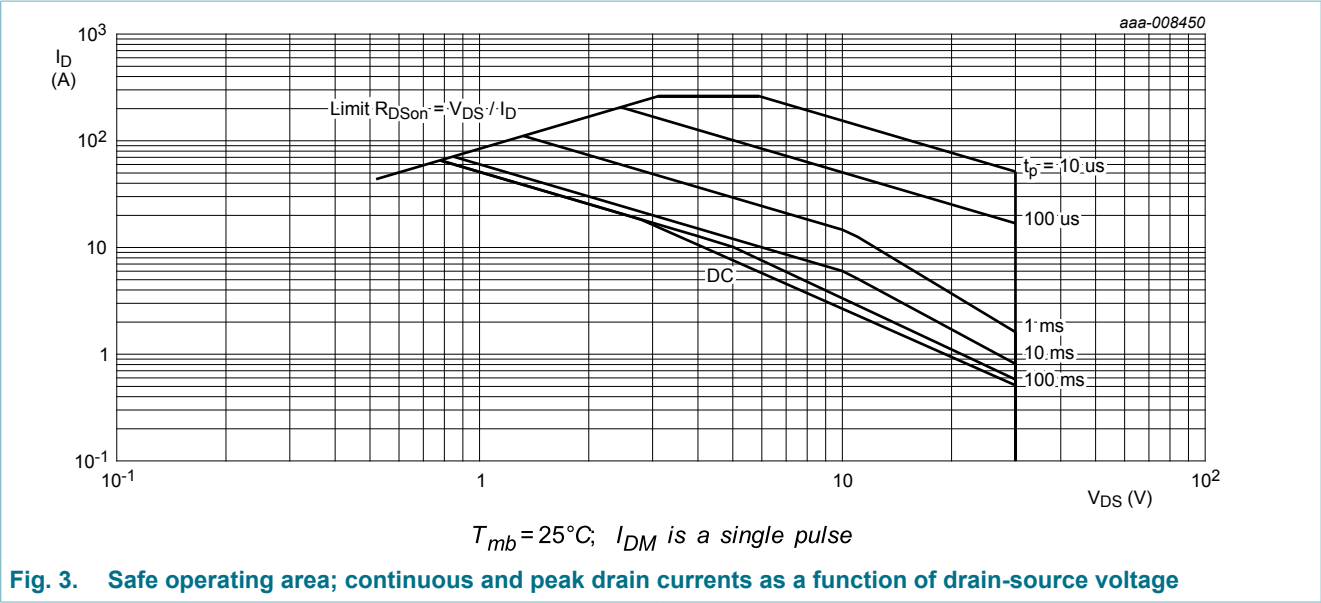


Fig. 2. Continuous drain current as a function of mounting base temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	2.72	2.94	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a>	-	57	-	K/W
		<a href="#">Fig. 6</a>	-	178	-	K/W

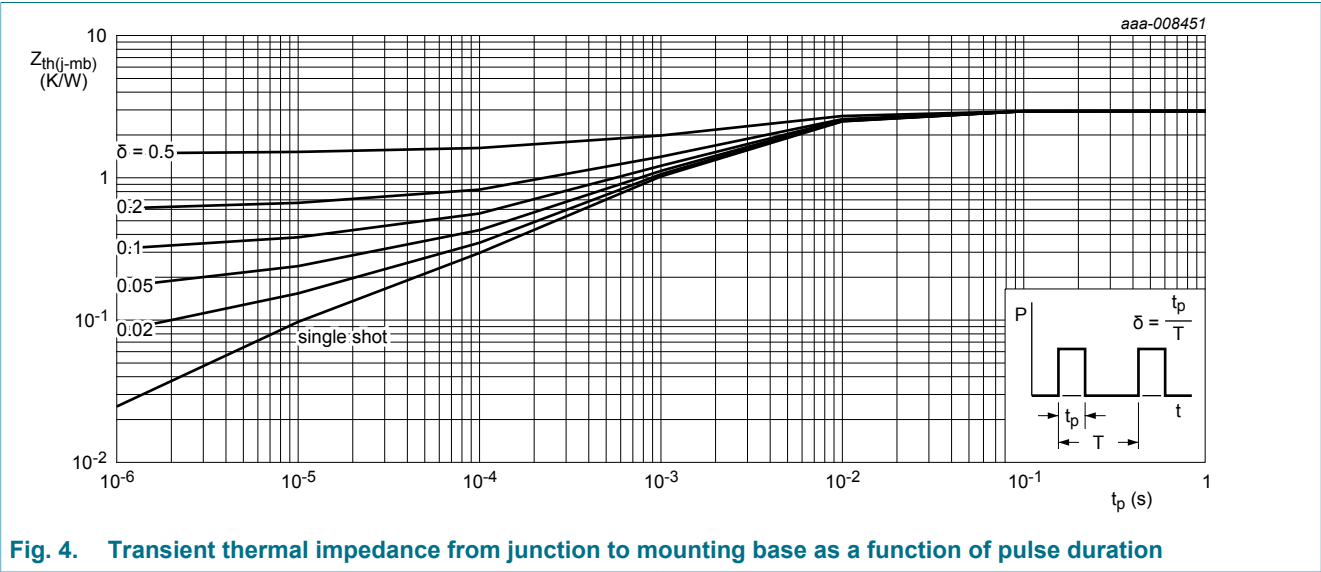


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

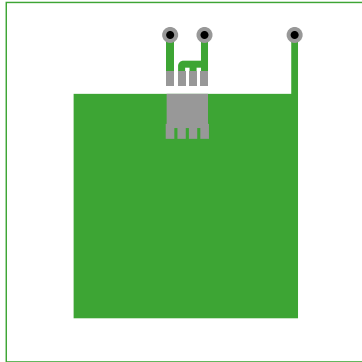


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

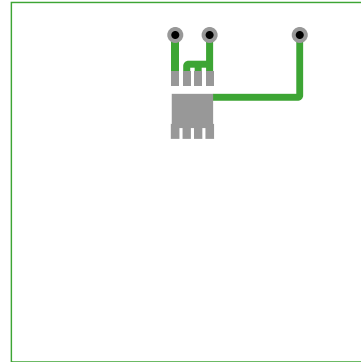


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 ^\circ C$	1.2	1.68	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 ^\circ C \leq T_j \leq 150 ^\circ C$	-	-3.9	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 25 ^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 24 V; V_{GS} = 0 V; T_j = 125 ^\circ C$	-	0.42	-	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 15 A; T_j = 25 ^\circ C;$ <a href="#">Fig. 10</a>	-	7	8.6	mΩ
		$V_{GS} = 4.5 V; I_D = 15 A; T_j = 150 ^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	14.2	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 25 ^\circ C;$ <a href="#">Fig. 10</a>	-	5.5	6.5	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 150 ^\circ C;$ <a href="#">Fig. 10; Fig. 11</a>	-	-	10.7	mΩ
$R_G$	gate resistance	$f = 1 MHz$	-	0.44	-	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Dynamic characteristics</b>							
$Q_{G(tot)}$	total gate charge	$I_D = 15\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	13.6	-	nC
		$I_D = 15\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	6.4	-	nC
		$I_D = 0\text{ A}$ ; $V_{DS} = 0\text{ V}$ ; $V_{GS} = 10\text{ V}$		-	12.7	-	nC
$Q_{GS}$	gate-source charge	$I_D = 15\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; $V_{GS} = 4.5\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	1.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	1.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	0.2	-	nC
$Q_{GD}$	gate-drain charge			-	1.7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 15\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	2	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a>		-	817	-	pF
$C_{oss}$	output capacitance			-	605	-	pF
$C_{rss}$	reverse transfer capacitance			-	62	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}$ ; $R_L = 1\text{ }Ω$ ; $V_{GS} = 4.5\text{ V}$ ; $R_{G(ext)} = 5\text{ }Ω$		-	7.5	-	ns
$t_r$	rise time			-	11	-	ns
$t_{d(off)}$	turn-off delay time			-	9.8	-	ns
$t_f$	fall time			-	7.2	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$		-	12.3	-	nC
<b>Source-drain diode</b>							
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 15</a>		-	0.81	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 15\text{ A}$ ; $di_S/dt = -100\text{ A/}μ\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; <a href="#">Fig. 16</a>		-	23.8	-	ns
$Q_r$	recovered charge		<a href="#">[1]</a>	-	12.6	-	nC
$t_a$	reverse recovery rise time			-	10.3	-	ns
$t_b$	reverse recovery fall time			-	13.5	-	ns
$S$	softness factor			-	1.3	-	

[1] includes capacitive recovery

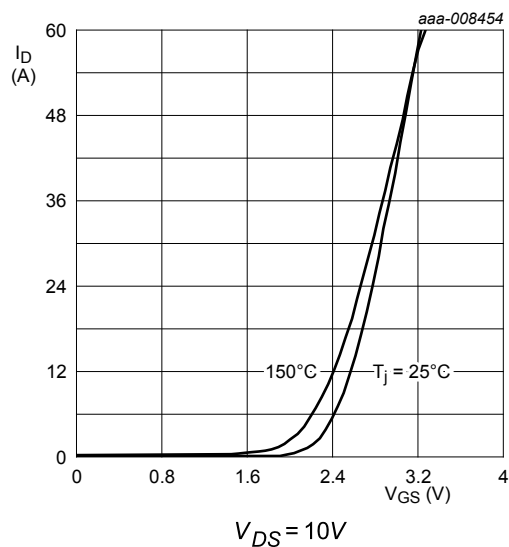


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

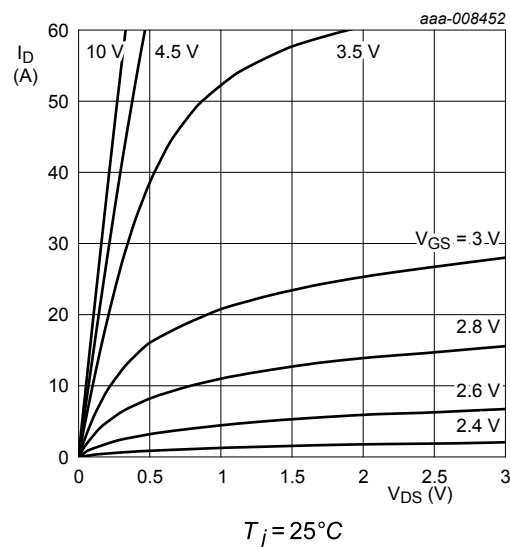


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

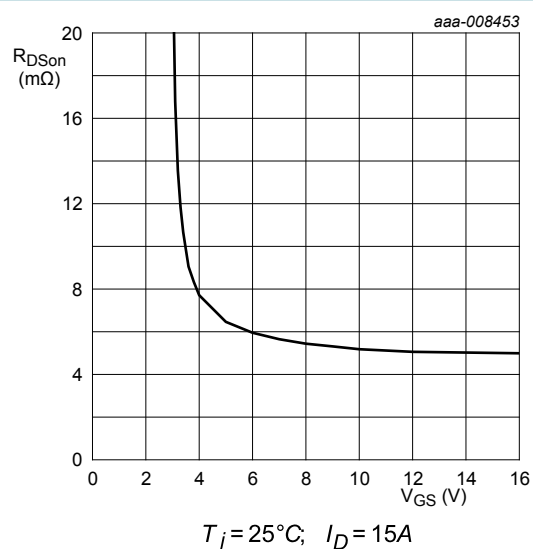


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

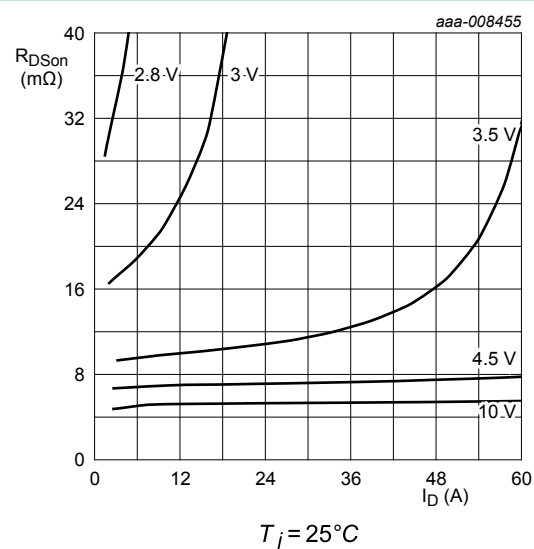


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

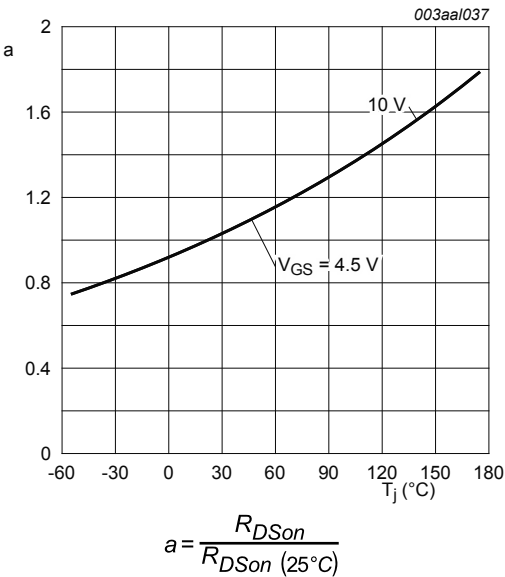


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

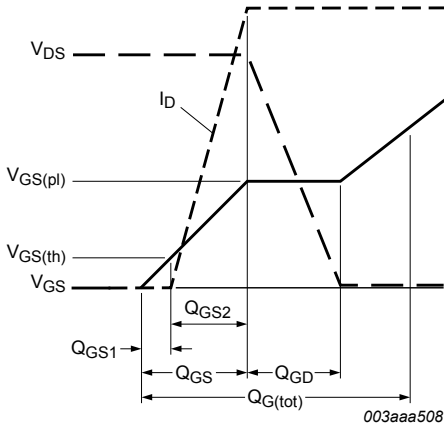


Fig. 12. Gate charge waveform definitions

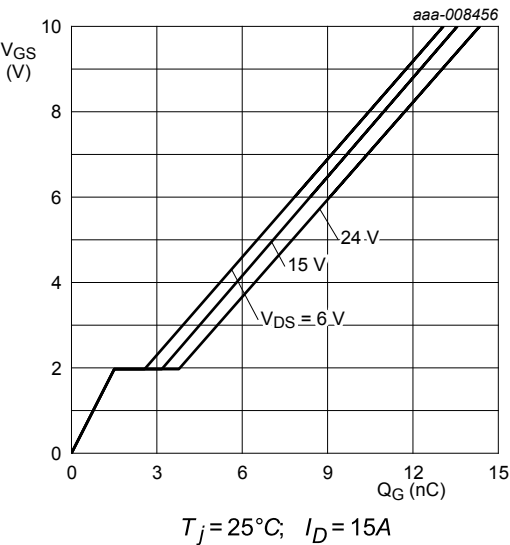


Fig. 13. Gate-source voltage as a function of gate charge; typical values

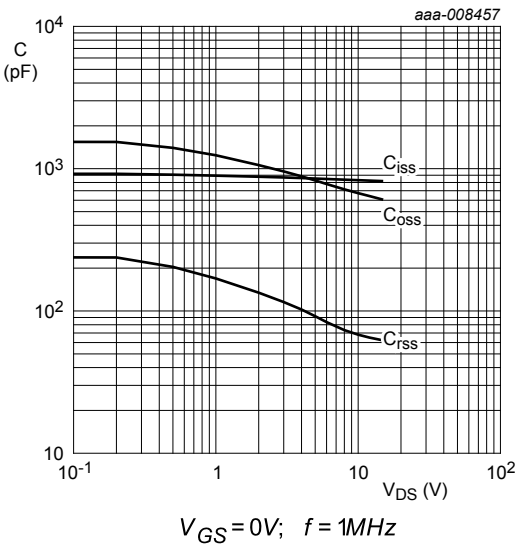


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



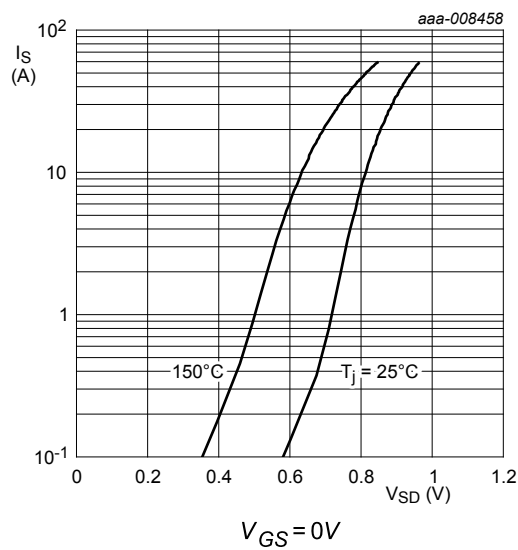


Fig. 15. Source current as a function of source-drain voltage; typical values

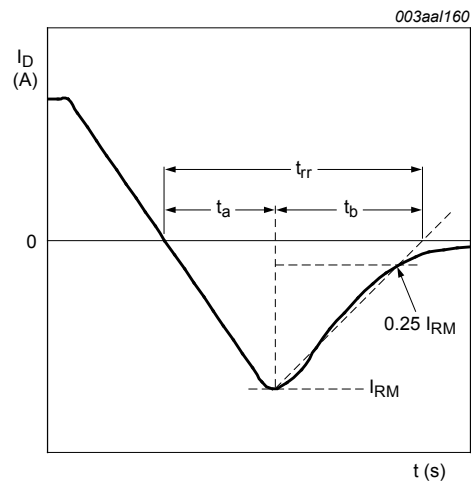


Fig. 16. Reverse recovery timing definition

11. Package outline

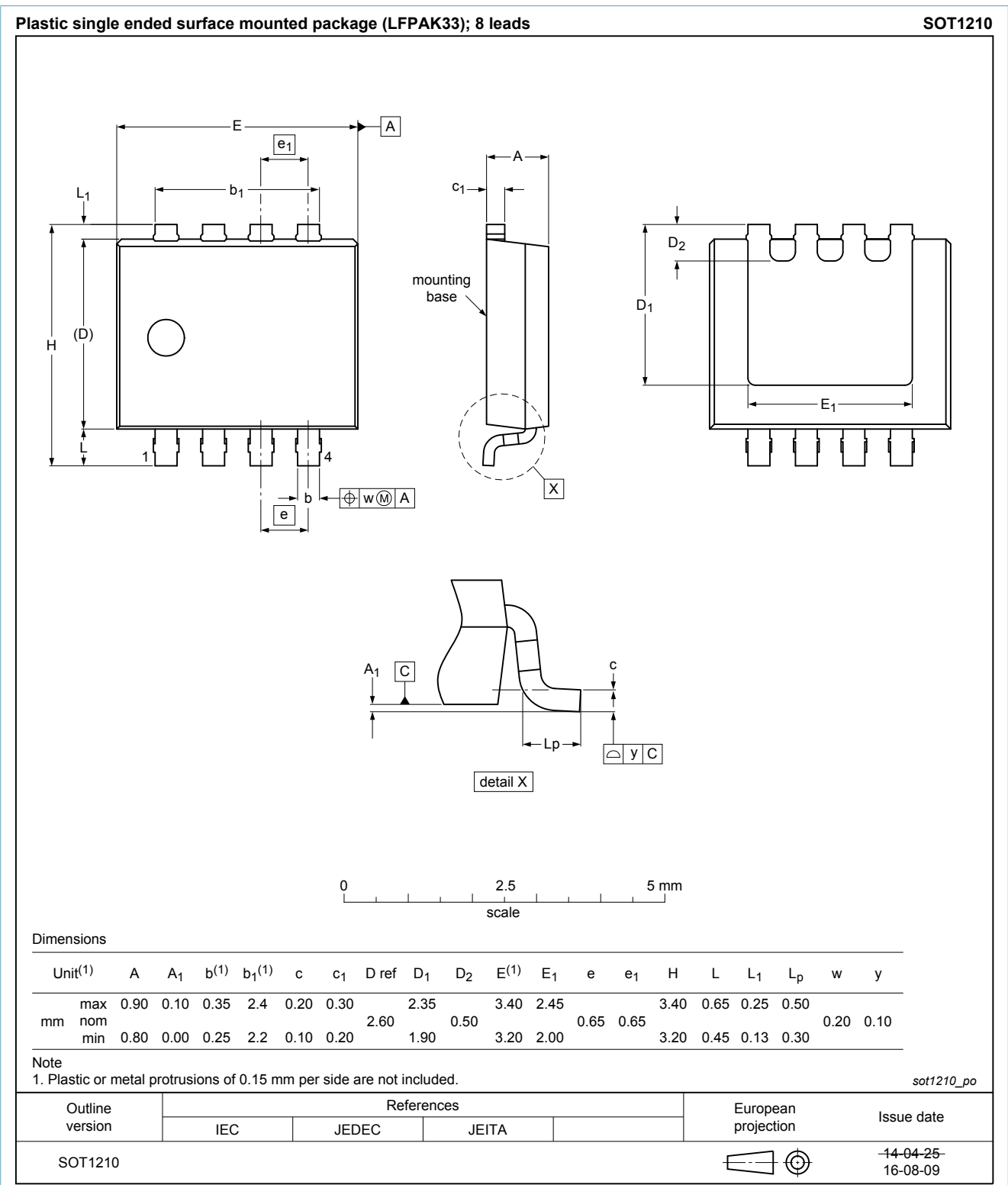


Fig. 17. Package outline LPAK33 (SOT1210)

12. Soldering

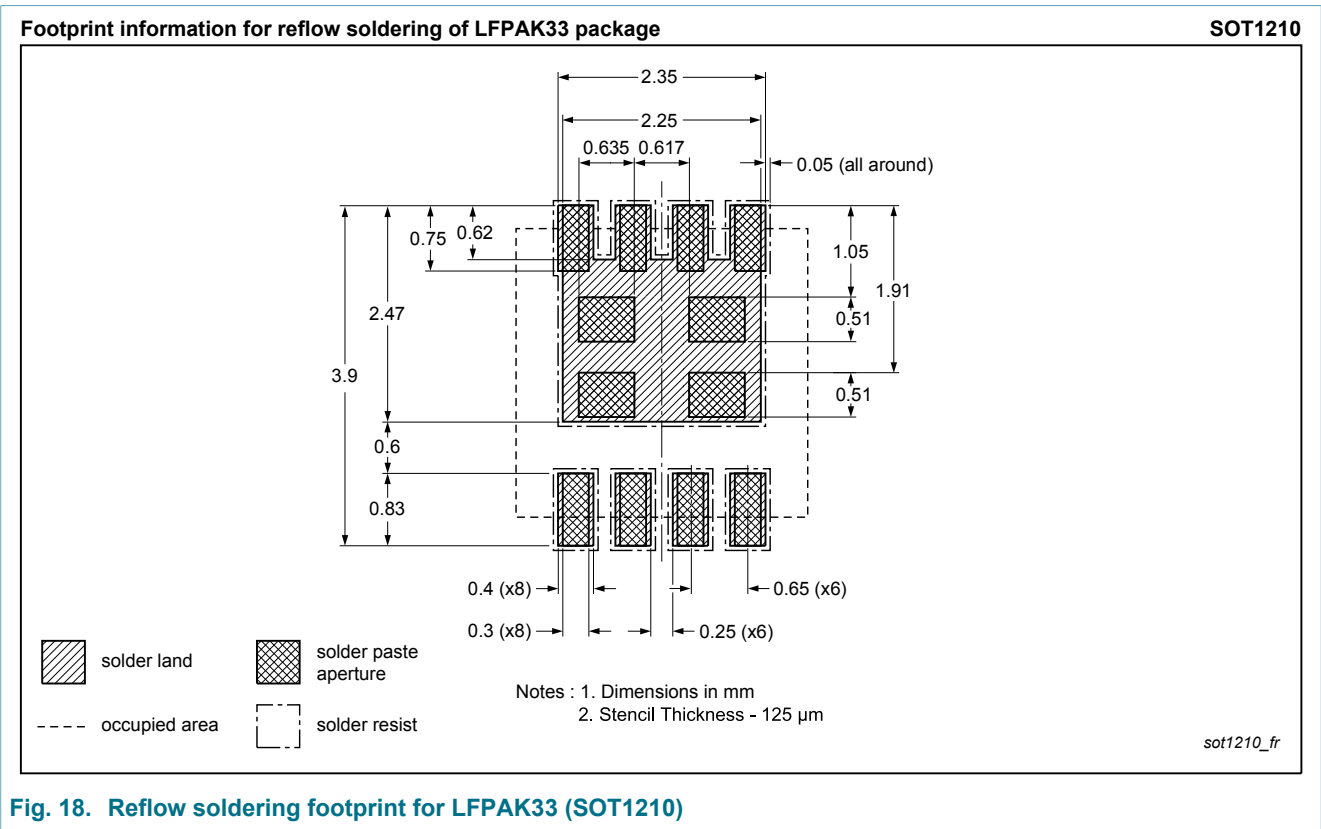


Fig. 18. Reflow soldering footprint for LPAK33 (SOT1210)

## 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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14. Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 2

9. Thermal characteristics..... 4

10. Characteristics.....5

11. Package outline..... 10

12. Soldering..... 11

13. Legal information..... 12

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