# PSMN7R6-60BS



# N-channel 60 V 7.8 m $\Omega$ standard level MOSFET in D2PAK Rev. 2 — 2 March 2012 Product data

Product data sheet

## **Product profile**

## 1.1 General description

Standard level N-channel MOSFET in a D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

## 1.3 Applications

- DC-to-DC converters
- Load switching

- Motor control
- Server power supplies

#### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	-	60	V
I <sub>D</sub>	drain current	$T_{mb}$ = 25 °C; $V_{GS}$ = 10 V; see <u>Figure 1</u>	-	-	92	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	-	149	W
Tj	junction temperature		-55	-	175	°C
Static charact	eristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $T_j = 25 \text{ °C}$ ; see Figure 13; see Figure 9	-	5.9	7.8	mΩ
Dynamic char	acteristics					
$Q_{GD}$	gate-drain charge	$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $V_{DS} = 30 \text{ V}$ ; see <u>Figure 15</u> ; see <u>Figure 14</u>	-	10.6	-	nC
Q <sub>G(tot)</sub>	total gate charge	$V_{GS} = 10 \text{ V}$ ; $I_D = 25 \text{ A}$ ; $V_{DS} = 30 \text{ V}$ ; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	38.7	-	nC
Avalanche rug	gedness					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_D$ = 92 A; $V_{sup}$ ≤ 100 V; $R_{GS}$ = 50 $\Omega$ ; unclamped	-	-	110	mJ



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		_
2	D	drain[1]	mb	B
3	S	source		
mb	D	mounting base; connected to drain	1 3	mbb076 S
			SOT404 (D2PAK)	

<sup>[1]</sup> It is not possible to make connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN7R6-60BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C	-	60	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	60	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 100 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	-	65	Α
		$V_{GS} = 10 \text{ V}; T_{mb} = 25 \text{ °C}; \text{ see } \frac{\text{Figure 1}}{\text{Model}}$	-	92	Α
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$ ; see Figure 3	-	389	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <u>Figure 2</u>	-	149	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature		-	260	°C
Source-drain	diode				
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	-	92	Α
I <sub>SM</sub>	peak source current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 \text{ °C}$	-	389	Α
Avalanche ru	ggedness				
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	$V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; $I_{D}$ = 92 A; $V_{sup}$ ≤ 100 V; $R_{GS}$ = 50 Ω; unclamped	-	110	mJ

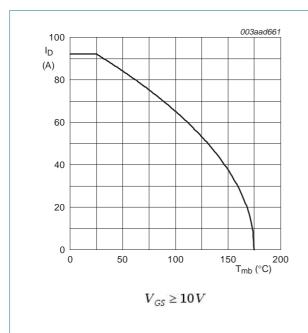


Fig 1. Continuous drain current as a function of mounting base temperature

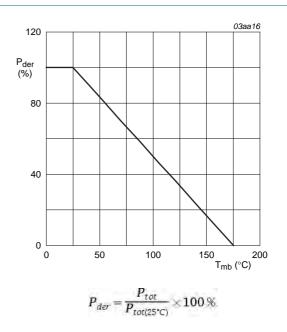
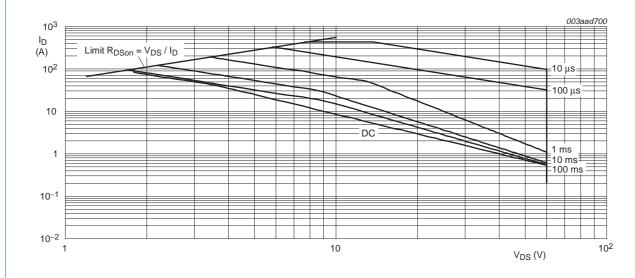


Fig 2. Normalized total power dissipation as a function of mounting base temperature



 $T_{mb} = 25 \,^{\circ}C; I_{DM}$  is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.49	1.01	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

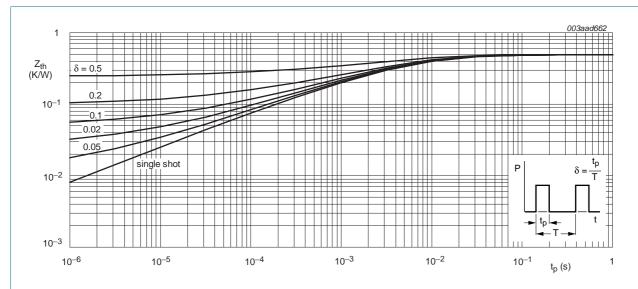


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

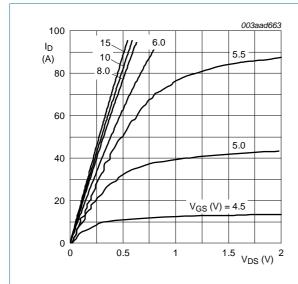
## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics					
V <sub>(BR)DSS</sub> drain-source		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	54	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ °C}$ ; see <u>Figure 10</u> ; see <u>Figure 11</u>	2	3	4	V
$V_{GSth}$	gate-source threshold voltage	$I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$ ; $T_j$ = 175 °C; see <u>Figure 11</u>	1	-	-	V
		$I_D = 1$ mA; $V_{DS} = V_{GS}$ ; $T_j = -55$ °C; see <u>Figure 11</u>	-	-	4.6	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	0.05	10	μΑ
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 ^{\circ}\text{C}$	-	-	100	μΑ
lgss	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nΑ
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	2	100	nA
Doon	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 ^{\circ}\text{C};$ see Figure 12	-	13.3	18	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; see <u>Figure 13</u> ; see <u>Figure 9</u>	-	5.9	7.8	mΩ
$R_G$	gate resistance	f = 1 MHz	-	0.98	-	Ω
Dynamic c	haracteristics					
Q <sub>G(tot)</sub>	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 30 \text{ V}; V_{GS} = 10 \text{ V};$	-	38.7	-	nC
Q <sub>GS</sub>	gate-source charge	see Figure 14; see Figure 15	-	12.9	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	6.9	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	6	-	nC
$Q_{GD}$	gate-drain charge	$I_D$ = 25 A; $V_{DS}$ = 30 V; $V_{GS}$ = 10 V; see <u>Figure 15</u> ; see <u>Figure 14</u>	-	10.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}$ ; $V_{DS} = 30 \text{ V}$ ; see <u>Figure 14</u> ; see <u>Figure 15</u>	-	5.6	-	V
C <sub>iss</sub>	input capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 16}}{\text{Figure 8}}; \text{ see } \frac{\text{Figure 8}}{\text{Figure 16}}$	-	2651	-	pF
C <sub>oss</sub>	output capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 16}}{\text{ MHz}}$	-	342	-	pF
C <sub>rss</sub>	reverse transfer capacitance	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure 16}}{\text{Figure 8}}; \text{ see } \frac{\text{Figure 8}}{\text{Figure 8}}$	-	183	-	pF
d(on)	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega; V_{GS} = 10 \text{ V};$	-	19	-	ns
r	rise time	$R_{G(ext)} = 4.7 \Omega$	-	21	-	ns
d(off)	turn-off delay time		-	37	-	ns
t <sub>f</sub>	fall time		-	13	-	ns

 Table 6.
 Characteristics ... continued

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Source-drai	n diode					
V <sub>SD</sub>	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C};$ see <u>Figure 17</u>	-	0.86	1.2	V
t <sub>rr</sub>	reverse recovery time	$I_S = 25 \text{ A}$ ; $dI_S/dt = 100 \text{ A/}\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ;	-	40.4	-	ns
Q <sub>r</sub>	recovered charge	$V_{DS} = 30 \text{ V}$	-	56	-	nC



 $T_i = 25$  °C;  $t_p = 300 \, \mu s$ 

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

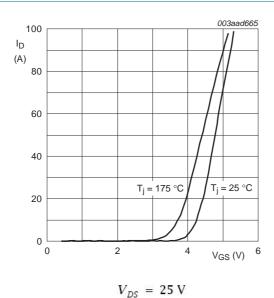


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

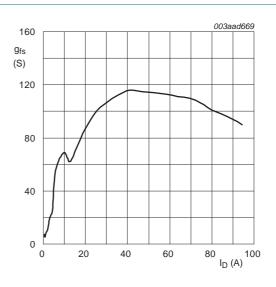
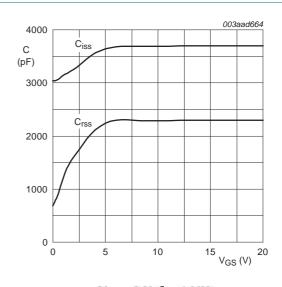


Fig 6. Forward transconductance as a function of drain current; typical values



 $V_{DS} = 0 \text{ V; } f = 1 \text{ MHz}$ 

Fig 8. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

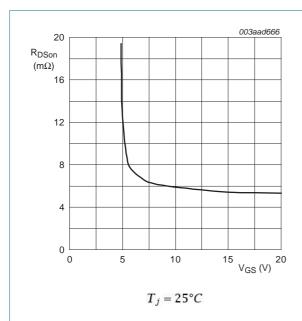


Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

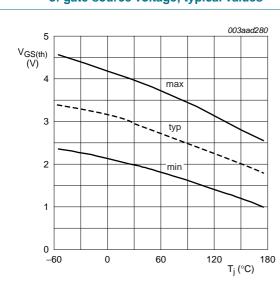
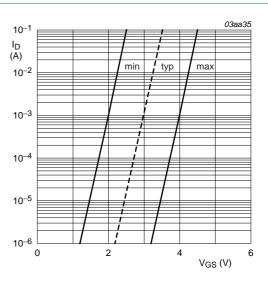


Fig 11. Gate-source threshold voltage as a function of junction temperature

 $I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$ 



 $T_j = 25 \,^{\circ}C; V_{DS} = 5V$ 

Fig 10. Sub-threshold drain current as a function of gate-source voltage

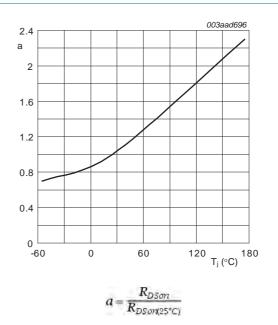


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

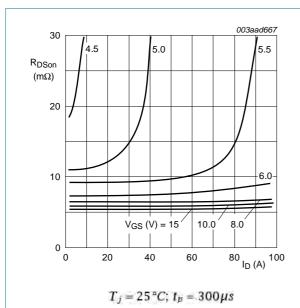
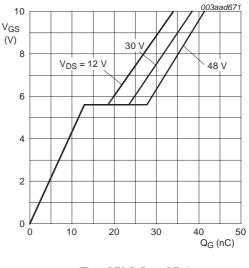


Fig 13. Drain-source on-state resistance as a function of drain current; typical values



$$T_j = 25^{\circ}C; I_D = 25 A$$

Fig 14. Gate-source voltage as a function of gate charge; typical values

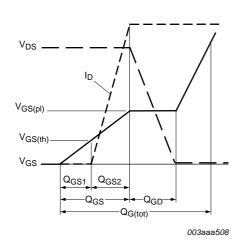
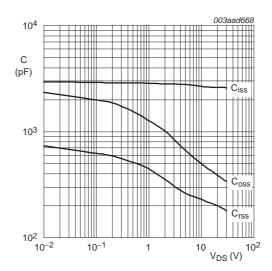


Fig 15. Gate charge waveform definitions



 $V_{DS} = 0V$ ; f = 1 MHz

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

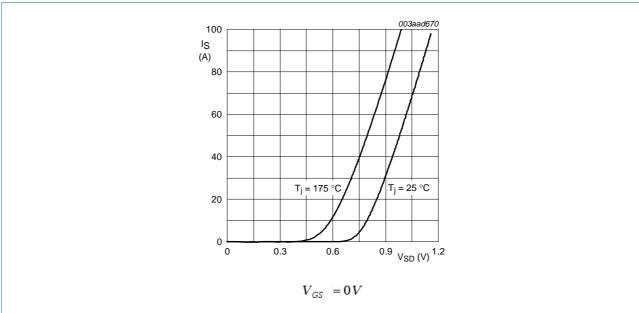


Fig 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

## 7. Package outline

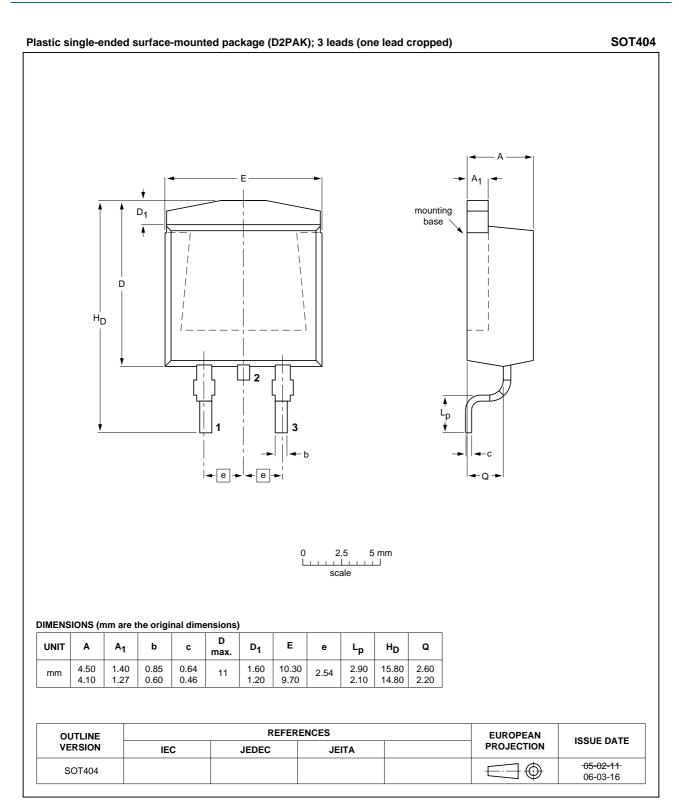


Fig 18. Package outline SOT404 (D2PAK)

## 8. Revision history

## Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN7R6-60BS v.2	20120302	Product data sheet	-	PSMN7R6-60BS v.1
Modifications:	<ul><li>Status changed f</li><li>Various changes</li></ul>	rom objective to product.		
PSMN7R6-60BS v.1	20111020	Objective data sheet	-	-

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#### 9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design
- [2] The term 'short data sheet' is explained in section "Definitions".
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PSMN7R6-60BS

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## PSMN7R6-60BS

#### N-channel 60 V 7.8 mΩ standard level MOSFET in D2PAK

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# PSMN7R6-60BS

## **NXP Semiconductors**

## N-channel 60 V 7.8 mΩ standard level MOSFET in D2PAK

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