



# PSMN8R0-30YLC

N-channel 30 V 7.9 mΩ logic level MOSFET in LPAK using NextPower technology

Rev. 2 — 1 September 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, QOSS for high system efficiencies at low and high loads

### 1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

### 1.4 Quick reference data

Table 1. Quick reference data

| Symbol                        | Parameter                        | Conditions                                                                                           | Min | Typ | Max | Unit |
|-------------------------------|----------------------------------|------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $V_{DS}$                      | drain-source voltage             | $25\text{ °C} \leq T_j \leq 175\text{ °C}$                                                           | -   | -   | 30  | V    |
| $I_D$                         | drain current                    | $T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a>                      | -   | -   | 54  | A    |
| $P_{tot}$                     | total power dissipation          | $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>                                               | -   | -   | 42  | W    |
| $T_j$                         | junction temperature             |                                                                                                      | -55 | -   | 175 | °C   |
| <b>Static characteristics</b> |                                  |                                                                                                      |     |     |     |      |
| $R_{DS(on)}$                  | drain-source on-state resistance | $V_{GS} = 4.5\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> | -   | 8.5 | 10  | mΩ   |
|                               |                                  | $V_{GS} = 10\text{ V}$ ; $I_D = 15\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a>  | -   | 6.7 | 7.9 | mΩ   |

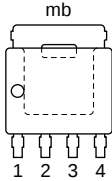
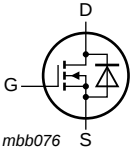


Table 1. Quick reference data ...continued

| Symbol                  | Parameter         | Conditions                                                                                                                                   | Min | Typ | Max | Unit |
|-------------------------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| Dynamic characteristics |                   |                                                                                                                                              |     |     |     |      |
| $Q_{GD}$                | gate-drain charge | $V_{GS} = 4.5\text{ V}$ ; $I_D = 15\text{ A}$ ;<br>$V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 14</a> ;<br>see <a href="#">Figure 15</a> | -   | 2.3 | -   | nC   |
| $Q_{G(tot)}$            | total gate charge | $V_{GS} = 4.5\text{ V}$ ; $I_D = 15\text{ A}$ ;<br>$V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 14</a> ;<br>see <a href="#">Figure 15</a> | -   | 7   | -   | nC   |

2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                          | Simplified outline                                                                 | Graphic symbol                                                                       |
|-----|--------|--------------------------------------|------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 1   | S      | source                               |  |  |
| 2   | S      | source                               |                                                                                    |                                                                                      |
| 3   | S      | source                               |                                                                                    |                                                                                      |
| 4   | G      | gate                                 |                                                                                    |                                                                                      |
| mb  | D      | mounting base;<br>connected to drain |                                                                                    |                                                                                      |
|     |        |                                      | SOT669 (LPAK;<br>Power-SO8)                                                        |                                                                                      |

3. Ordering information

Table 3. Ordering information

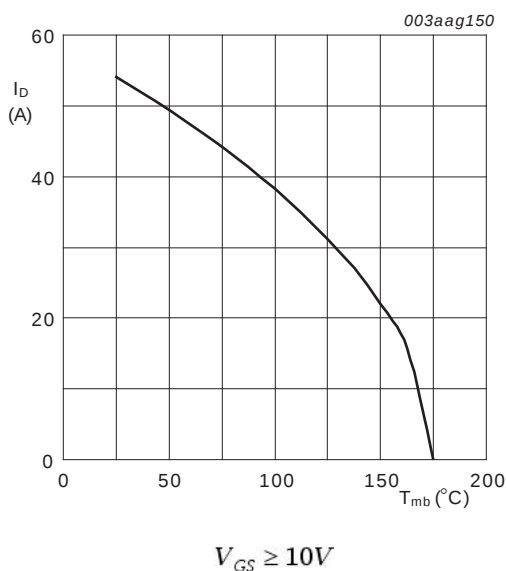
| Type number   | Package            |                                                       | Version |
|---------------|--------------------|-------------------------------------------------------|---------|
|               | Name               | Description                                           |         |
| PSMN8R0-30YLC | LPAK;<br>Power-SO8 | plastic single-ended surface-mounted package; 4 leads | SOT669  |

## 4. Limiting values

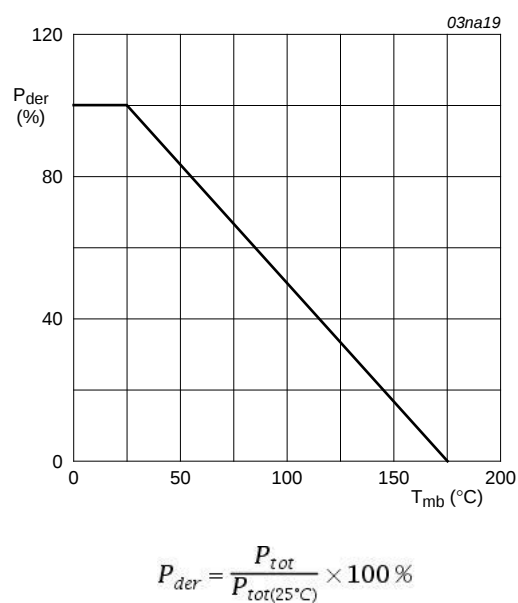
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                    | Conditions                                                                                                                                                                              | Min | Max | Unit |
|-----------------------------|----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------|
| $V_{DS}$                    | drain-source voltage                         | $25\text{ °C} \leq T_j \leq 175\text{ °C}$                                                                                                                                              | -   | 30  | V    |
| $V_{DGR}$                   | drain-gate voltage                           | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$                                                                                                               | -   | 30  | V    |
| $V_{GS}$                    | gate-source voltage                          |                                                                                                                                                                                         | -20 | 20  | V    |
| $I_D$                       | drain current                                | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>                                                                                                         | -   | 54  | A    |
|                             |                                              | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>                                                                                                        | -   | 38  | A    |
| $I_{DM}$                    | peak drain current                           | pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 4</a>                                                                                       | -   | 216 | A    |
| $P_{tot}$                   | total power dissipation                      | $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>                                                                                                                                  | -   | 42  | W    |
| $T_{stg}$                   | storage temperature                          |                                                                                                                                                                                         | -55 | 175 | °C   |
| $T_j$                       | junction temperature                         |                                                                                                                                                                                         | -55 | 175 | °C   |
| $T_{sld(M)}$                | peak soldering temperature                   |                                                                                                                                                                                         | -   | 260 | °C   |
| $V_{ESD}$                   | electrostatic discharge voltage              | MM (JEDEC JESD22-A115)                                                                                                                                                                  | 190 | -   | V    |
| <b>Source-drain diode</b>   |                                              |                                                                                                                                                                                         |     |     |      |
| $I_S$                       | source current                               | $T_{mb} = 25\text{ °C}$                                                                                                                                                                 | -   | 38  | A    |
| $I_{SM}$                    | peak source current                          | pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$                                                                                                                      | -   | 216 | A    |
| <b>Avalanche ruggedness</b> |                                              |                                                                                                                                                                                         |     |     |      |
| $E_{DS(AL)S}$               | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 54\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; unclamped; see <a href="#">Figure 3</a> | -   | 12  | mJ   |



**Fig 1. Continuous drain current as a function of mounting base temperature**



**Fig 2. Normalized total power dissipation as a function of mounting base temperature**

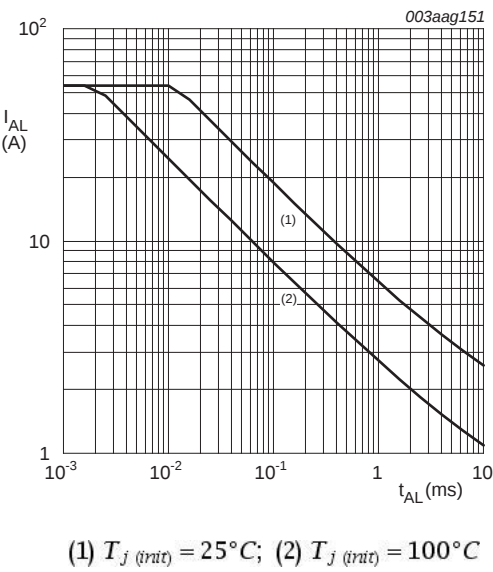


Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

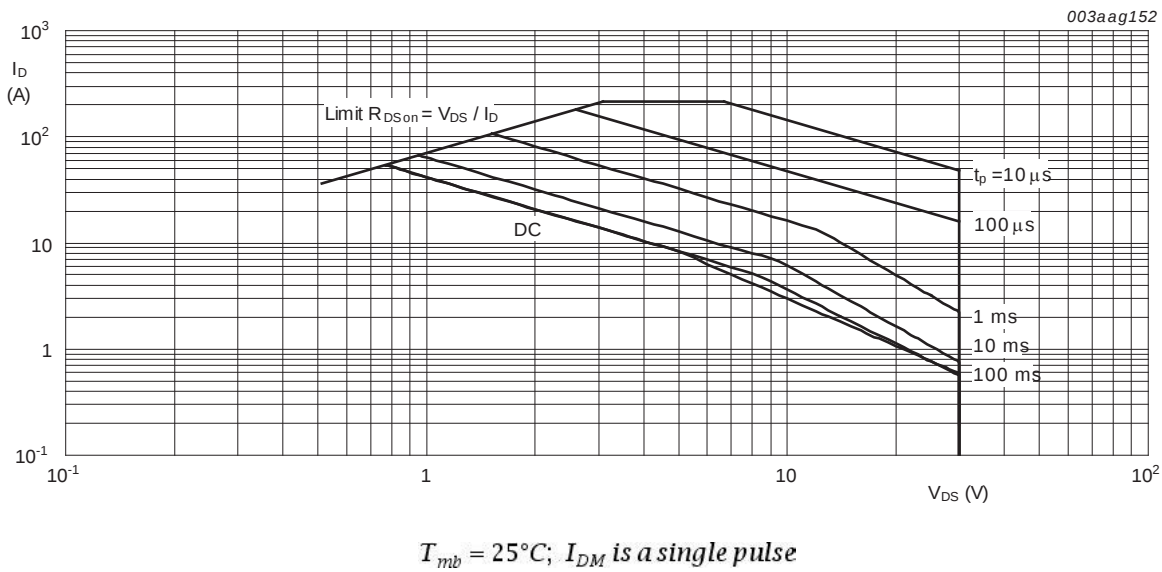
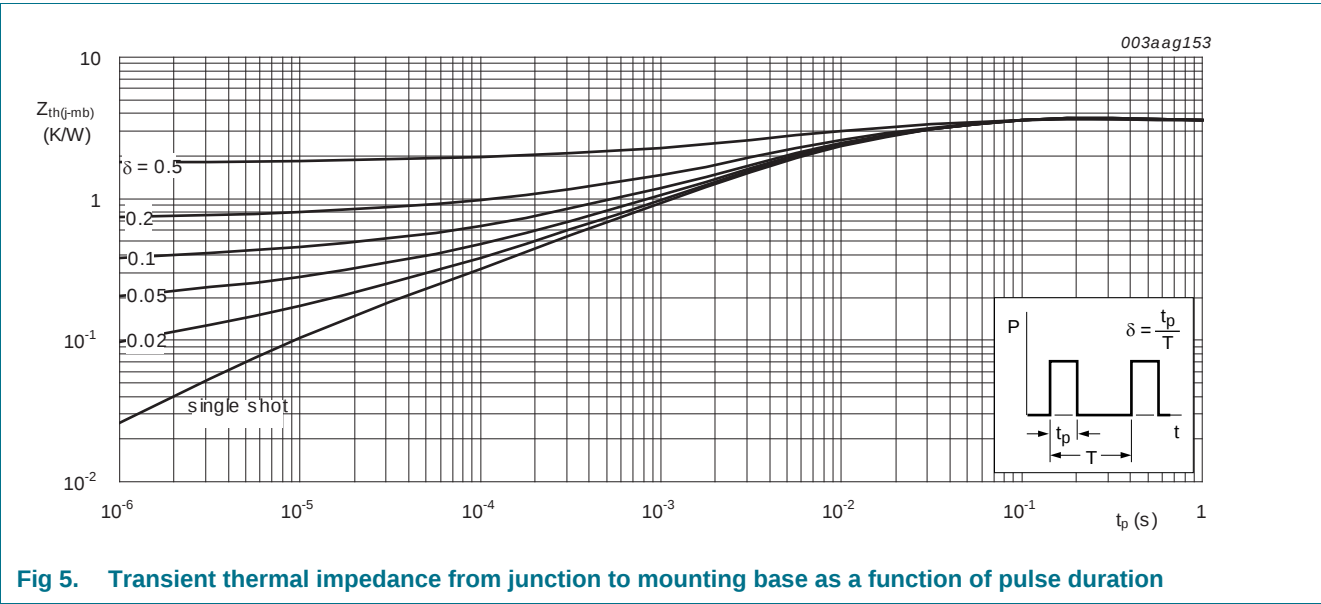


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

| Symbol         | Parameter                                         | Conditions                   | Min | Typ  | Max  | Unit |
|----------------|---------------------------------------------------|------------------------------|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 5</a> | -   | 3.38 | 3.61 | K/W  |



## 6. Characteristics

Table 6. Characteristics

| Symbol                         | Parameter                         | Conditions                                                                                                                                    | Min  | Typ  | Max  | Unit          |
|--------------------------------|-----------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| <b>Static characteristics</b>  |                                   |                                                                                                                                               |      |      |      |               |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage    | $I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$                                                                | 30   | -    | -    | V             |
|                                |                                   | $I_D = 250\ \mu\text{A}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = -55\ ^\circ\text{C}$                                                               | 27   | -    | -    | V             |
| $V_{GS(th)}$                   | gate-source threshold voltage     | $I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25\ ^\circ\text{C}$ ; see <a href="#">Figure 10</a>                                         | 1.05 | 1.59 | 1.95 | V             |
|                                |                                   | $I_D = 10\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 150\ ^\circ\text{C}$ ; see <a href="#">Figure 11</a>                                       | 0.5  | -    | -    | V             |
|                                |                                   | $I_D = 1\ \text{mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55\ ^\circ\text{C}$ ; see <a href="#">Figure 11</a>                                        | -    | -    | 2.25 | V             |
| $I_{DSS}$                      | drain leakage current             | $V_{DS} = 30\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$                                                                 | -    | -    | 1    | $\mu\text{A}$ |
|                                |                                   | $V_{DS} = 30\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ ; $T_j = 150\ ^\circ\text{C}$                                                                | -    | -    | 100  | $\mu\text{A}$ |
| $I_{GSS}$                      | gate leakage current              | $V_{GS} = 16\ \text{V}$ ; $V_{DS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$                                                                 | -    | -    | 100  | nA            |
|                                |                                   | $V_{GS} = -16\ \text{V}$ ; $V_{DS} = 0\ \text{V}$ ; $T_j = 25\ ^\circ\text{C}$                                                                | -    | -    | 100  | nA            |
| $R_{DS(on)}$                   | drain-source on-state resistance  | $V_{GS} = 4.5\ \text{V}$ ; $I_D = 15\ \text{A}$ ; $T_j = 25\ ^\circ\text{C}$ ; see <a href="#">Figure 12</a>                                  | -    | 8.5  | 10   | mΩ            |
|                                |                                   | $V_{GS} = 4.5\ \text{V}$ ; $I_D = 15\ \text{A}$ ; $T_j = 150\ ^\circ\text{C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a> | -    | -    | 16.6 | mΩ            |
|                                |                                   | $V_{GS} = 10\ \text{V}$ ; $I_D = 15\ \text{A}$ ; $T_j = 25\ ^\circ\text{C}$ ; see <a href="#">Figure 12</a>                                   | -    | 6.7  | 7.9  | mΩ            |
|                                |                                   | $V_{GS} = 10\ \text{V}$ ; $I_D = 15\ \text{A}$ ; $T_j = 150\ ^\circ\text{C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>  | -    | -    | 13.2 | mΩ            |
| $R_G$                          | gate resistance                   | $f = 1\ \text{MHz}$                                                                                                                           | -    | 2.2  | 4.4  | Ω             |
| <b>Dynamic characteristics</b> |                                   |                                                                                                                                               |      |      |      |               |
| $Q_{G(tot)}$                   | total gate charge                 | $I_D = 15\ \text{A}$ ; $V_{DS} = 15\ \text{V}$ ; $V_{GS} = 10\ \text{V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>      | -    | 15   | -    | nC            |
|                                |                                   | $I_D = 15\ \text{A}$ ; $V_{DS} = 15\ \text{V}$ ; $V_{GS} = 4.5\ \text{V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>     | -    | 7    | -    | nC            |
|                                |                                   | $I_D = 0\ \text{A}$ ; $V_{DS} = 0\ \text{V}$ ; $V_{GS} = 10\ \text{V}$                                                                        | -    | 13   | -    | nC            |
| $Q_{GS}$                       | gate-source charge                | $I_D = 15\ \text{A}$ ; $V_{DS} = 15\ \text{V}$ ; $V_{GS} = 4.5\ \text{V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>     | -    | 2.1  | -    | nC            |
| $Q_{GS(th)}$                   | pre-threshold gate-source charge  |                                                                                                                                               | -    | 1.5  | -    | nC            |
| $Q_{GS(th-pl)}$                | post-threshold gate-source charge |                                                                                                                                               | -    | 0.6  | -    | nC            |
| $Q_{GD}$                       | gate-drain charge                 |                                                                                                                                               | -    | 2.3  | -    | nC            |
| $V_{GS(pl)}$                   | gate-source plateau voltage       | $I_D = 15\ \text{A}$ ; $V_{DS} = 15\ \text{V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>                                | -    | 2.6  | -    | V             |
| $C_{iss}$                      | input capacitance                 | $V_{DS} = 15\ \text{V}$ ; $V_{GS} = 0\ \text{V}$ ; $f = 1\ \text{MHz}$ ; $T_j = 25\ ^\circ\text{C}$ ; see <a href="#">Figure 16</a>           | -    | 848  | -    | pF            |
| $C_{oss}$                      | output capacitance                |                                                                                                                                               | -    | 207  | -    | pF            |
| $C_{rss}$                      | reverse transfer capacitance      |                                                                                                                                               | -    | 70   | -    | pF            |

Table 6. Characteristics ...continued

| Symbol       | Parameter           | Conditions                                                                                                | Min | Typ | Max | Unit |
|--------------|---------------------|-----------------------------------------------------------------------------------------------------------|-----|-----|-----|------|
| $t_{d(on)}$  | turn-on delay time  | $V_{DS} = 15\text{ V}; R_L = 1\text{ }\Omega; V_{GS} = 4.5\text{ V};$<br>$R_{G(ext)} = 4.7\text{ }\Omega$ | -   | 15  | -   | ns   |
| $t_r$        | rise time           |                                                                                                           | -   | 11  | -   | ns   |
| $t_{d(off)}$ | turn-off delay time |                                                                                                           | -   | 19  | -   | ns   |
| $t_f$        | fall time           |                                                                                                           | -   | 7   | -   | ns   |
| $Q_{oss}$    | output charge       | $V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz};$<br>$T_j = 25\text{ }^\circ\text{C}$        | -   | 5   | -   | nC   |

Source-drain diode

|          |                            |                                                                                                                                         |   |      |     |    |
|----------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|---|------|-----|----|
| $V_{SD}$ | source-drain voltage       | $I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$<br>see <a href="#">Figure 17</a>                              | - | 0.85 | 1.1 | V  |
| $t_{rr}$ | reverse recovery time      | $I_S = 15\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$<br>$V_{DS} = 15\text{ V}$                                | - | 21   | -   | ns |
| $Q_r$    | recovered charge           |                                                                                                                                         | - | 13   | -   | nC |
| $t_a$    | reverse recovery rise time | $V_{GS} = 0\text{ V}; I_S = 15\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s};$<br>$V_{DS} = 15\text{ V};$ see <a href="#">Figure 18</a> | - | 12   | -   | ns |
| $t_b$    | reverse recovery fall time |                                                                                                                                         | - | 9    | -   | ns |

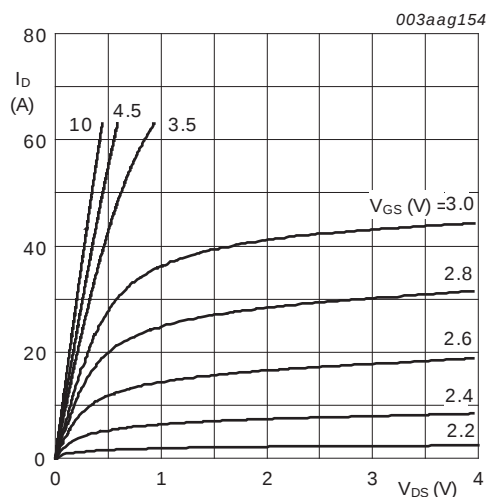


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

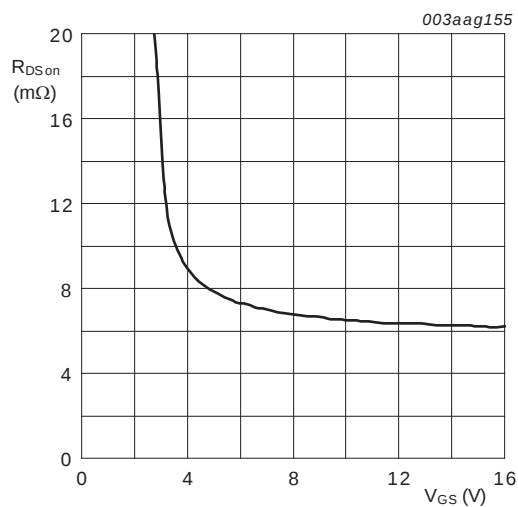


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

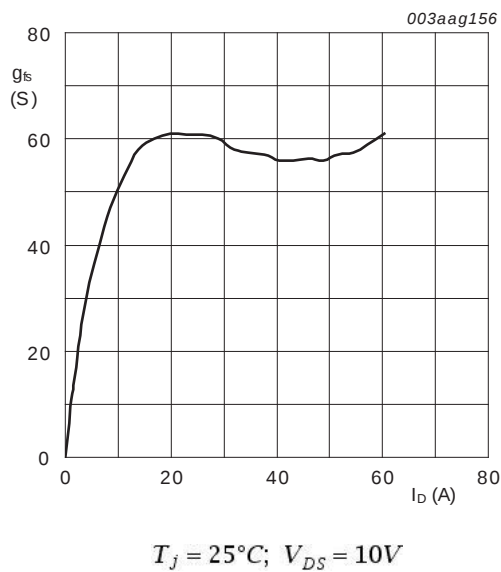


Fig 8. Forward transconductance as a function of drain current; typical values

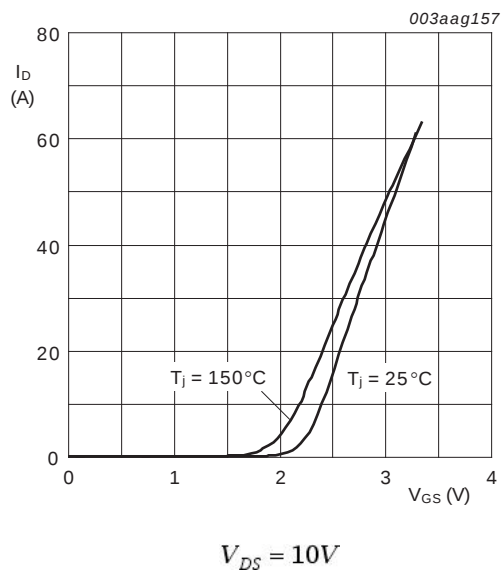


Fig 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

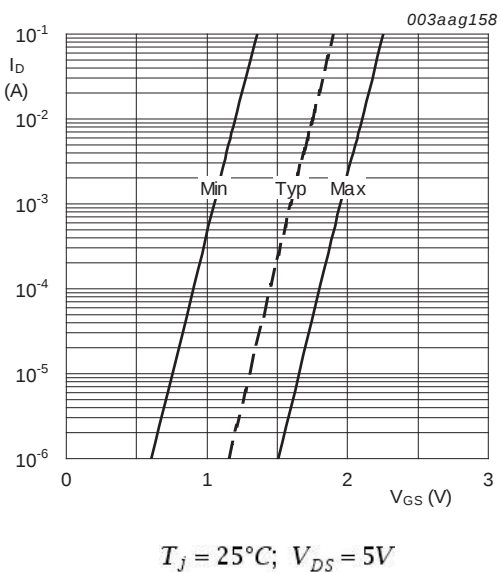


Fig 10. Sub-threshold drain current as a function of gate-source voltage

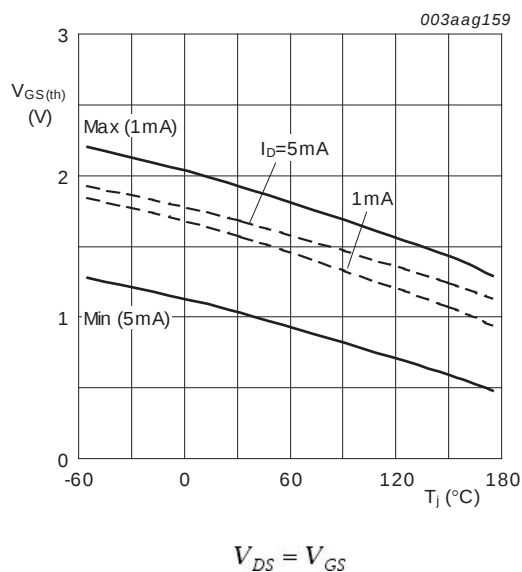
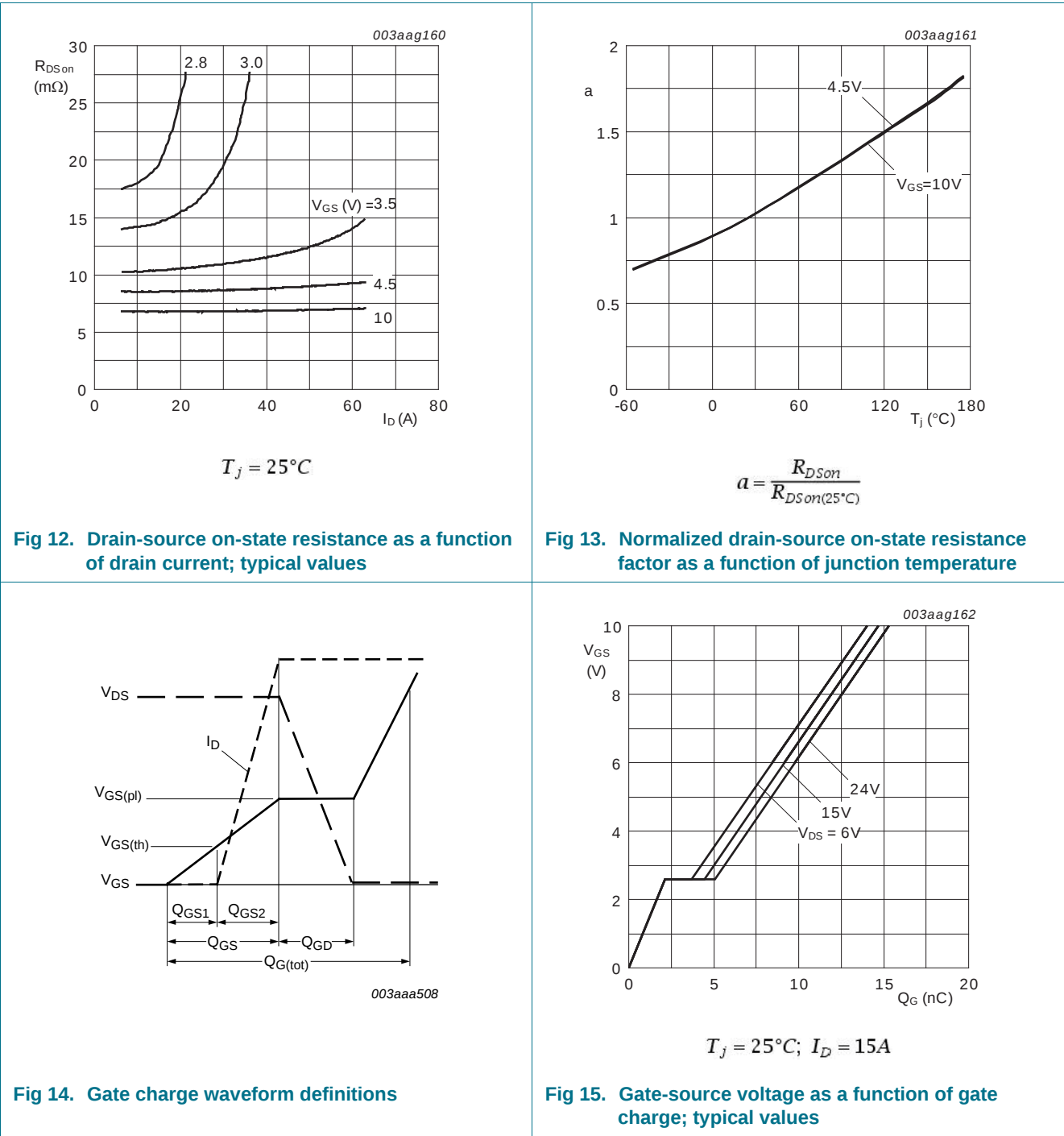
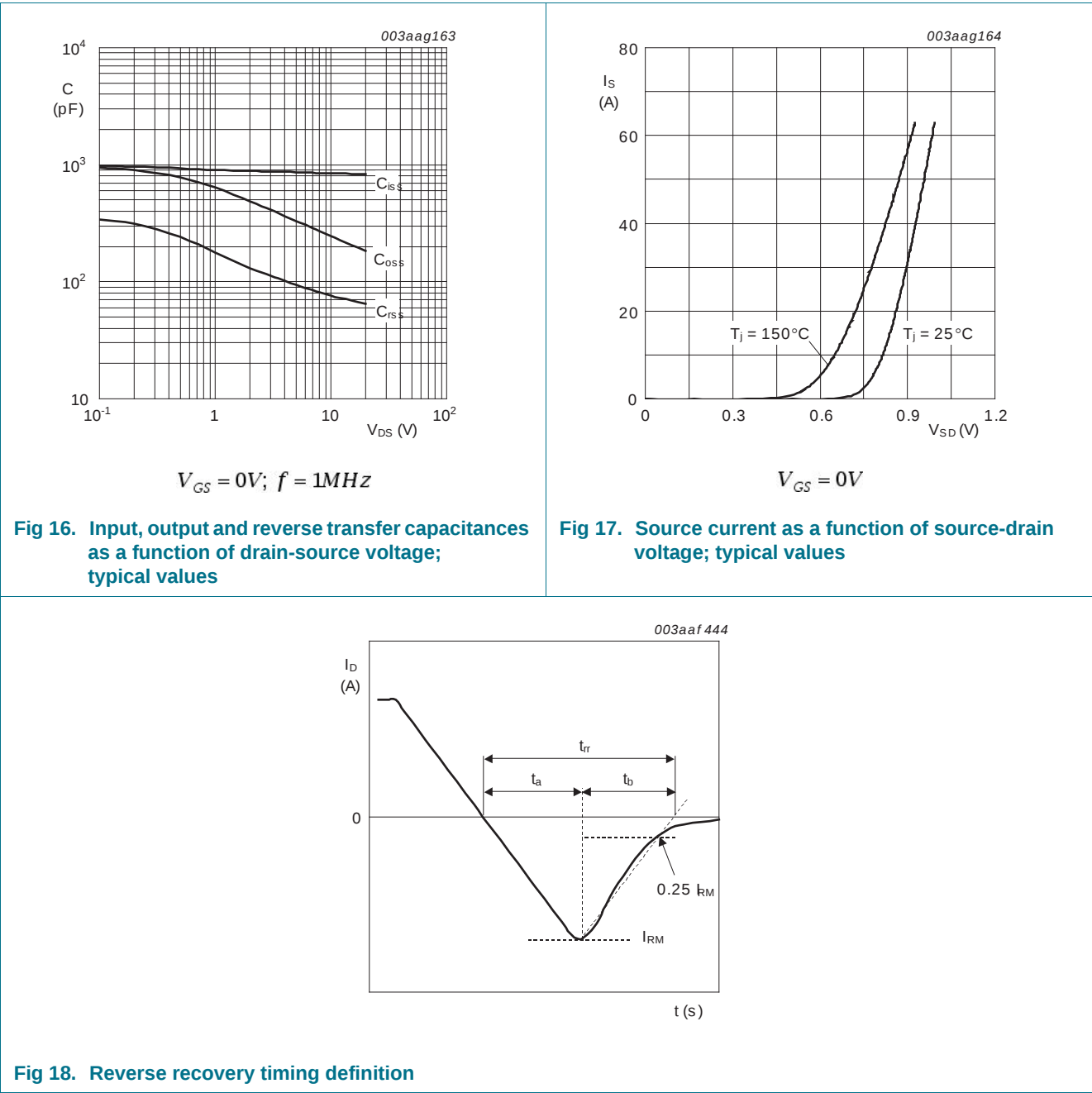


Fig 11. Gate-source threshold voltage as a function of junction temperature





7. Package outline

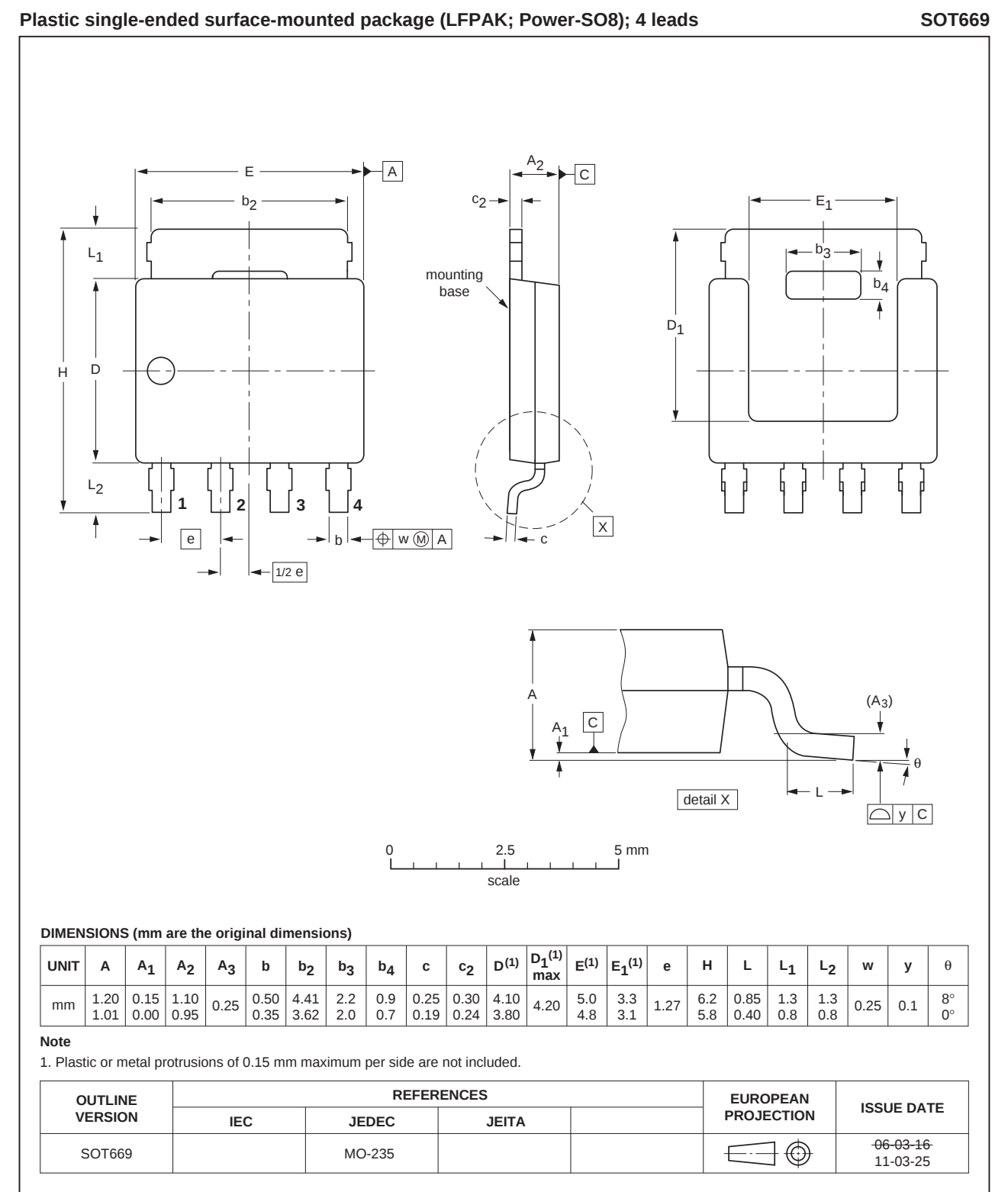


Fig 19. Package outline SOT669 (LPAK; Power-SO8)

8. Revision history

Table 7. Revision history

| Document ID       | Release date                                           | Data sheet status    | Change notice | Supersedes        |
|-------------------|--------------------------------------------------------|----------------------|---------------|-------------------|
| PSMN8R0-30YLC v.2 | 20110901                                               | Product data sheet   | -             | PSMN8R0-30YLC v.1 |
| Modifications:    | • Data sheet status changed from objective to product. |                      |               |                   |
| PSMN8R0-30YLC v.1 | 20110712                                               | Objective data sheet | -             | -                 |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1]</sup> <sup>[2]</sup> | Product status <sup>[3]</sup> | Definition                                                                            |
|-----------------------------------------------|-------------------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet                  | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet                | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet                    | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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