PSMN8R9-100BSE

N-channel 100 V, 10 mOhm, standard level MOSFET in D2PAK

6 June 2024 Product data sheet

1. General description

SuperSOA N-channel enhancement mode MOSFET in a D2PAK package qualified to 175 °C. PSMN8R9-100BSE delivers low R_{DSon} and very strong linear-mode (SOA) performance, and complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Avalanche rated, 100% tested
- Low R_{DSon} for low I^2R conduction losses
- D2PAK package

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	75	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	-	419	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	296	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	8	10	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	32	45	nC
$Q_{G(tot)}$	total gate charge			-	114	160	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 75 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4		-	-	422	mJ

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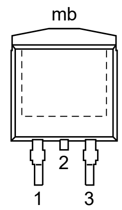
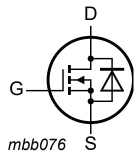
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN8R9-100BSE	D2PAK	plastic, single-ended surface-mounted package (D2PAK); 3 terminals (one lead cropped); 2.54 mm pitch; 11 mm x 10 mm x 4.3 mm body	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN8R9-100BSE	PSMN8R9 100BSE

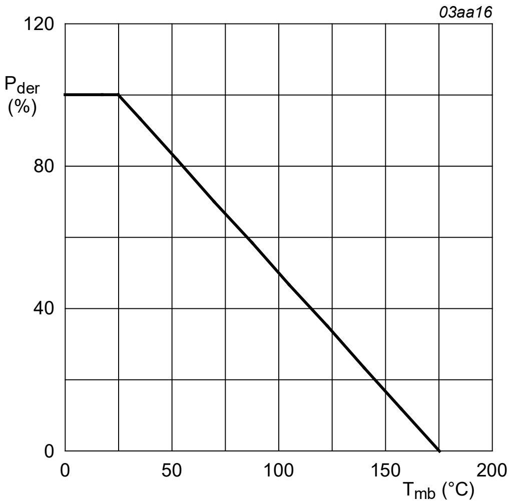
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

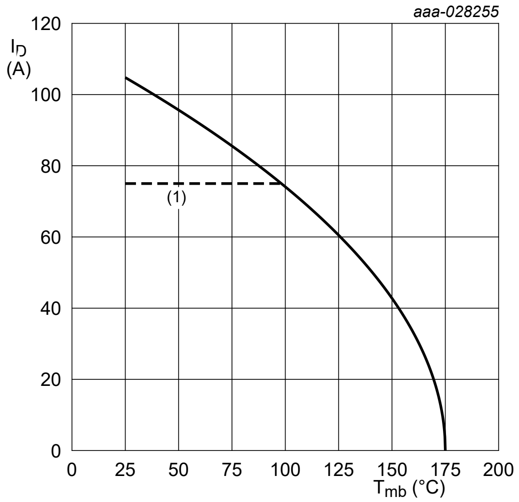
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	296	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	75	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	74	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	419	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	75	A

Symbol	Parameter	Conditions		Min	Max	Unit
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	419	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 75 A; $V_{sup} \leq$ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4		-	422	mJ



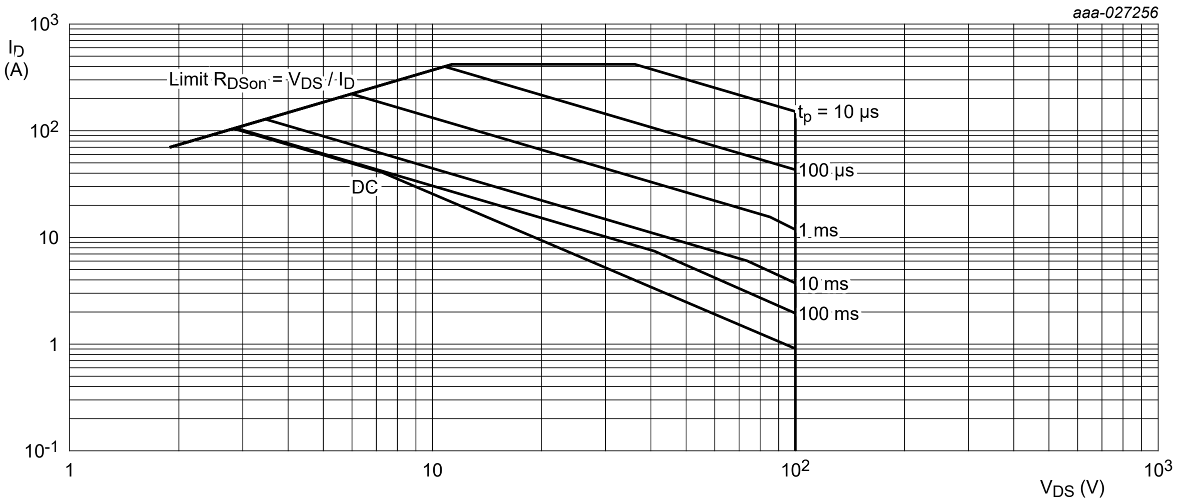
$$P_{der} = \frac{P_{tot}}{P_{tot\,(25\,°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



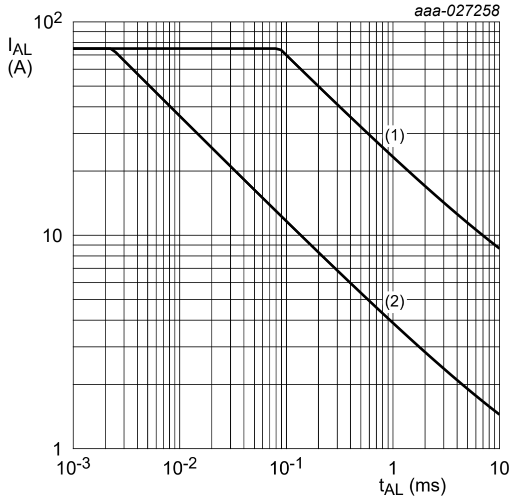
VGS ≥ 10V
1) Capped at 75A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25°C; (2) $T_{j\ (init)}$ = 100°C

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.42	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient			-	50	-	K/W

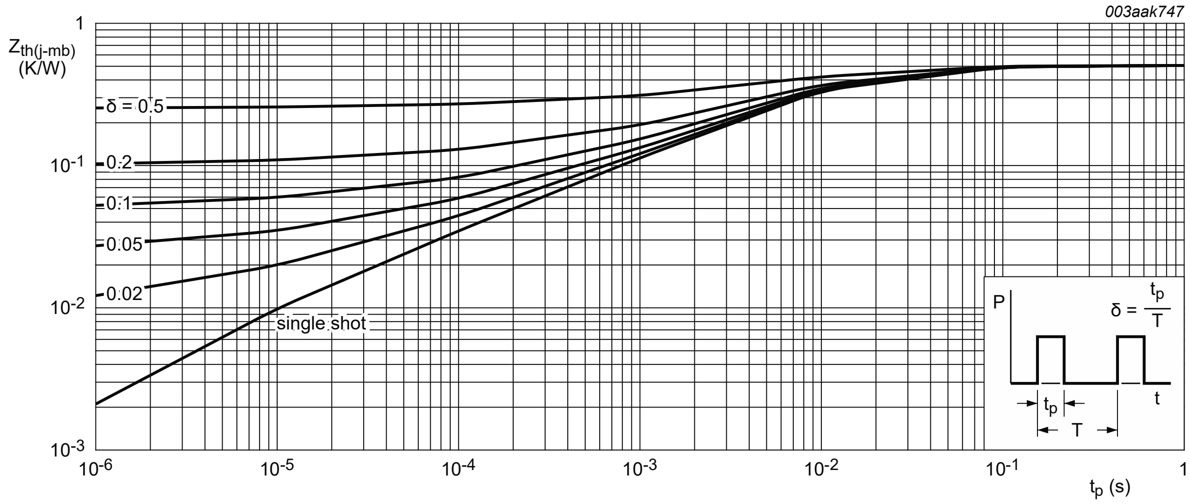


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

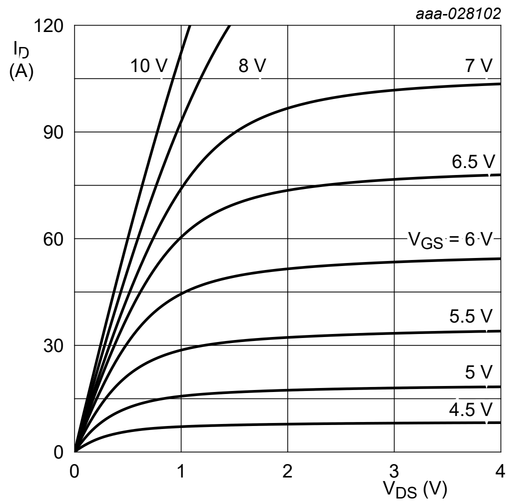
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		1.8	2.7	4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C; Fig. 11		1	-	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C; Fig. 11		-	-	4.6	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.1	2	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		-	8	10	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 13		-	-	18.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 13		-	-	27	mΩ
R_G	gate resistance	f = 1 MHz		0.4	0.8	1.6	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	114	160	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	45	63	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 14; Fig. 15		-	33	46	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	18	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	15	-	nC
Q_{GD}	gate-drain charge			-	32	45	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; Fig. 14; Fig. 15		-	5.3	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	7028	9488	pF
C_{oss}	output capacitance			-	447	603	pF
C_{rss}	reverse transfer capacitance			-	237	332	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	28	42	ns
t_r	rise time			-	52	78	ns
$t_{d(off)}$	turn-off delay time			-	60	90	ns
t_f	fall time			-	44	66	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.83	1.2	V

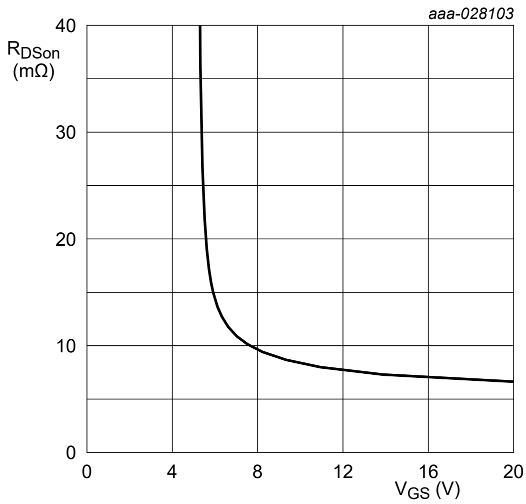
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V		-	77	100	ns
Q_r	recovered charge		[1]	-	248	322	nC

[1] includes capacitive recovery



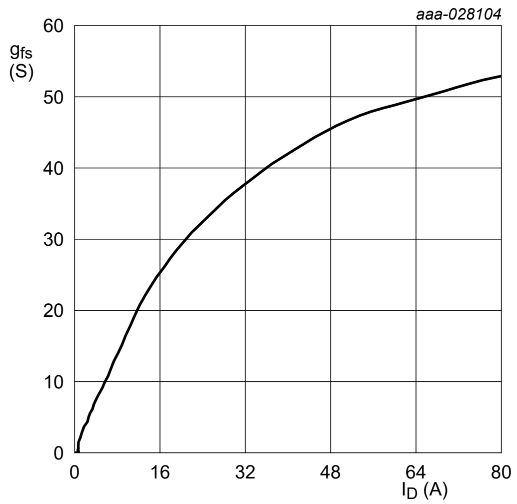
T_j = 25 °C

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values



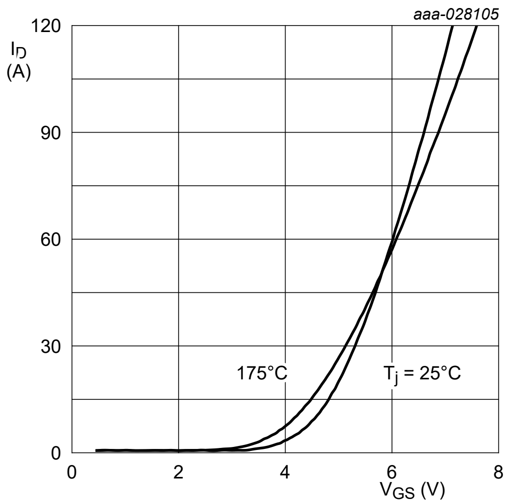
T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



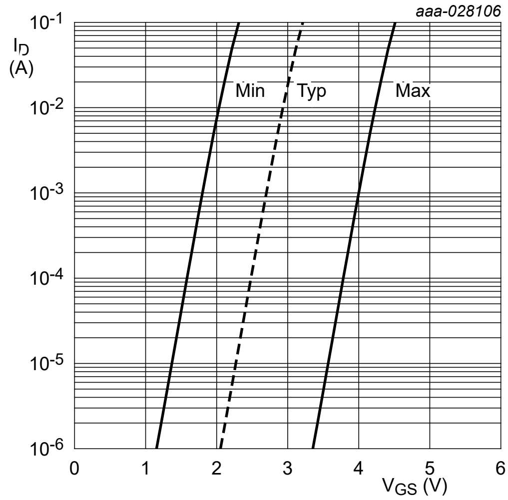
T_j = 25 °C; V_{DS} = 8 V

Fig. 8. Forward transconductance as a function of drain current; typical values



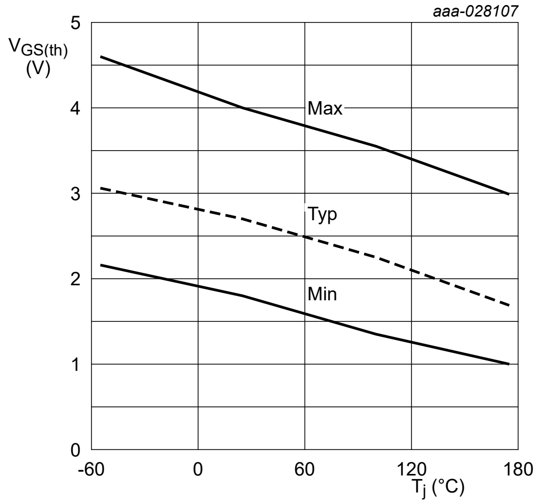
V_{DS} = 8 V

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values



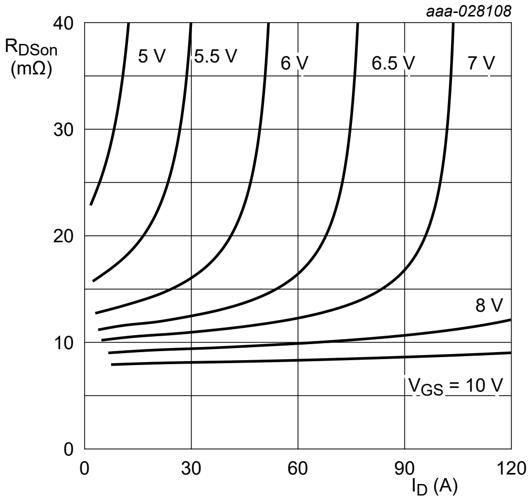
T_j = 25 °C; V_{DS} = 5 V

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



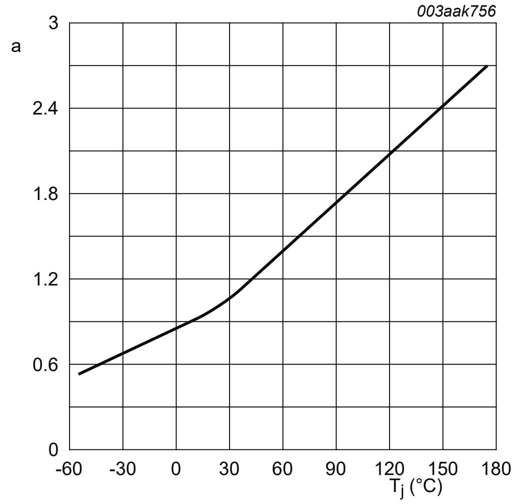
I_D = 1 mA ; V_{DS} = V_{GS}

Fig. 11. Gate-source threshold voltage as a function of junction temperature



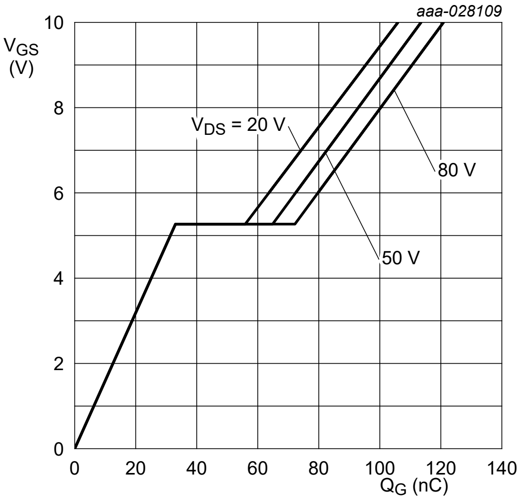
T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25°C)}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

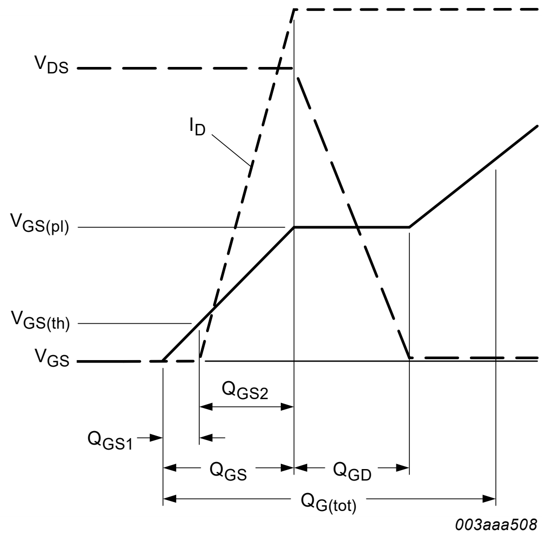
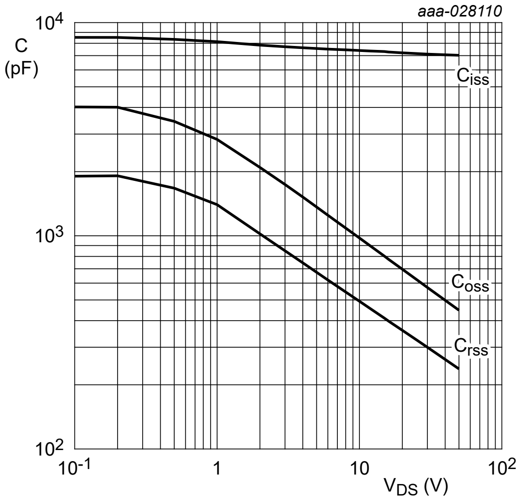
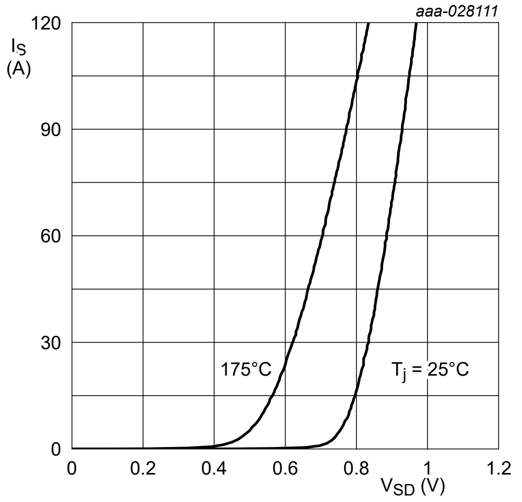


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

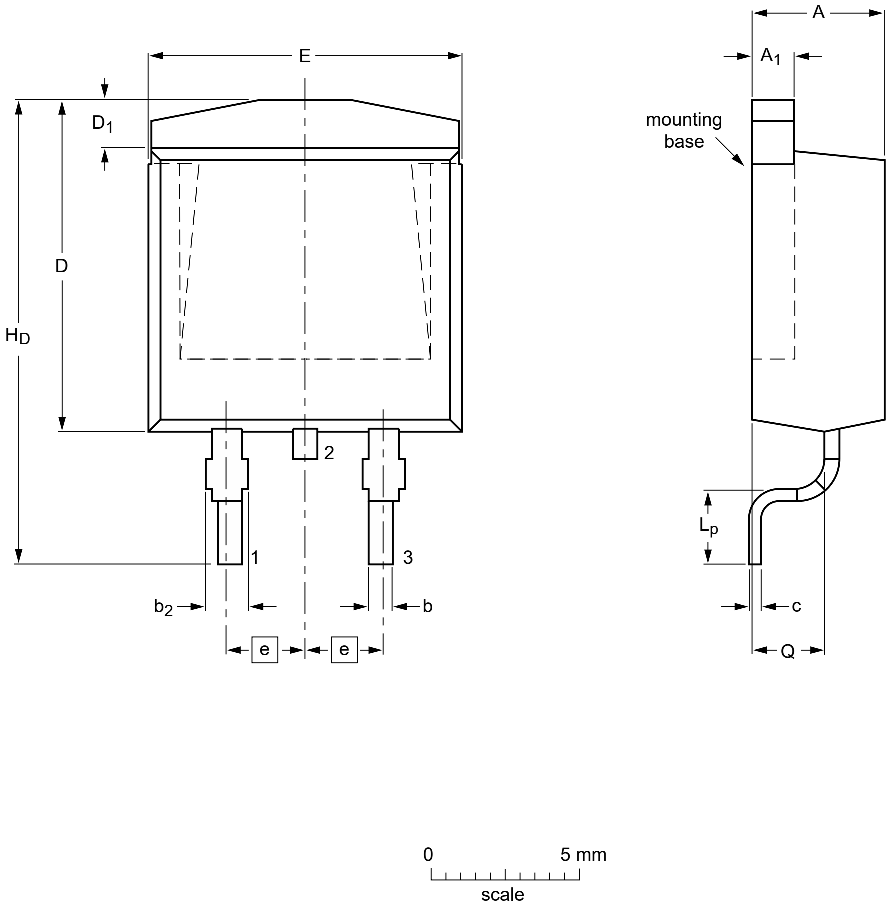


V_{GS} = 0 V

Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_2	c	D	D_1	E	e	H_D	L_p	Q
mm	max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
	nom									2.54			
	min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

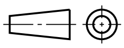
Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT404						~~06-03-16~~ 13-02-25

Fig. 18. Package outline D2PAK (SOT404)

12. Soldering

Footprint information for reflow soldering of D2PAK package **SOT404**

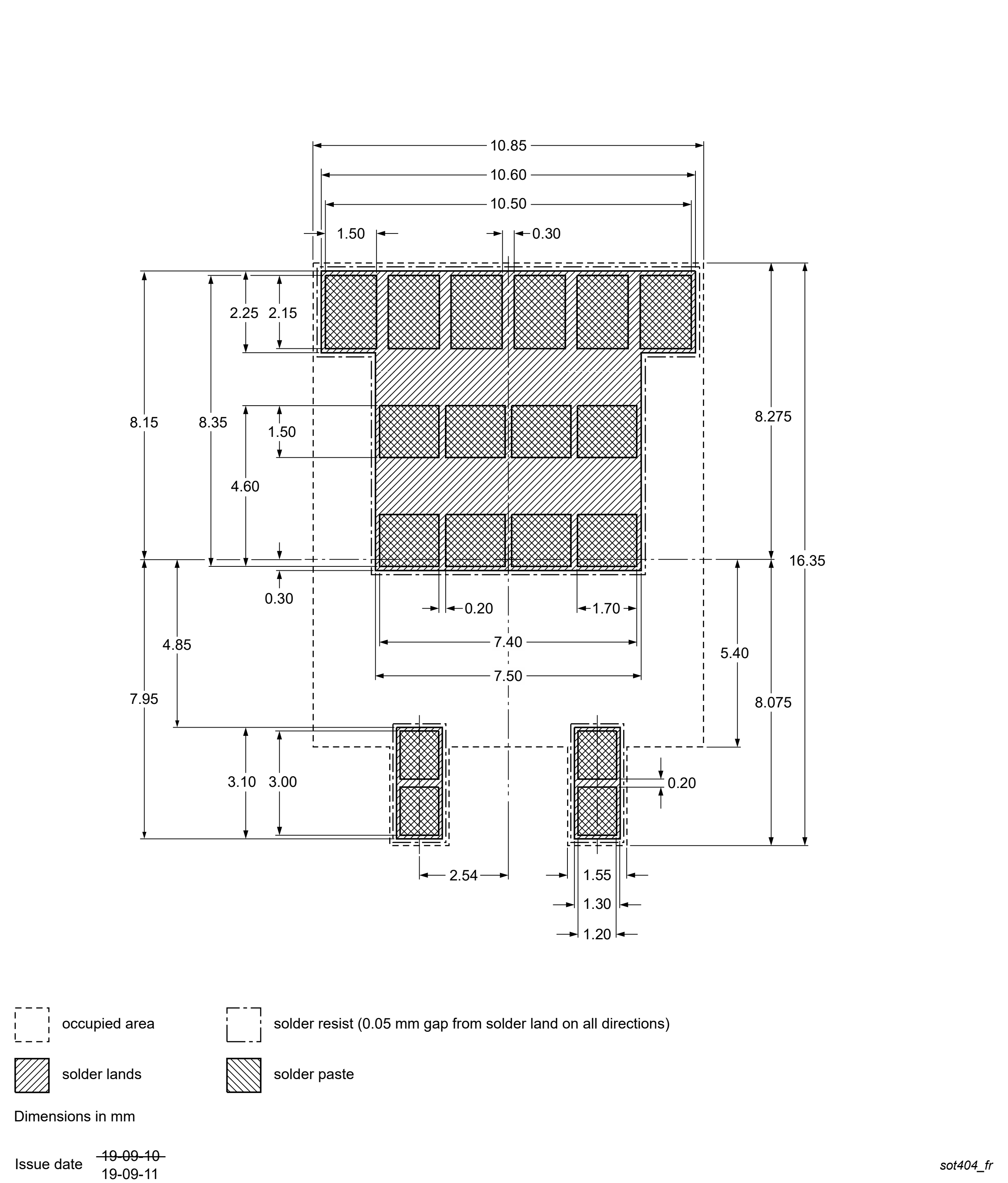


Fig. 19. Reflow soldering footprint for D2PAK (SOT404)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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