General Description

The PST731xxB family of low-dropout (LDO), low-power linear regulators offers high power supply rejection ratio (PSRR) while maintaining very low 35μA ground current. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response, and excellent PSRR performance. The PST731xxB is stable with a 1.0μF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 3% over all load, line, process, and temperature variations. It is fully specified from T_J = –40°C to +125°C and is offered in a small TSOT23-5 package, a tiny SC70-5 package, and a ultra-small 2mm × 2mm DFN package with a thermal pad, which are ideal for small form factor portable equipment such as wireless handsets and PDAs.

The PST731xxB is available in standard fixed output voltages of 1.2V (PST73112B), 1.5V (PST73115B), 1.8V (PST73118B), 2.5V (PST73125B), 2.8V (PST73128B), 3.0V (PST73130B), 3.3V (PST73133B), and custom voltage options (50mV step options between 0.8V and 5.0V are available upon request).

Features

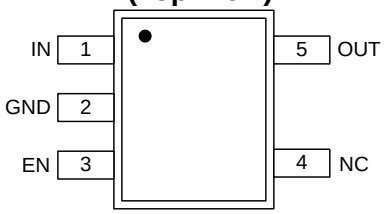
- Wide Input Voltage Range: 2.5V to 6.0V
- Up to 300mA Load Current
- Standard Fixed Output Voltage Options: 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, and 3.3V
- Other Output Voltage Options Available on Request
- Very Low I_Q: 35μA
- Ultra Low Dropout: 190mV at 300mA Load
- High PSRR: 65db at 100Hz
- Ultra-Fast Start-Up Time: 25μs
- Excellent Load/Line Transient Response
- Line Regulation: 0.03% typical
- Load Regulation: 0.1% typical
- Stable With 1μF Output Capacitor and Full Load Range (0 to 300mA)
- Short Circuit and Overcurrent Protection
- Thermal Shutdown Protection
- 5kV HBM ESD Protection
- Ambient Temperature Range: -40ºc To 85°C
- TSOT23-5, SOT23-5,SC70-5, and DFN package

Applications

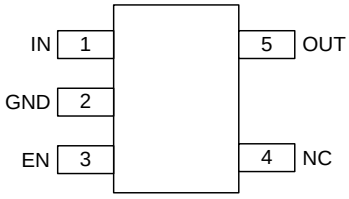
- Smart Phones and Cellular Phones
- PDAs
- MP3/MP4 Player
- Digital Still Cameras
- Portable instruments

Pin Configuration

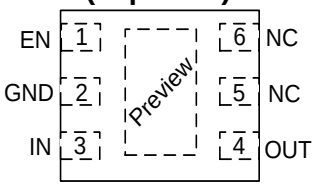
TSOT23-5
(Top View)



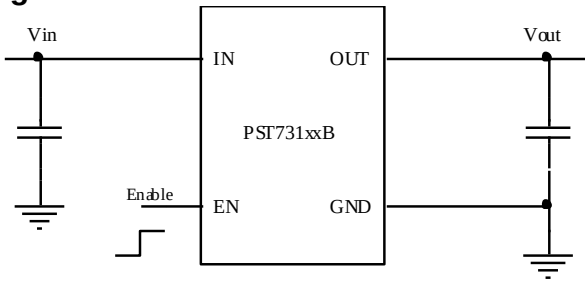
SC70-5
(Top View)



DFN2x2-6
(Top View)



Typical Application Diagram

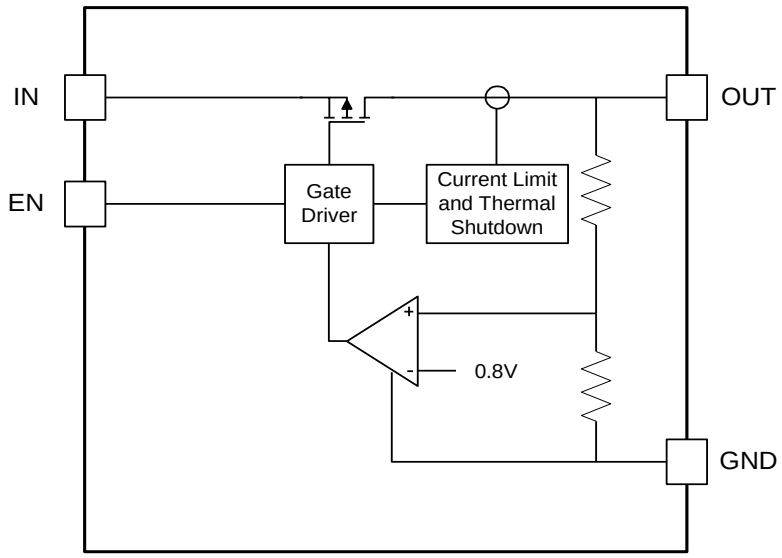


■ Ordering Information

PART NUMBER	TEMPERATURE RANGE	OUTPUT VOLTAGE	PACKAGE	TAPE&REEL
PST731xxBETV	-40°C to 85°C	xx/10 V *	TSOT23-5	-T
PST731xxBEJV	-40°C to 85°C	xx/10 V *	SOT23-5	-T
PST731xxBESL	-40°C to 85°C	xx/10 V *	SC70-5	-T
PST731xxBEFG	-40°C to 85°C	xx/10 V *	DFN2x2-6	-T

* **xx** is nominal output voltage (for example, 28 = 2.8V, 285 = 2.85V).

■ Block Diagram



■ Pin Description

Pin No.		Pin Name	Pin Function
TSOT23-5 SC70-5	DFN2x2-6		
1	3	IN	Supply input pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor.
2	2	GND	Ground
3	1	EN	Enable control input, active high. Do not leave EN floating.
4	5, 6	NC	No connection
5	4	OUT	Output pin. Bypass a 1μF ceramic capacitor from this pin to ground

■ Absolute Maximum Rating

Parameter		Rating	Unit
IN Voltage		-0.3 to 6.5	V
Other Pin Voltage		-0.3 to V_{IN}+0.3	V
Maximum Load Current		500	mA
Junction to Ambient Thermal Resistance (θ_{JA}), TSOT23-5		230	°C/W
Junction to Ambient Thermal Resistance (θ_{JA}), DFN2x2-6		130	°C/W
Operating Junction Temperature		-40 to 125	°C
Storage Temperature		-65 to 150	°C
Lead Temperature (Soldering, 10 sec)		300	°C
MSL Level (Note 2)		Level 2	
ESD Susceptibility	HBM (Human Body Model)	5	kV
	MM (Machine Model)	400	V

■ Electrical Characteristics

(V_{IN}= V_{EN} =3.6V, T_A = 25°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage Operation Range	V_{IN}		2.5		6.0	V
Dropout Voltage（Note 3）		I_{OUT} = 300mA		250	350	mV
DC Supply Quiescent Current	I_{Q_ON}	Active mode: V_{EN}=V_{IN}		35	70	μA
DC Supply Shutdown Current	I_{Q_OFF}	V_{EN}=0V		0.01	1	μA
Regulated Output Voltage	V_{OUT}	I_{OUT}=1mA, -40°C≤T_A≤85°C	-2		2	%
Line Regulation	$\Delta V_{OUT\_Line}/V_{OUT}$	V_{IN} = V_{OUT} +1V to 5.5V, I_{OUT} = 10mA			0.4	%
Load Regulation	$\Delta V_{OUT\_Load}/V_{OUT}$	I_{OUT} from 0mA to 300mA			0.6	%
Soft-start Time		From Enable to Power On		25		μs
Current Limit		R_{LOAD}=1Ω	450	600		mA
Power Supply Rejection Ratio	PSRR	f=100Hz, C_{OUT}=1μF, I_{OUT}=20mA		65		dB
EN Low Threshold	VIL				0.4	V
EN High Threshold	VIH		1.4			V
EN Pin Input Current	I_{EN}			0	0.1	μA
Over-temperature Shutdown Threshold				155		°C
Over-temperature Shutdown Hysteresis				20		°C

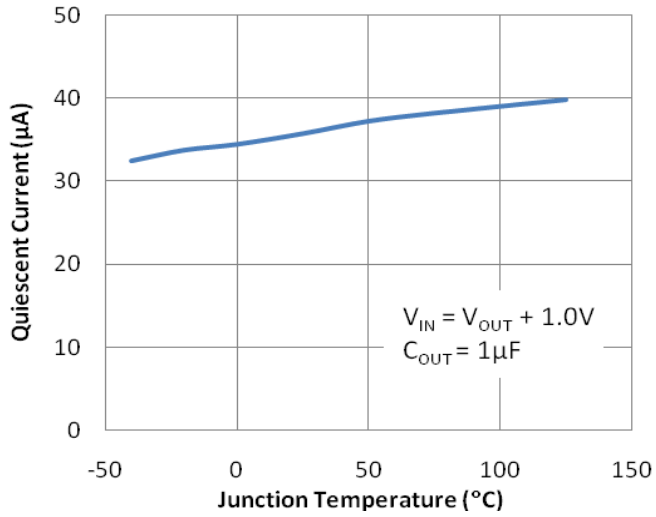
Note: Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 2: Level and body temperature defined by IPC/JEDEC J-STD-020

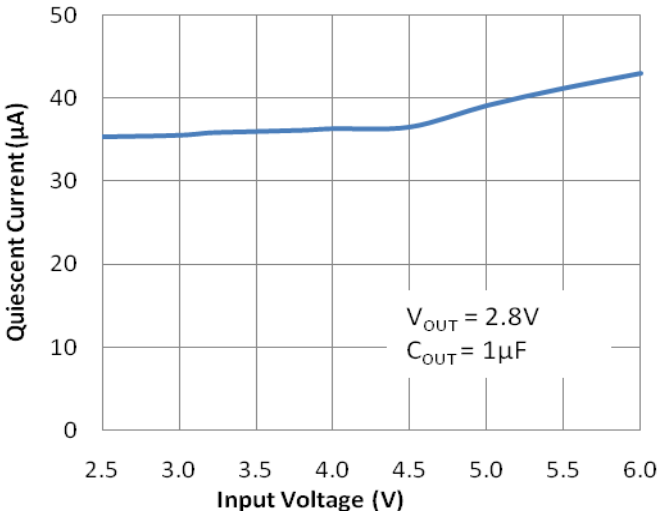
Note 3: Dropout Voltage is defined as Vin-Vout when Vout is 98% of nominal.

Typical Performance Characteristics

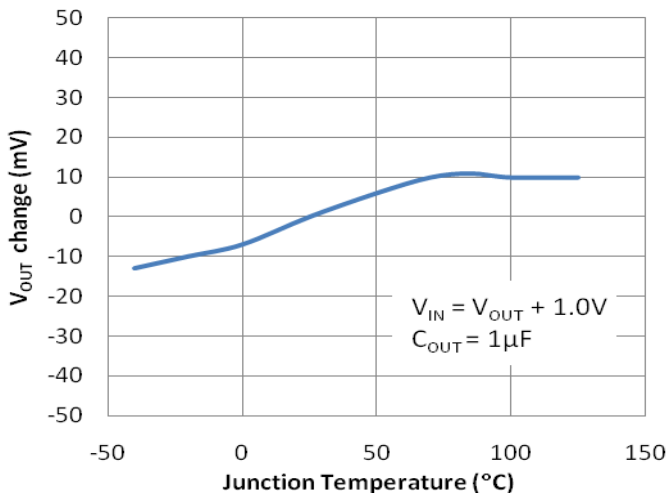
Quiescent Current vs. Temperature



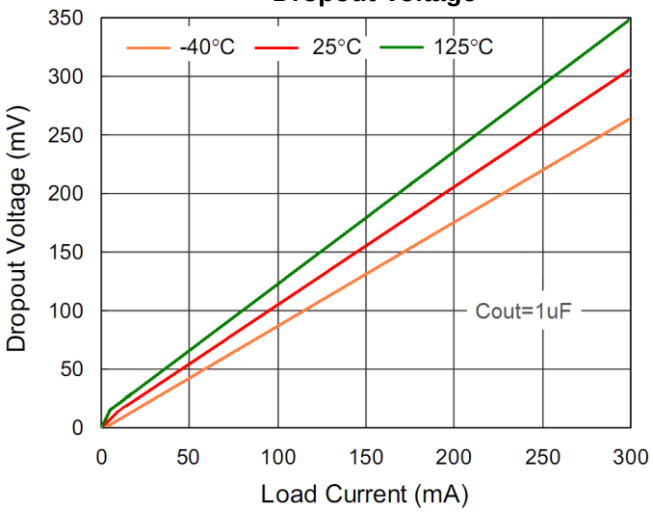
Quiescent Current vs. Input Voltage



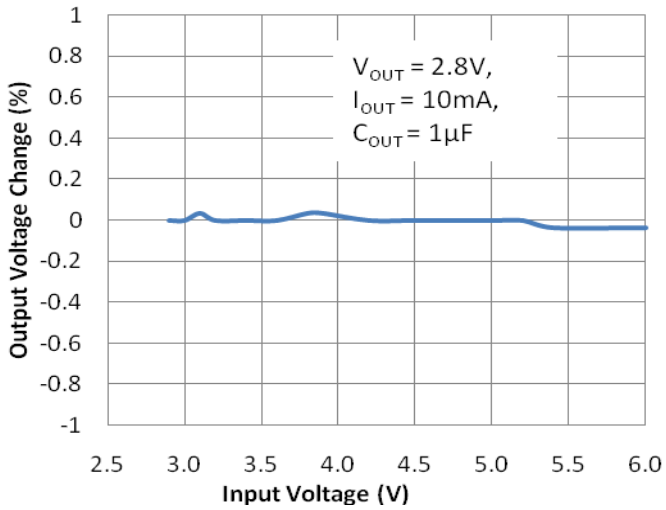
Output Voltage Change vs. Temperature



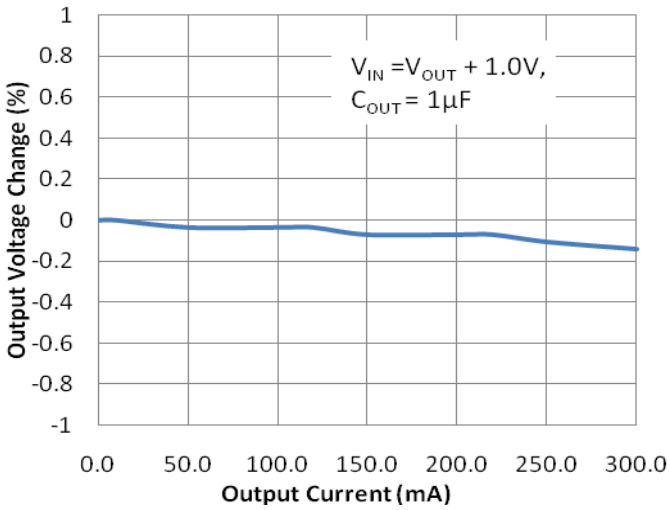
Dropout Voltage



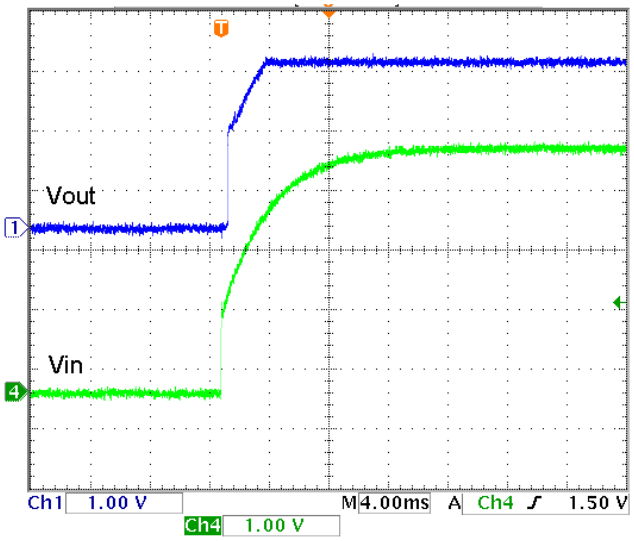
Line Regulation



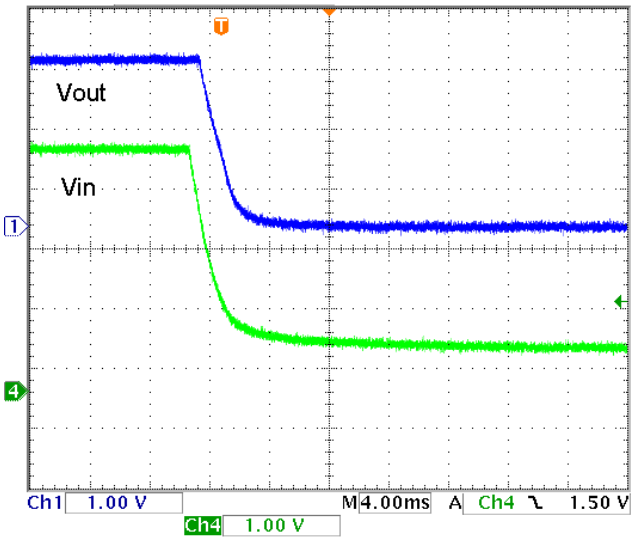
Load Regulation



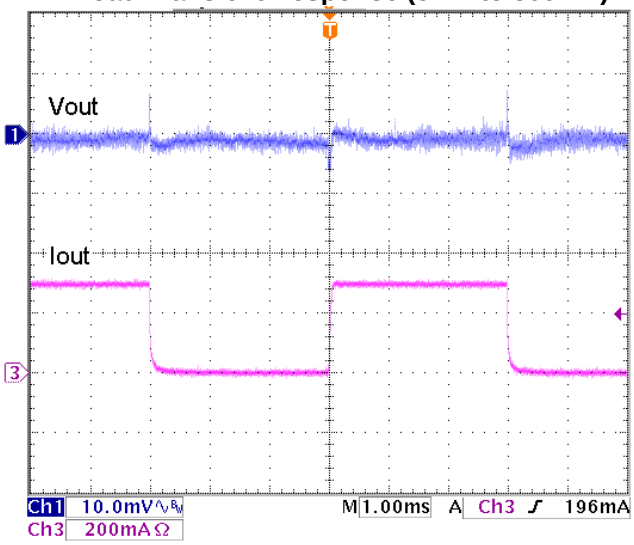
Power On



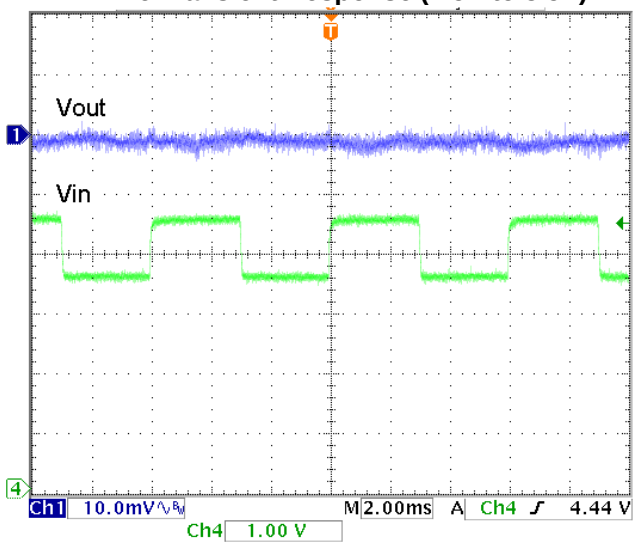
Power Down



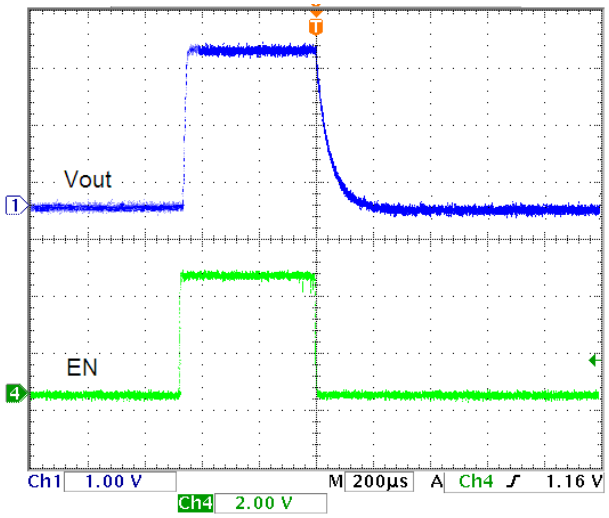
Load Transient Response (5mA to 300mA)



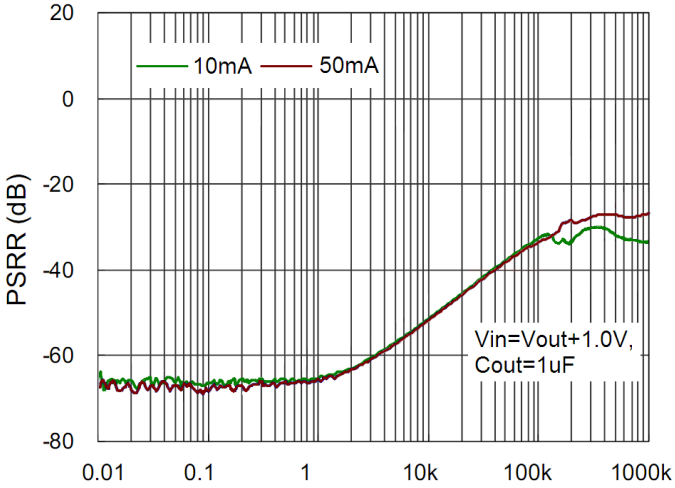
Line Transient Response (4.5V to 3.5V)



LDO Enable/Disable



Power Supply Ripple Rejection vs. Frequency



Input Capacitor

A 1μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 2.2μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics is X7R or X5R. Higher capacitance values help to improve load/line transient response. Place output capacitor as close as possible to OUT and GND pins.

ON/OFF Input Operation

The PST731XXB is turned on by pulling up the EN pin to logic high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

Ultra Fast Start-up

After enabled, the PST731XXB is able to provide full power in as little as tens of microseconds, typically 25μs. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

Fast Transient Response

Fast transient response LDOs can also extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100μA to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDOs.

The PST731XXB's fast transient response from 0 to 300mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Low Quiescent Current

Cellular phone baseband internal digital circuits typically operate all the time. That requires LDO stays on at all times. However, in the standby mode, the microprocessor consumes only around 100~300μA. Since the phone stays in standby for the longest percentage of time, using a 40μA quiescent current LDO, instead of 100μA, saves 60μA and can substantially extends the battery standby time.

The PST731XXB, consuming only around 35μA for all input range and output loading, provides great power saving in portable and low power applications.

Current Limit Protection

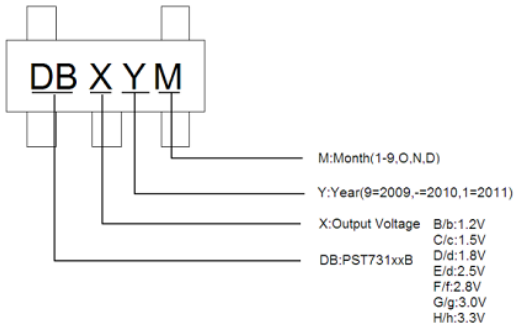
When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuit to GND, the current limit protection will be triggered and clamp the output current to approximately 500mA to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

Thermal protection disables the output when the junction temperature rises to approximately +155°C, allowing the

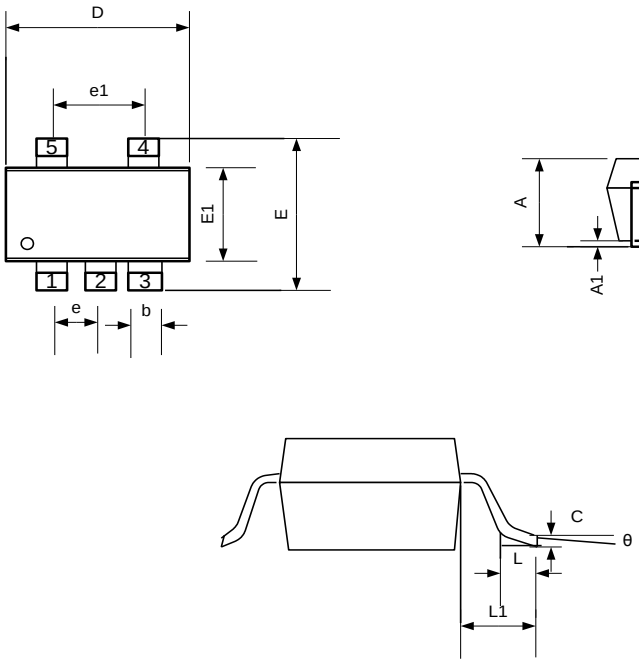
device to cool down. When the junction temperature reduces to approximately +135°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

■ Marking Information



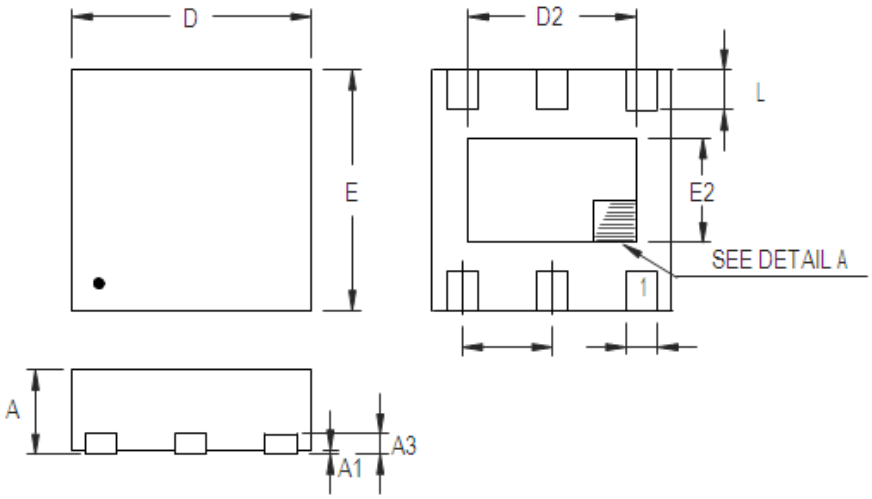
■ Package Information

TSOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.9	1.1	0.036	0.044
A1	0.01	0.13	0.0004	0.0052
b	0.3	0.5	0.012	0.02
C	0.09	0.2	0.0036	0.008
D	2.8	3	0.112	0.12
E	2.5	3.1	0.1	0.124
E1	1.5	1.7	0.06	0.068
L	0.2	0.55	0.008	0.022
L1	0.35	0.8	0.014	0.032
e	0.95 Bsc.		0.038 Bsc.	
e1	1.90 Bsc.		0.076 Bsc.	
θ	0^o	10^o	0^o	10^o

DFN2X2-6



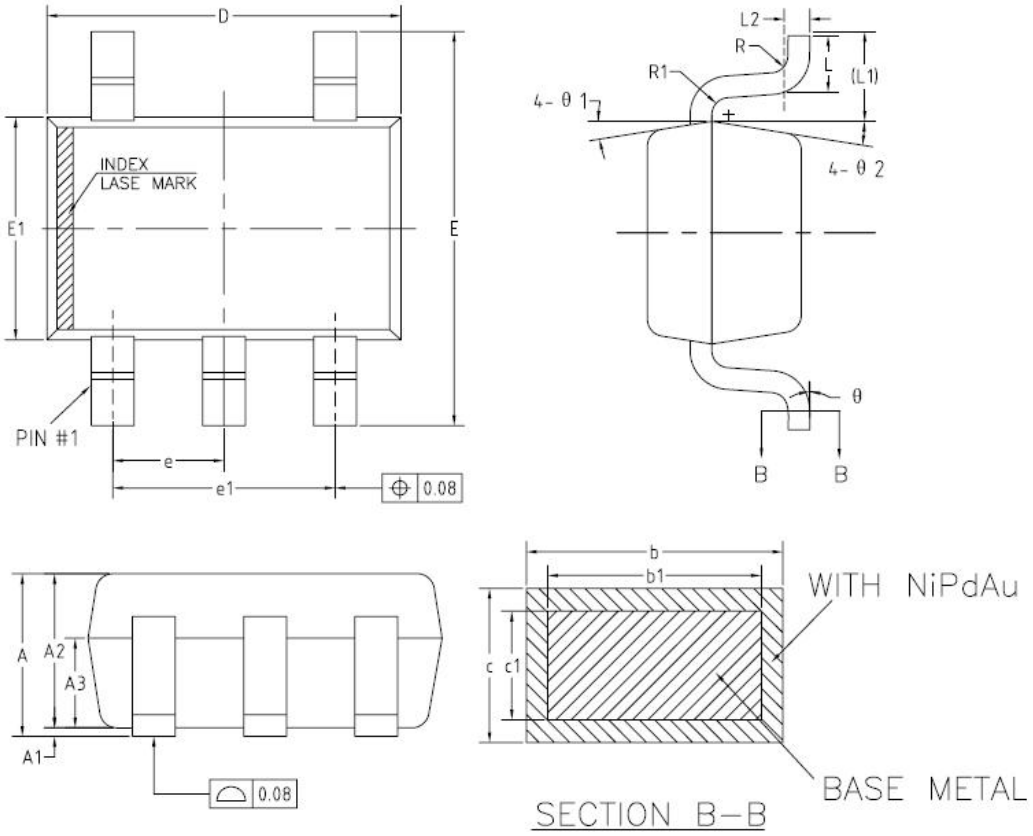
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note: The configuration of the Pin#1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.7	0.8	0.028	0.031
A1	0	0.05	0	0.002
A3	0.175	0.25	0.007	0.01
b	0.2	0.35	0.008	0.014
D	1.95	2.05	0.077	0.081
D2	1	1.45	0.039	0.057
E	1.95	2.05	0.077	0.081
E2	0.5	0.85	0.02	0.033
e	0.65		0.026	
L	0.3	0.4	0.012	0.016

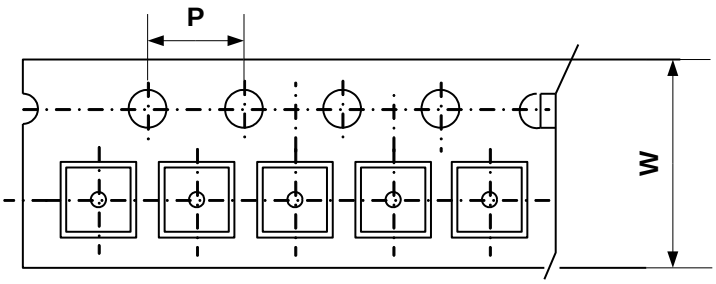
SC70-5

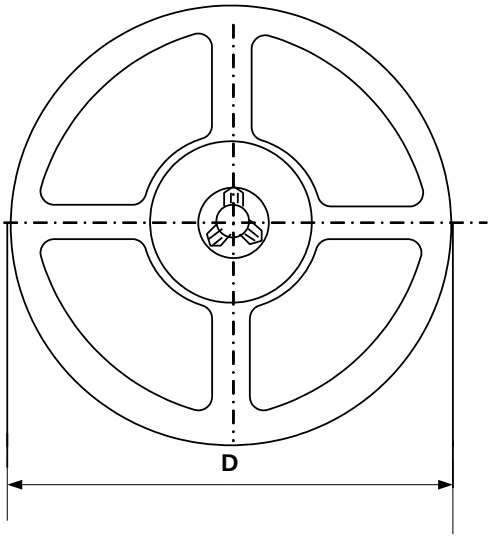


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYBOL	MIN	NOM	MAX
A	0.85	-	1.05
A1	0.00	-	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
b	0.22	-	0.29
b1	0.22	0.25	0.28
c	0.115	-	0.15
c1	0.115	0.13	0.14
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.25	1.30	1.35
e	0.65BSC		
e1	1.30BSC		
L	0.28	0.33	0.38
L1	0.50REF		
L2	1.30BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	-	8°
θ1	6°	9°	12°
θ2	6°	9°	12°

■ Packing Information





Package Type	Carrier Width (W)	Pitch (P)	Reel Size(D)	Packing Minimum
TSOT23-5L	8.0±0.1 mm	4.0±0.1 mm	180±1 mm	3000pcs

Note: Carrier Tape Dimension, Reel Size and Packing Minimum

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