3.3V 8Gb SLC
NAND Flash Memory
Specification and Technical Notes

PSU8GA30AT

Part Number	Cell	Density	Organization	Vcc	PKG Type
PSU8GA30AT	SLC	8G	X8	2.7V~3.6V	TSOP I

Revision 1.0
June 30, 2011

Document Title

PSU8GA30AT (1G x 8 bit NAND Flash Memory, SLC)

Revision History

Rev.	Description	Date	Remark
0.1	Initial draft	February 22, 2011	Preliminary
1.0	Revise Copy-Back Program Operation with Random Data Input diagram	June 30, 2011	Preliminary

PSU8GA30AT (1G x 8 bit NAND Flash Memory, SLC)

Product List

Part Number	Vcc Range	Organization	Package Type
PSU8GA30AT	2.7V~3.6V	X8	TSOP I

Features

- Voltage Supply: 2.7 V ~ 3.6V
- Organization
  - Memory Cell Array: (4K + 218) x 256K x 8bit
  - Data Register: (4K + 218) x 8bit
- Automatic Program and Erase
  - Page Program: (4K + 218) Bytes
  - Block Erase: (256K + 13.6K) Bytes
- Page Read Operation
  - Page Size: (4K + 218) Byte
  - Random Read: 30us (Max.)
  - Serial Access: 30ns (Min.)
- Memory Cell: 1bit/Memory Cell
- Fast Write Cycle Time
  - Program time: 300us (Typ.)
  - Block Erase time: 2.5ms (Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
  - Endurance: please refer to qualification report
  - Data Retention: please refer to qualification report
- Operating temperature：
  - Commercial: 0 to 70 ℃
  - Industrial: -40 to 85 ℃
- Command Register Operation
- Unique ID for Copyright Protection

  Package: Pb-FREE 48-Pin TSOP I

Summary Description

The Duetron PSU8GA30AT is an 8G bit Single-Level-Cell (SLC) product with 8 I/O and spare 218 x 256K x 8bit capacity. The device is offered in 3.3V Vcc Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 4096 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the (4K + 218) Byte page in typical 300us and an erase operation can be performed in typical 2.5ms on a (256K + 13.6K) Bytes.

Data in the page mode can be read out at 30ns cycle time per Byte. The I/O pins serve as the ports for address and command inputs as well as data input/output. The copy back function allows the optimization of defective blocks management: when a page program operation fails, the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out.

Pin Assignment (TSOP I)

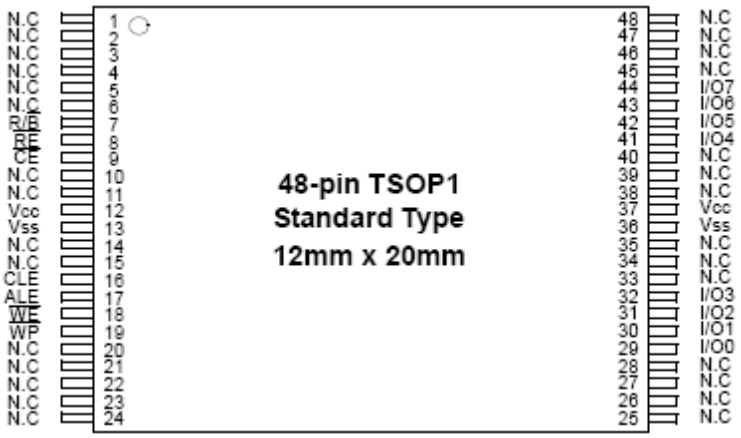
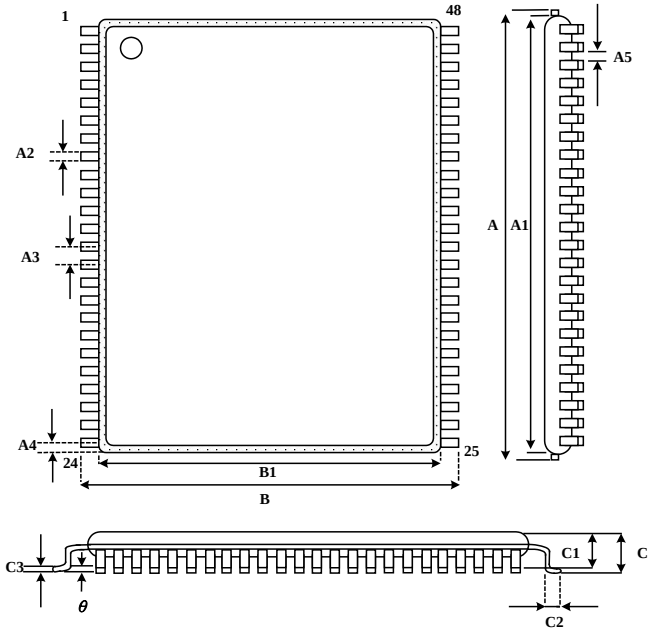


Diagram of 48-TSOP1



Unit:Millimeter (mm) ; θ : (˚)

ITEM	MIN	TYP	MAX
A	–	–	12.4
A1	11.9	–	12.1
A2	0.14	–	0.3
A3	–	0.5	–
A4	–	0.25	–
A5	–	0.1	–
B	19.8	–	20.2
B1	18.3	–	18.5
C	–	–	1.2
C1	0.9	–	1.1
C2	0.4	–	0.6
C3	0.09	–	0.2
θ (°)	0 (°)	–	10 (°)

Pin Description

Pin Name	Pin Function
I/O_0 ~ I/O_7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE# with ALE high.
CE#	**CHIP ENABLE** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**WRITE ENABLE** The WE# input controls writes to the I/O port. Commands, address and data are latched on the

	rising edge of the WE# pulse.
WP#	**WRITE PROTECT** The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**READY/BUSY OUTPUT** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V_{CC}	**POWER** V_{CC} is the power supply for device.
V_{SS}	**GROUND**
N.C.	**NO CONNECTION** Lead is not internally connected.

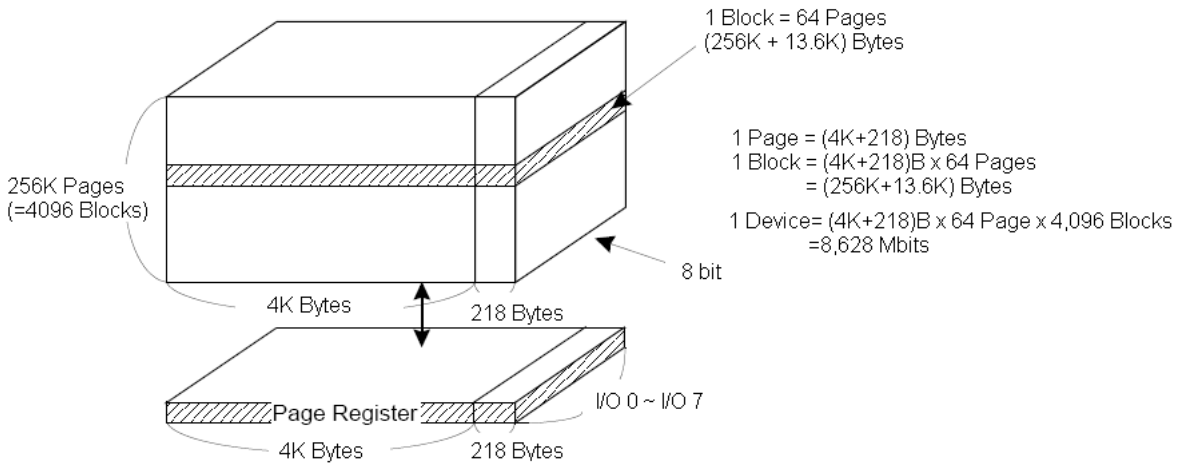
NOTE : Connect all VCC and VSS pins of each device to common power supply outputs. Do not leave VCC or VSS disconnected.

Array Organization

1 Page = (4K+218) Bytes

1 Block = (4K+218) B x 64 Pages = (256K+13.6K) Bytes

1 Device = (4K+218) B x 64 Pages x 4096 Blocks

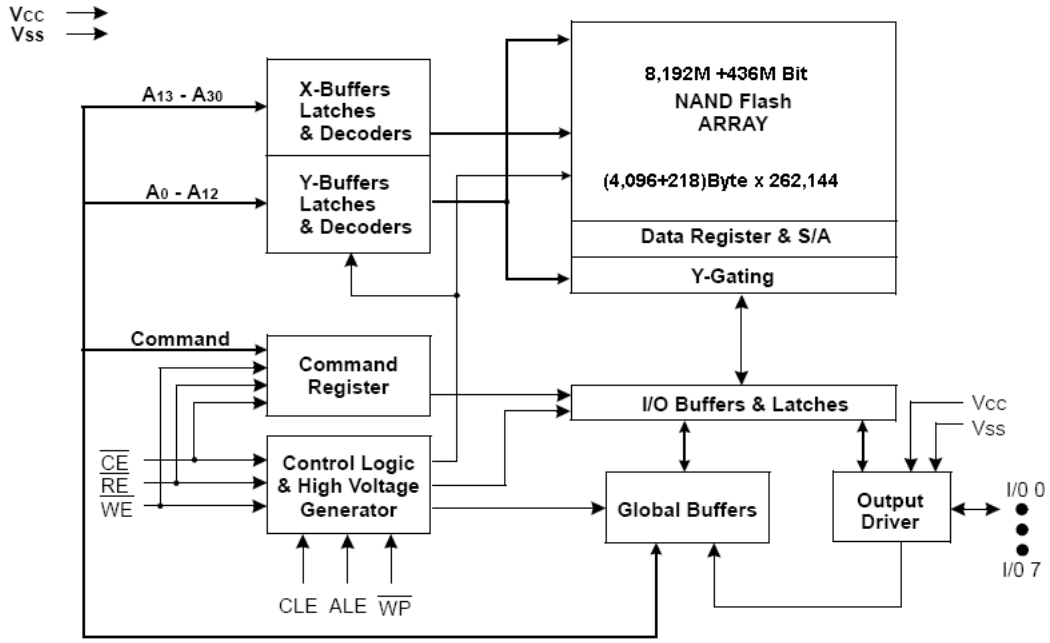


Address Cycle Map

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd cycle	A8	A9	A10	A11	A12	*L	*L	*L	Column Address
3rd cycle	A13	A14	A15	A16	A17	A18	A19	A20	Row Address
4th cycle	A21	A22	A23	A24	A25	A26	A27	A28	Row Address
5th cycle	A29	A30	**A31	*L	*L	*L	*L	*L	Row Address

NOTE : Column Address : Starting Address of the Register.
*** L must be set to "Low".**
*** The device ignores any additional input of address cycles than required.**
**** A31 is reserved for stack option**

Block Diagram



Command Sets

Function	1st Set	2nd Set	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input (1)	85h	-	
Random Data Output (1)	05h	E0h	
Read Status	70h	-	O
Read Status 2	F1h		O
Two-Plane Read (3)	60h---60h	30h	
Two-Plane Read for Copy-Back	60h---60h	35h	
Two-Plane Random Data Output (1) (3)	00h---05h	E0h	
Two-Plane Page Program (2)	80h---11h	81h---10h	
Two-Plane Copy-Back Program (2)	85h---11h	81h---10h	
Two-Plane Block Erase	60h---60h	D0h	
Cache Program	80h	15h	
Cache Read	31h		
Read Start for Last Page Cache Read	3Fh		

Two-Plane Cache Read [3]	60h---60h	33h	
Two-Plane Cache Program [2]	80h---11h	81h---15h	

NOTE :
1. Random Data Input/Output can be executed in a page.
2. Any command between 11h and 80h/81h/85h is prohibited except 70h/F1h and FFh.
3. Two-Plane Random Data must be used after Two-Plane Read operation or Two-Plane Cache Read Operation

Absolute Maximum Ratings

Parameter		Symbol	Rating	Unit
Voltage on any pin relative to VSS		Vcc	-0.6 to +4.6	V
		VIN	-0.6 to +4.6	
		VI/O	-0.6 to Vcc+0.3(<4.6V)	
Temperature Under Bias	Commercial	TBIAS	-10 to +125	℃
	Industrial		-40 to +125	
Storage Temperature	Commercial	TSTG	-65 to +150	℃
	Industrial			
Short Circuit Current		IOS	5	mA

NOTE :

1. Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
   Maximum DC voltage on input/output pins is Vcc+0.3V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

(Voltage reference to GND, Commercial :TA=0 to 70℃, Industrial : TA=-40 to 85℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	2.7	3.3	3.6	V
Supply Voltage	Vss	0	0	0	V

DC and Operation Characteristics

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	tRC=30ns, CE#=VIL, IOUT=0mA	-	15	30	mA
	Program	ICC2	-	-	15	30	
	Erase	ICC3	-	-	15	30	
Stand-by Current (TTL)		ISB1	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)		ISB2	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc (max)		-	+/-10	
Output Leakage Current		ILO	VOUT=0 to Vcc (max)		-	+/-10	
Input High Voltage		VIH (1)		0.8 x Vcc	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL (1)		-0.3	-	0.2 x Vcc	
Output High Voltage Level		VOH	IOH=-400 uA	2.4	-	-	
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.4V	8	10	-	mA

NOTE :

1. VIL can undershoot to -0.4V and VIH can overshoot to VCC + 0.4V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25℃. Not 100% tested.

Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
PSU8GA30AT	NVB	4,016	-	4,096	Blocks

NOTE :

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented **as first shipped**. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment.
3. The number of valid block is on the basis of single plane operations, and this may be decreased with two plane operations.

AC Test Condition (Commercial: T_A=0 to 70℃, Industrial: T_A=-40 to 85℃ ,Vcc=2.7V~3.6V, unless otherwise noted)

Parameter	PSU8GA30AT
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load	1 TTL GATE and C_L=50pF

Capacitance (T_A=25℃, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	8	pF
	$C_{I/O(w)}$			5	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	8	pF
	$C_{IN(w)}$		-	5	pF

NOTE : 1. Capacitance is periodically sampled and not 100% tested.

2. $C_{I/O(w)}$ and $C_{IN(w)}$ are tested at wafer level

Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input (5 clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input (5 clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE :

1. X can be VIL or VIH.
2. WP# should be biased to CMOS high or CMOS low for standby.

Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	300	700	us
Dummy Busy Time for Multi Plane Program	t_{DBSY}	-	0.5	1	us
Dummy Busy Time for Cache Program (Last page)	tCBSY	-		1	ms
Number of Partial Program Cycles in the Same Page	NOP	-	-	4	cycle
Block Erase Time	t_{BERS}	-	2.5	10	ms

NOTE :

1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25℃ temperature.
2. **tPROG is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.**

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	$t_{CLS}^{(1)}$	15	-	ns
CLE Hold Time	t_{CLH}	5	-	ns
CE# Setup Time	$t_{CS}^{(1)}$	20	-	ns
CE# Hold Time	t_{CH}	5	-	ns
WE# Pulse Width	t_{WP}	15	-	ns
ALE Setup Time	$t_{ALS}^{(1)}$	15	-	ns
ALE Hold Time	t_{ALH}	5	-	ns
Data Setup Time	$t_{DS}^{(1)}$	15	-	ns
Data Hold Time	t_{DH}	5	-	ns
Write Cycle Time	t_{WC}	30	-	ns
WE# High Hold Time	t_{WH}	10	-	ns

Address to Data Loading Time	t_{ADL}(2)	100(2)	-	ns

NOTE :
1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. t_{ADL} is the time from the WE rising edge of final address cycle to the WE# rising edge of first data cycle.

AC Characteristics for Operation

Parameter		Symbol	Min	Max	Unit
Data Transfer from Cell to Register		tR	-	30	us
ALE to RE# Delay		tAR	10	-	ns
CLE to RE# Delay		tCLR	10	-	ns
Ready to RE# Low		tRR	20	-	ns
RE# Pulse Width		tRP	15	-	ns
WE# High to Busy		tWB	-	100	ns
Read Cycle Time		tRC	30	-	ns
RE# Access Time		tREA	-	20	ns
CE# Access Time		tCEA	-	25	ns
RE# High to Output Hi-Z		tRHZ	-	100	ns
CE# High to Output Hi-Z		tCHZ	-	30	ns
RE# High to Output Hold		tRHOH	15	-	ns
RE# Low to Output Hold		tRLOH	5	-	ns
CE# High to Output Hold		tCOH	15	-	ns
RE# High Hold Time		tREH	10	-	ns
Output Hi-Z to RE# Low		tIR	0	-	ns
RE# High to WE# Low		tRHW	100	-	ns
WE# High to RE# Low		tWHR	60	-	ns
Cache Busy in Read Cache (following 31h and 3Fh)		tDCBSYR		35	us
Device Resetting Time during…	Read	tRST	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5 (1)	us

NOTE: 1. If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

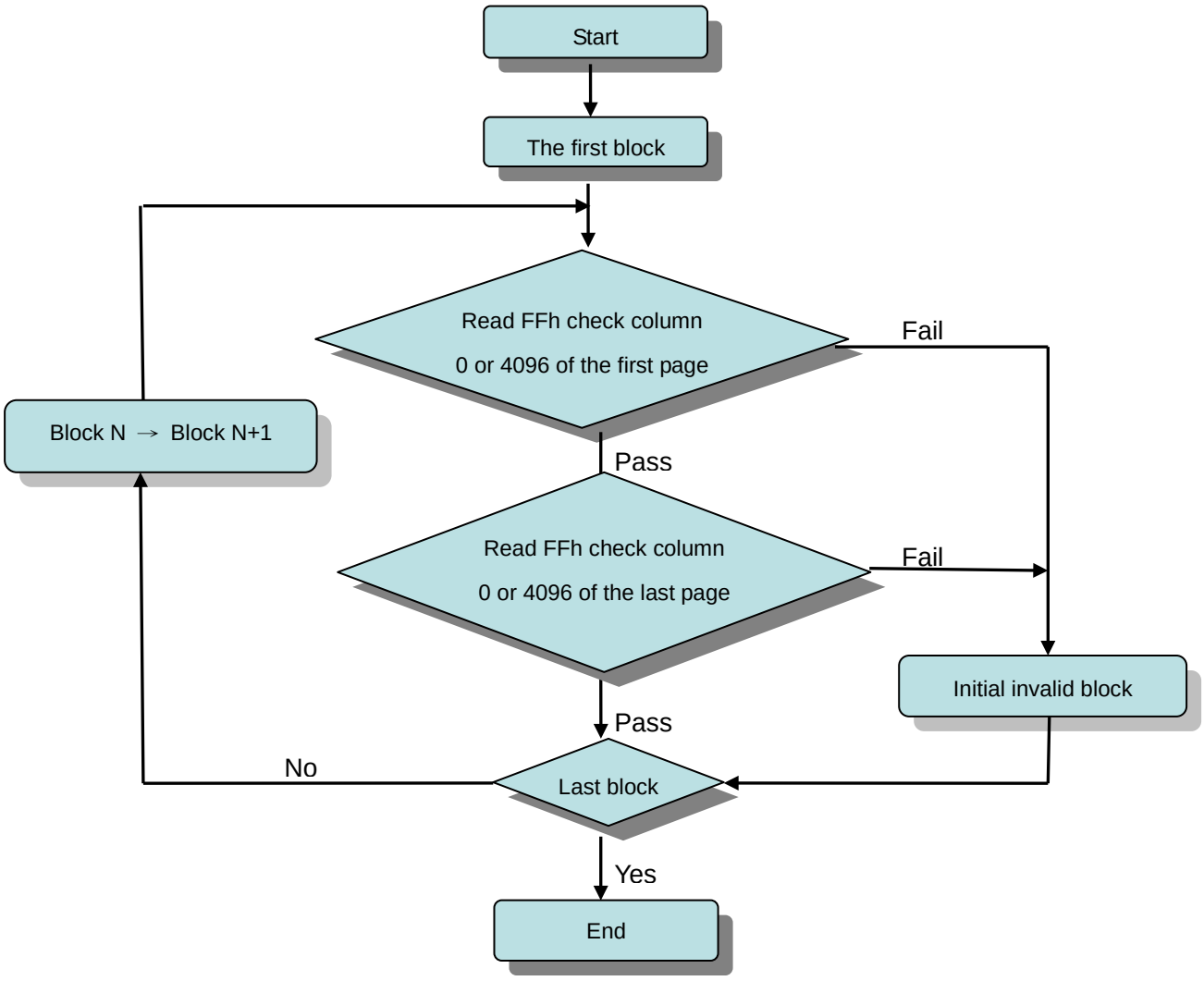
Mask Out Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Duetron. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

Identifying Initial Invalid Block(s) and Block Replacement Management

Unpredictable behavior may result from programming or erasing the defective blocks. Figure 7 illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.

A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address of 0 or 4,096. If the read data is not FFh, the block is interpreted as an invalid block. The initial invalid block information is erasable, and which is impossible to be recovered once it has been erased. Therefore, the host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.




```
For (i=0; i<Num_of_LUs; i++)
{
      For (j=0; j<Blocks_Per_LU; j++)
      {
            Defect_Block_Found=False;

            Read_Page(lu=i, block=j, page=0);
            If (Data[coloumn=0]!=FFh)    Defect_Block_Found=True;
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)    Defect_Block_Found=True;

            Read_Page(lu=i, block=j, page=Page_Per_Block-1);
            If (Data[coloumn=0]!=FFh)    Defect_Block_Found=True;
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)    Defect_Block_Found=True;

            If (Defect_Block_Found)    Mark_Block_as_Defective(lu=i, block=j);
```

```
        }
    }
```

Algorithm for Bad Block Scanning

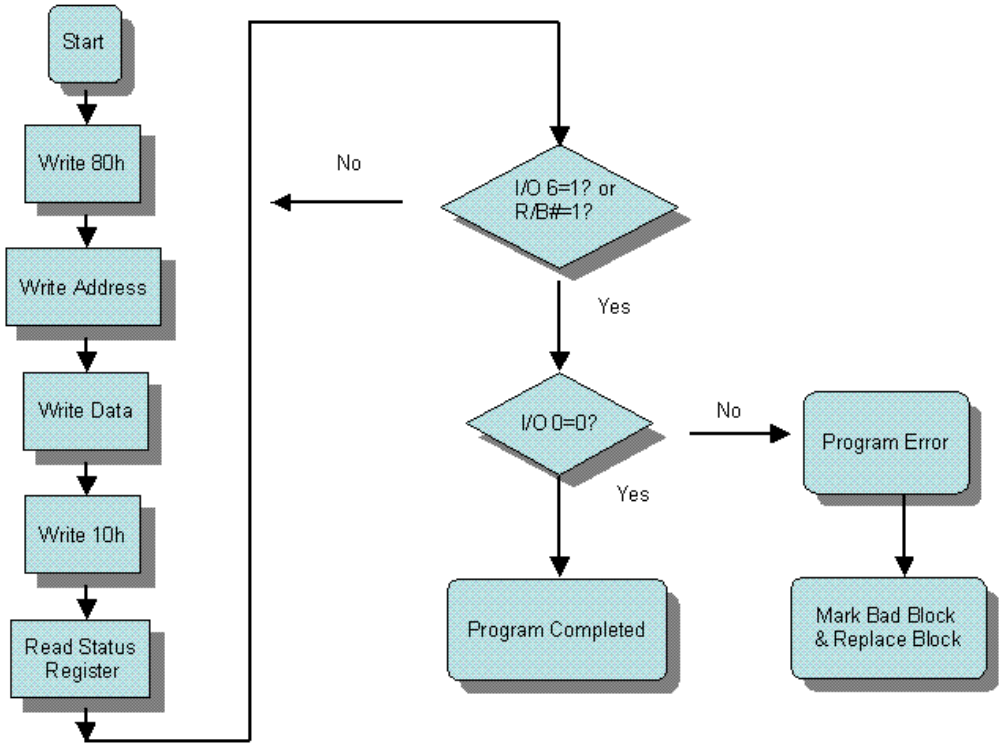
Error in Write or Read Operation

Within its lifetime, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

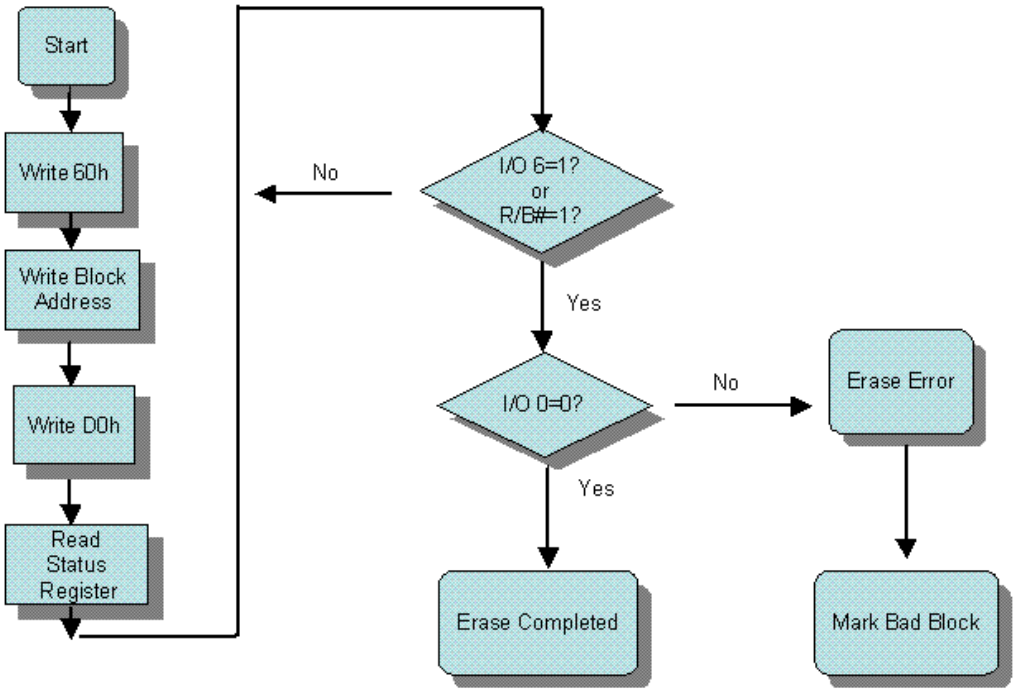
Failure Mode		Detection and Countermeasure Sequence
Write	Erase failure	Read Status after Erase → Block Replacement
	Program failure	Read Status after Program → Block Replacement
Read	Up to four bits failure	Verify ECC → ECC Correction

NOTE: Error Correcting Code → RS Code or BCH Code etc.
Example: 4bits correction / 528 Byte

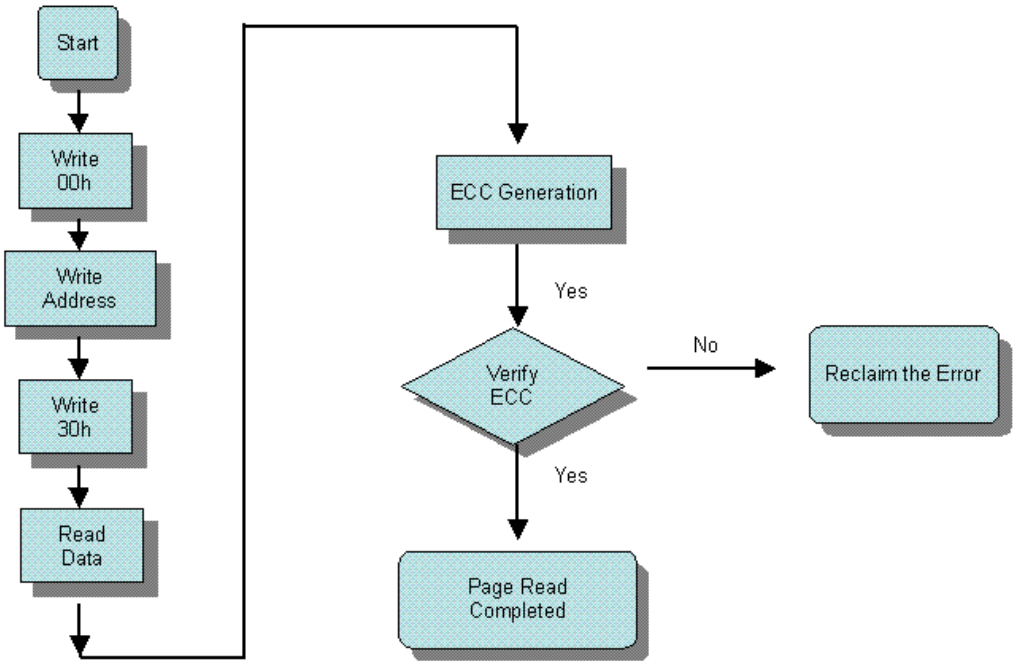
Program Flow Chart



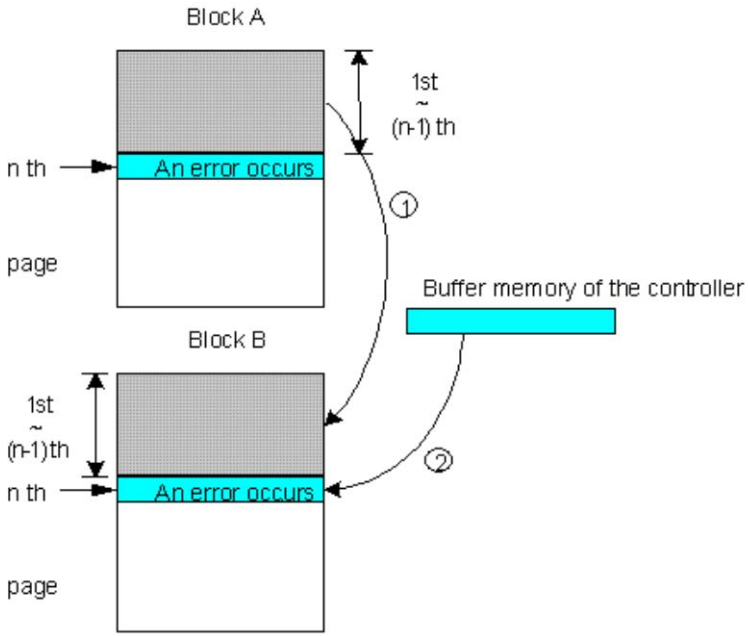
Erase Flow Chart



Read Flow Chart



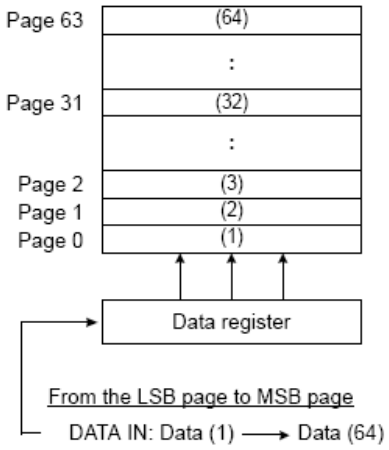
Block Replacement

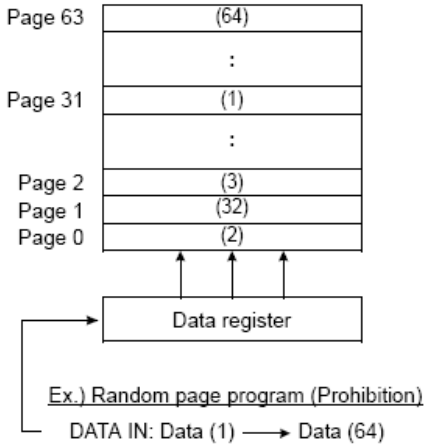


NOTE:
Step 1 - When an error happens in the n^{th} page of the Block “A” during erase or program operation.
Step 2 - Copy the data in the 1^{st} ~$(n-1)^{th}$ page to the same location of another free block. (Block “B”)
Step 3 - Then, copy the nth page data of the Block “A” in the buffer memory of the controller to the nth page of the block “B”.
Step 4 – Prevent further access to bad block “A”. It needs to identify Block “A” as bad Block..

Addressing for Program Operation

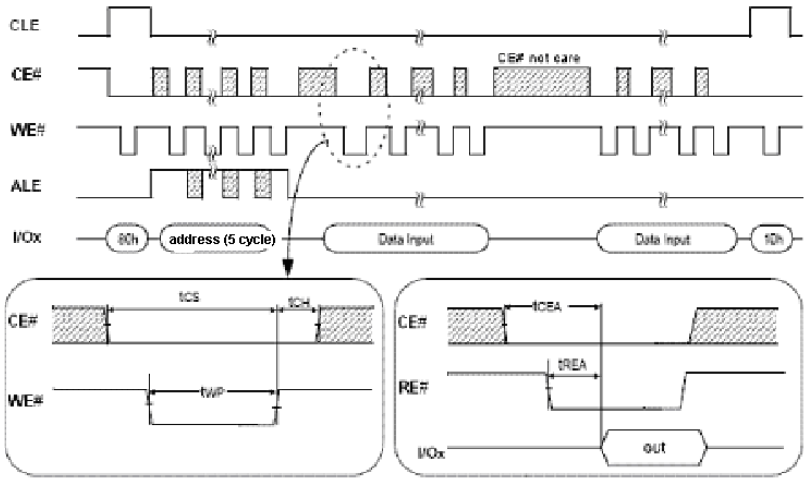
Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.



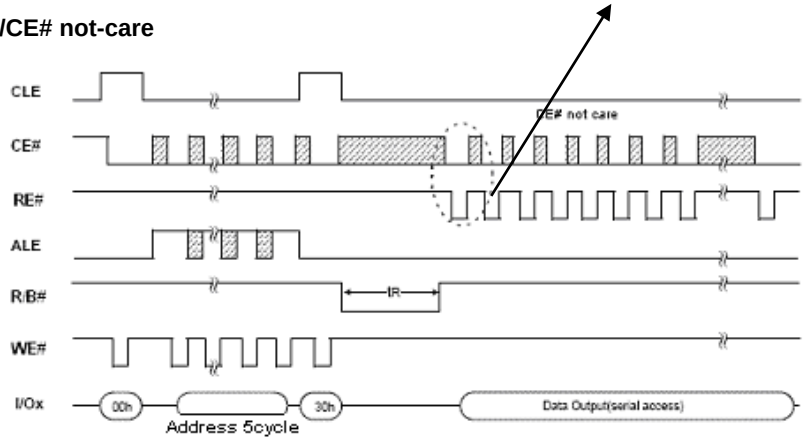


System Interface Using CE# Don't Care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 4,314byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications that use slow cycle time on the order of μ-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.



Read Operation w/CE# not-care



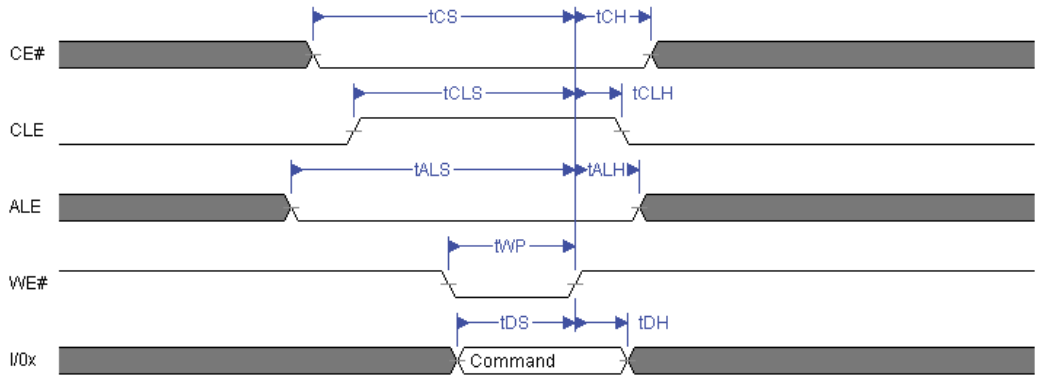
Program/Read Operation with "CE# not-care"

NOTE:

Device	Data	I/O	Address				
	Data In/Out	I/Ox	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
PSU8GA30AT	4,314Byte	I/O 0~I/O 7	A0 ~ A7	A8 ~ A12	A13 ~ A20	A21 ~ A28	A29~A30

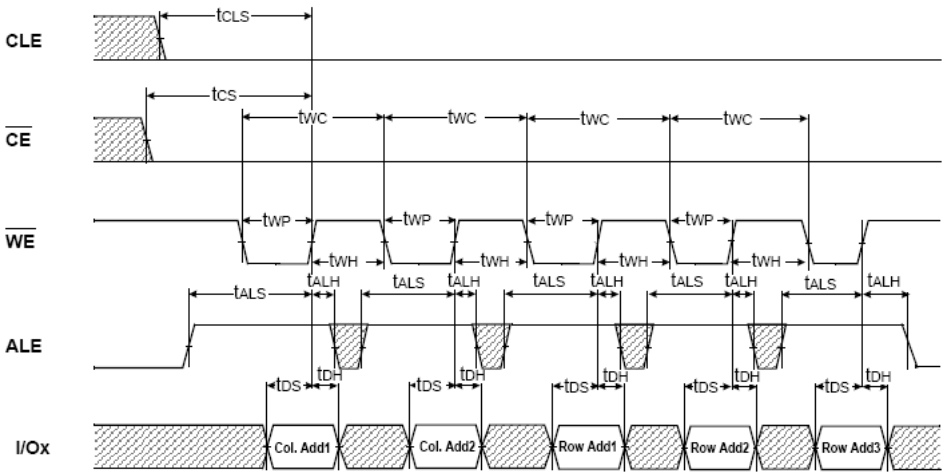
Timing Diagrams

Command Latch Cycle



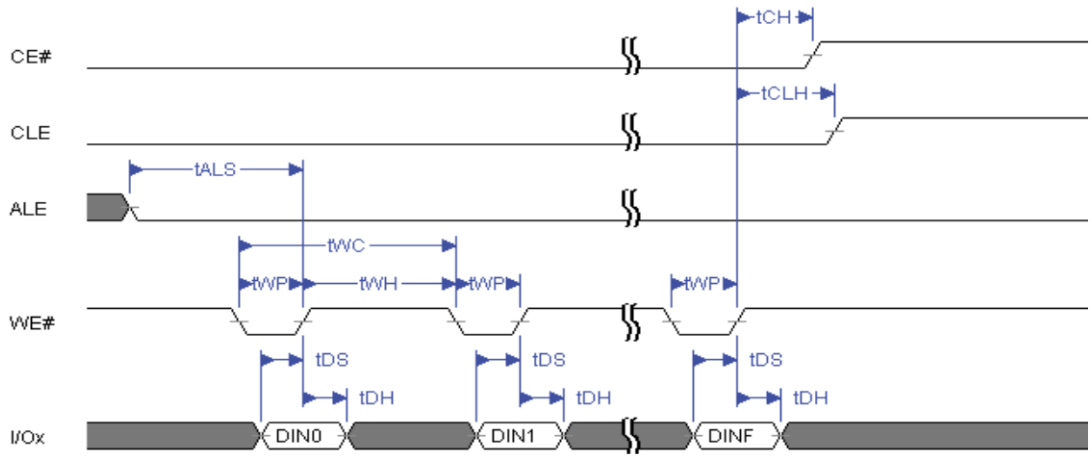
Command Latch Cycle

Address Latch Cycle



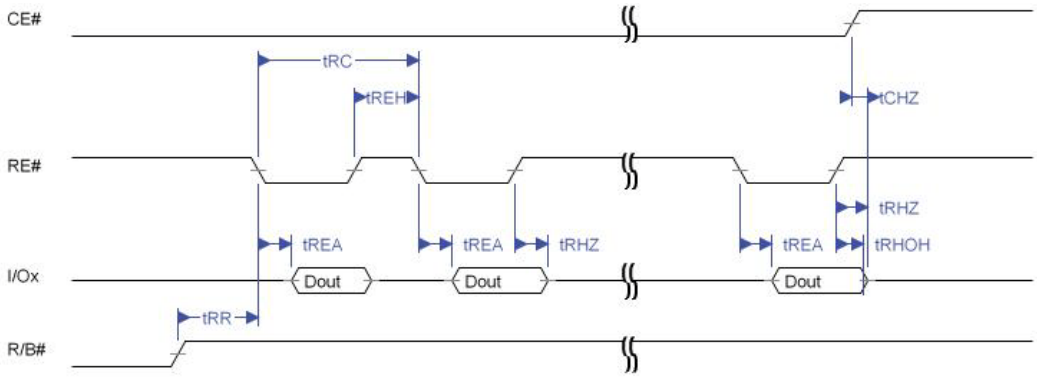
Address Latch Cycle

Input Data Latch Cycle



Input Data Latch Cycle

Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

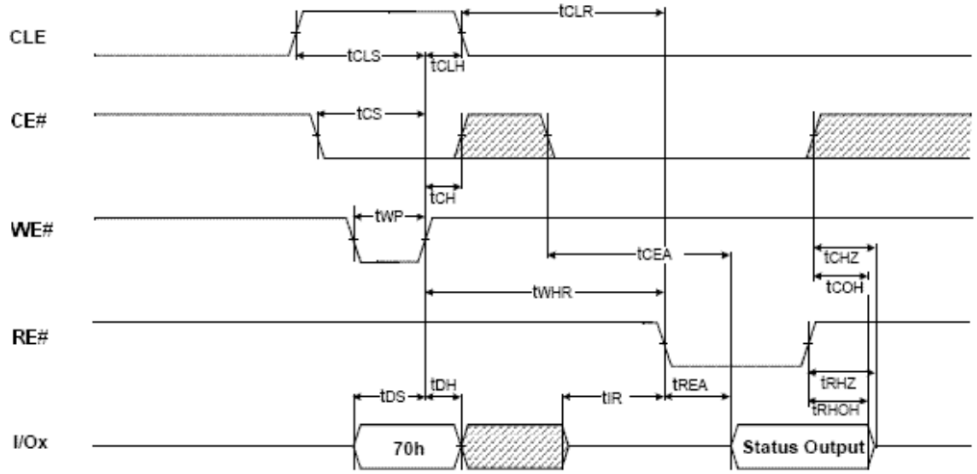


NOTE:

1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 20MHz.
3. tCHZ and tRHZ are sampling tested and not 100% tested.

Sequential Out Cycle after Read

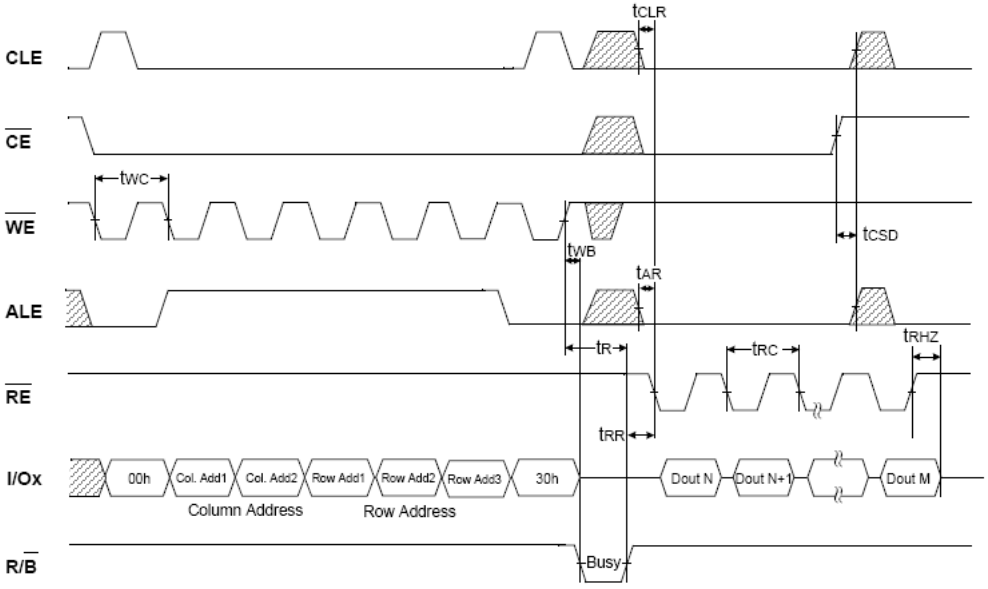
Status Read Cycle



Note: 70h represents the hexadecimal number

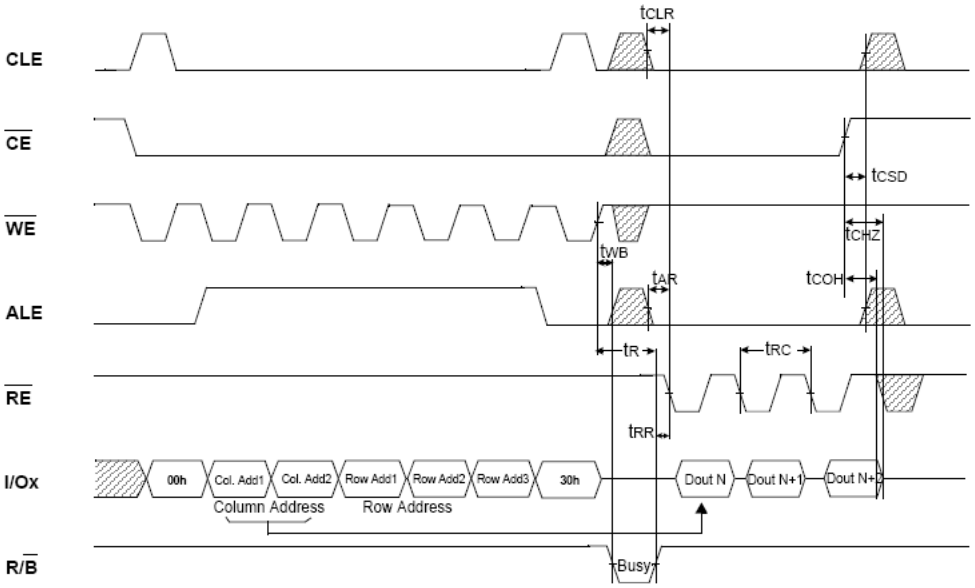
Status Read Cycle

Read Operation



Read Operation (Read One Page)

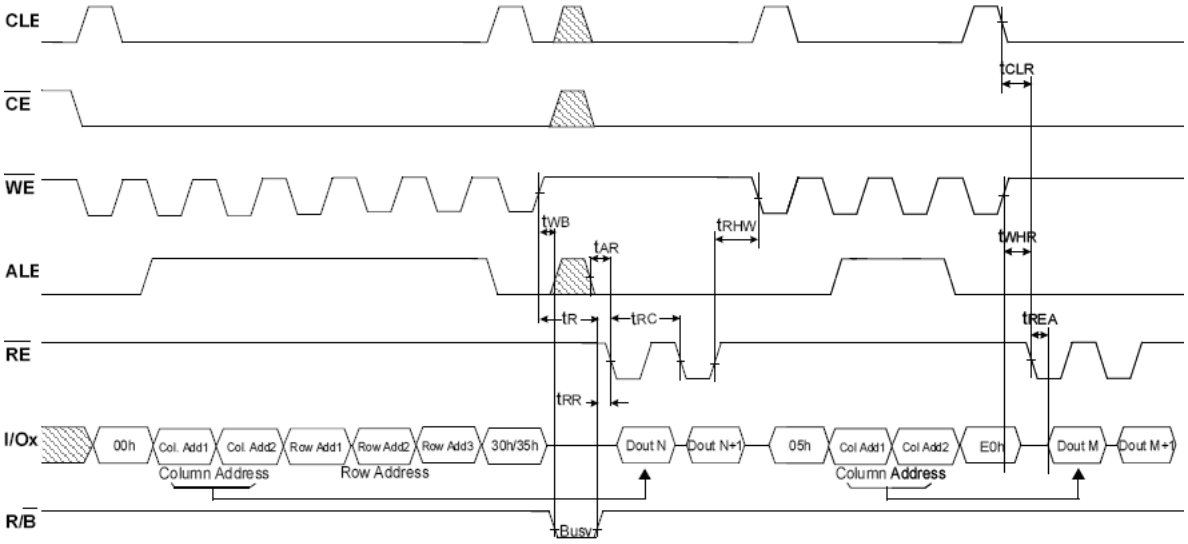
Read Operation (Intercepted by CE#)



Read Operation Intercepted by CE#

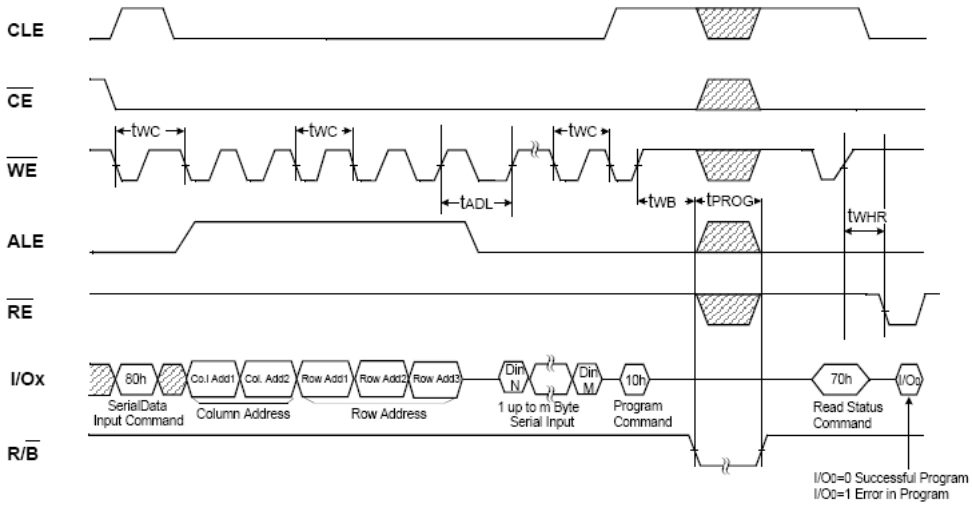
Two-plane read

Random Data Output In a Page



Random Data Output

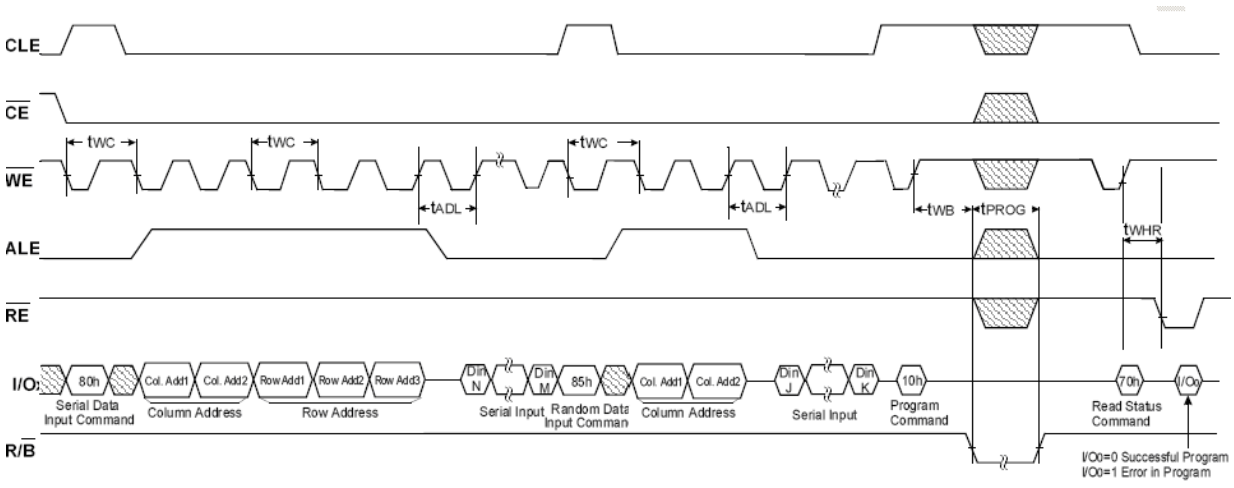
Page Program Operation



NOTE: t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of the first data cycle.

Random Data Output

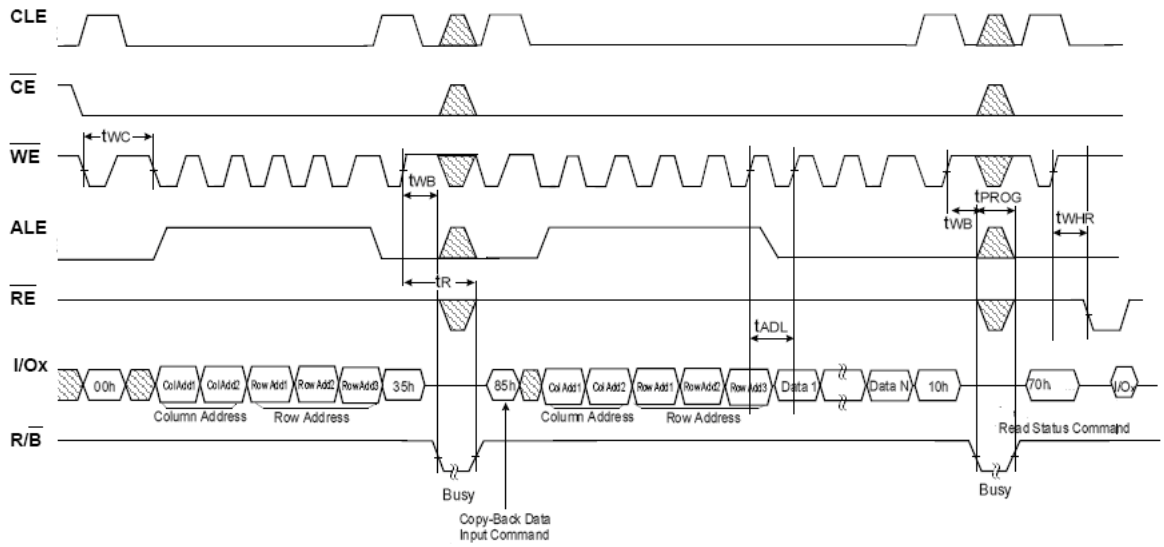
Page Program Operation with Random Data Input



NOTE: t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of the first data cycle.

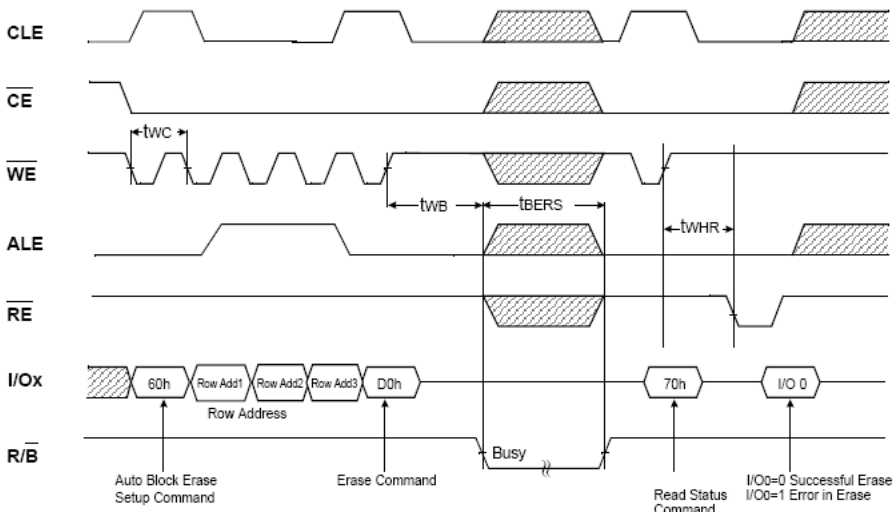
Random Data In

Copy-Back Program Operation with Random Data Input



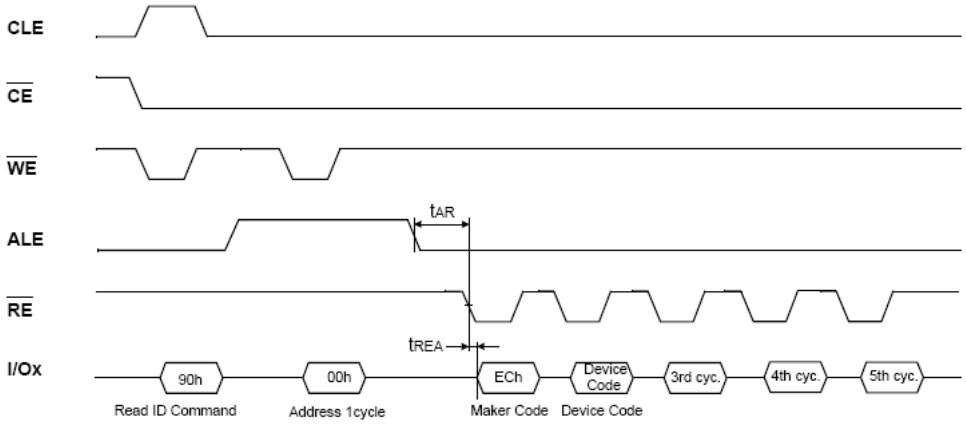
Copy-Back Program Operation with Random Data Input

Block Erase Operation



Block Erase Operation

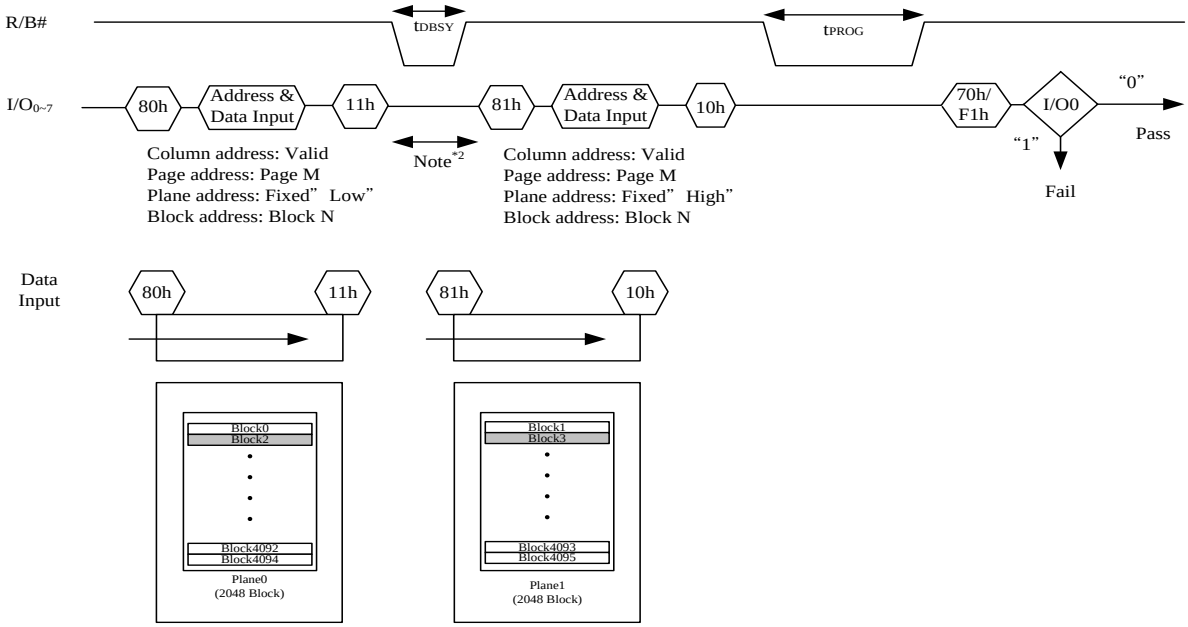
Read ID Operation



Read ID Operation

Two-plane operation

The device is equipped with two memory planes, and the two sets of 4,314-byte data registers enable simultaneous read/program/erase operations in two planes to enhance system performance. Since the two memory planes share the same page decoding circuit, two-plane operations need to be executed on symmetric pages. For instance, if page 31 of block 0 (plane 0) is selected for some two-plane operation, the page 31 of block 1 (plane 1) is its mirrored page and needs to perform the same operation at the same time.



Command Sequence of Two-plane Page Program

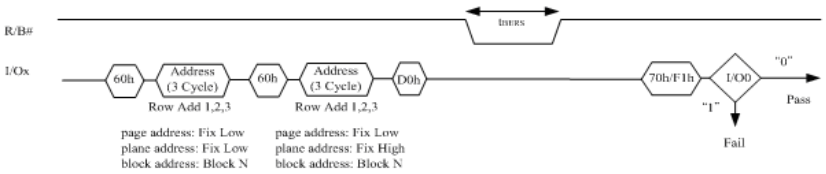
Note: 1. It is noticeable that same row address except for A_{20} is applied to the two blocks

2. Any command between 11h and 81h is prohibited except 70h/F1h and FFh.

Two-plane Block Erase

Similar to Two-plane Page Program, two symmetric blocks from each plane can be simultaneously erased by using Two-plane Block Erase command. Following figure illustrates the Two-plane Block

Erase sequence. The completion can be detected by monitoring R/B# pin or the Status bit I/O6.



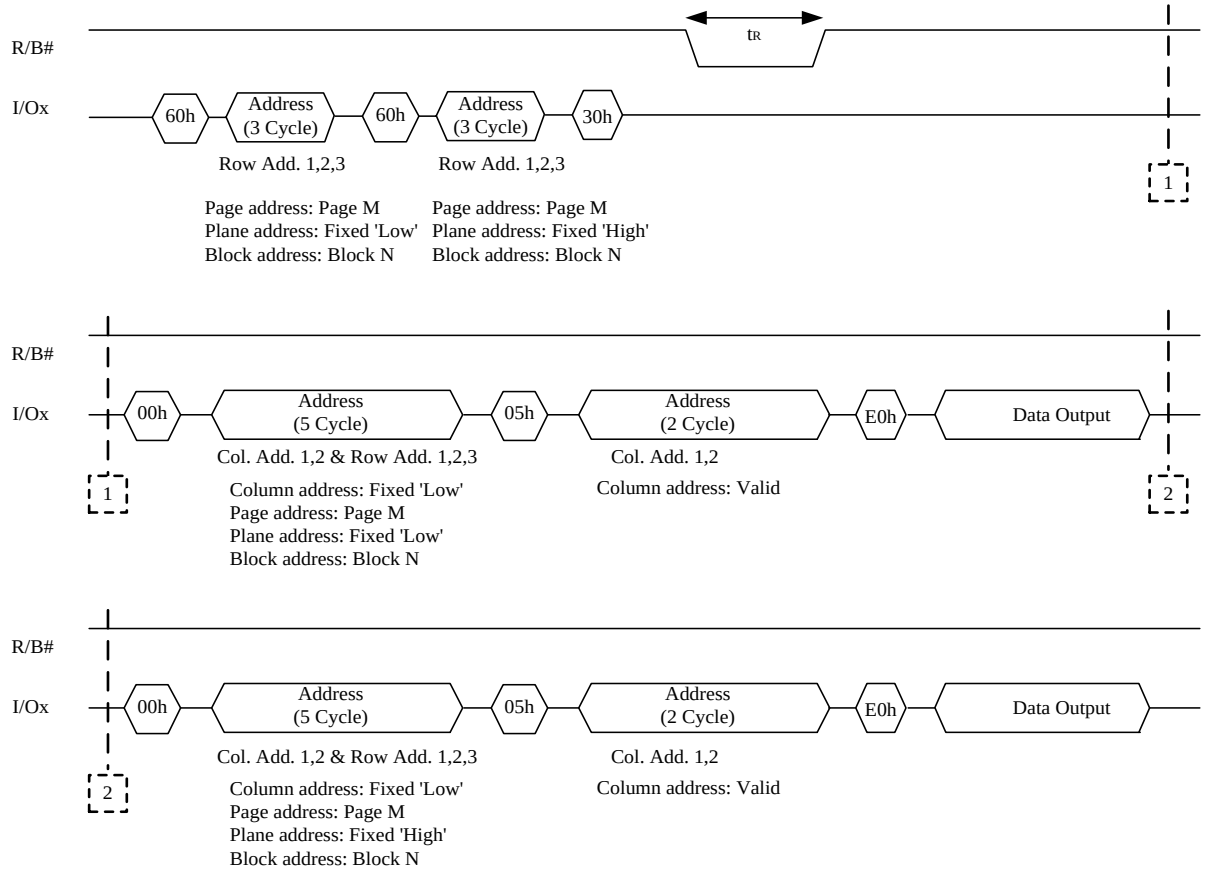
Command Sequence of Two-plane Block Erase

.

Two-plane Page Read

The Two-plane Page Read sequence and its restrictions are shown in Fig below. Two-plane Page Read is initiated by repeating command 60h followed the three address cycles twice, and only same page of same block can be selected from each plane.

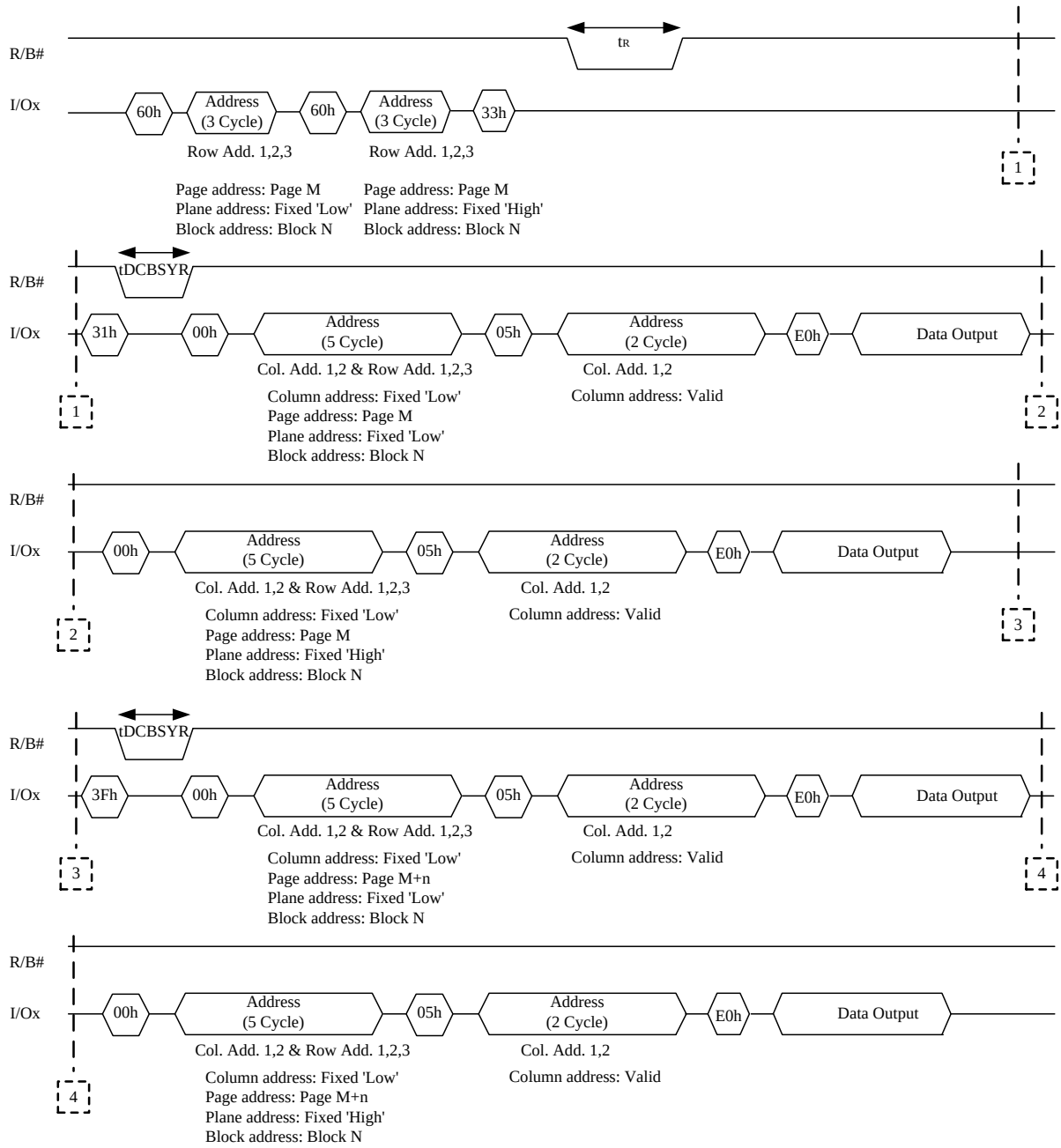
After Read Confirm command (30h) the 8,628 bytes of data within the selected two pages are transferred to the cache registers via data registers within t_R. The host controller can detect the completion of data transfer (t_R) by monitoring the R/B# output. Once the data is loaded into the cache registers, the data output of the first plane can be read out by issuing command 00h with five address cycles, command 05h with two-cycle column address and finally E0h. The data output of the second plane can be read out using the identical command sequence. Two-plane Read command can only must be used in a block which has been programmed with Two-plane Page Program operation



Command Sequence of Two-plane Page Read

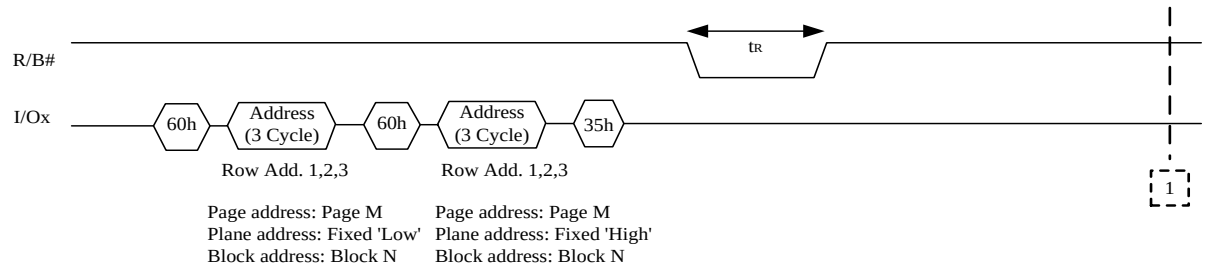
Two-plane Cache Read

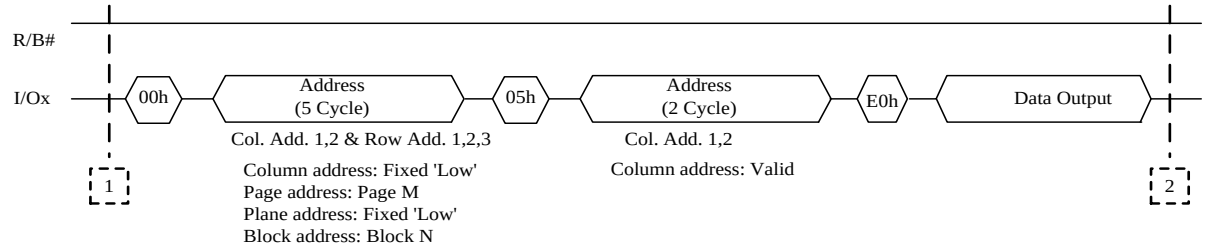
The Two-plane Cache Read sequence is shown in below, only same page of same block can be selected from each plane. After Read Confirm command (33h), the 8,628 bytes of data are transferred to data registers within t_R. After issuing Cache Read command (31h), read data in the data registers are transferred to cache registers within a short period of time (t_{DCBSYR}). Once the data are loaded into the cache registers, the data of both planes can be read out in the same way as the Two-Plane Page Read operation. The host controller shall use 3Fh instead of 31h to indicate the Two-plane Cache Read operation for the last target pages.

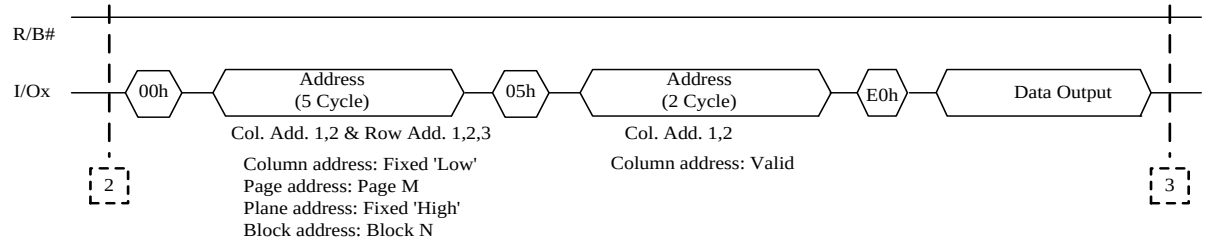


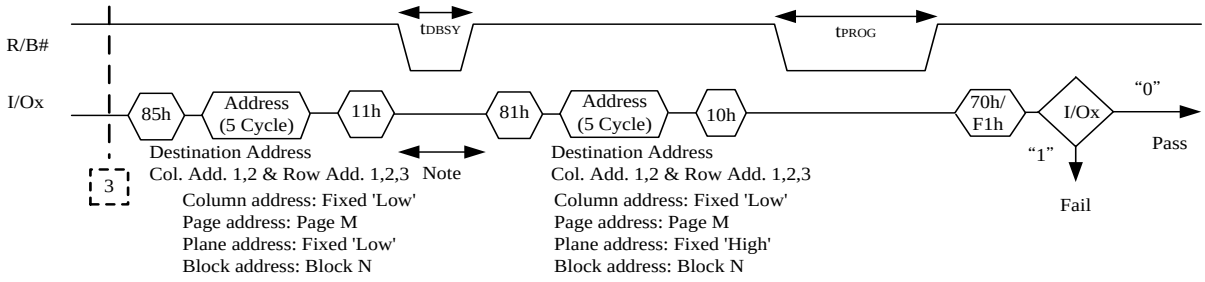
Command sequence of Two-plane Cache Read

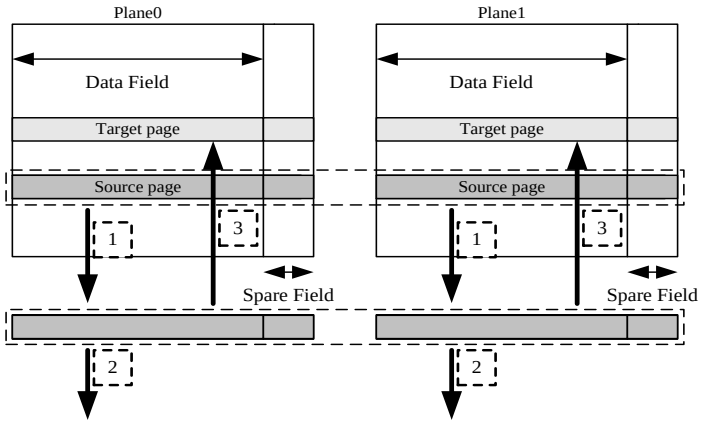
Two-plane Copy-Back program











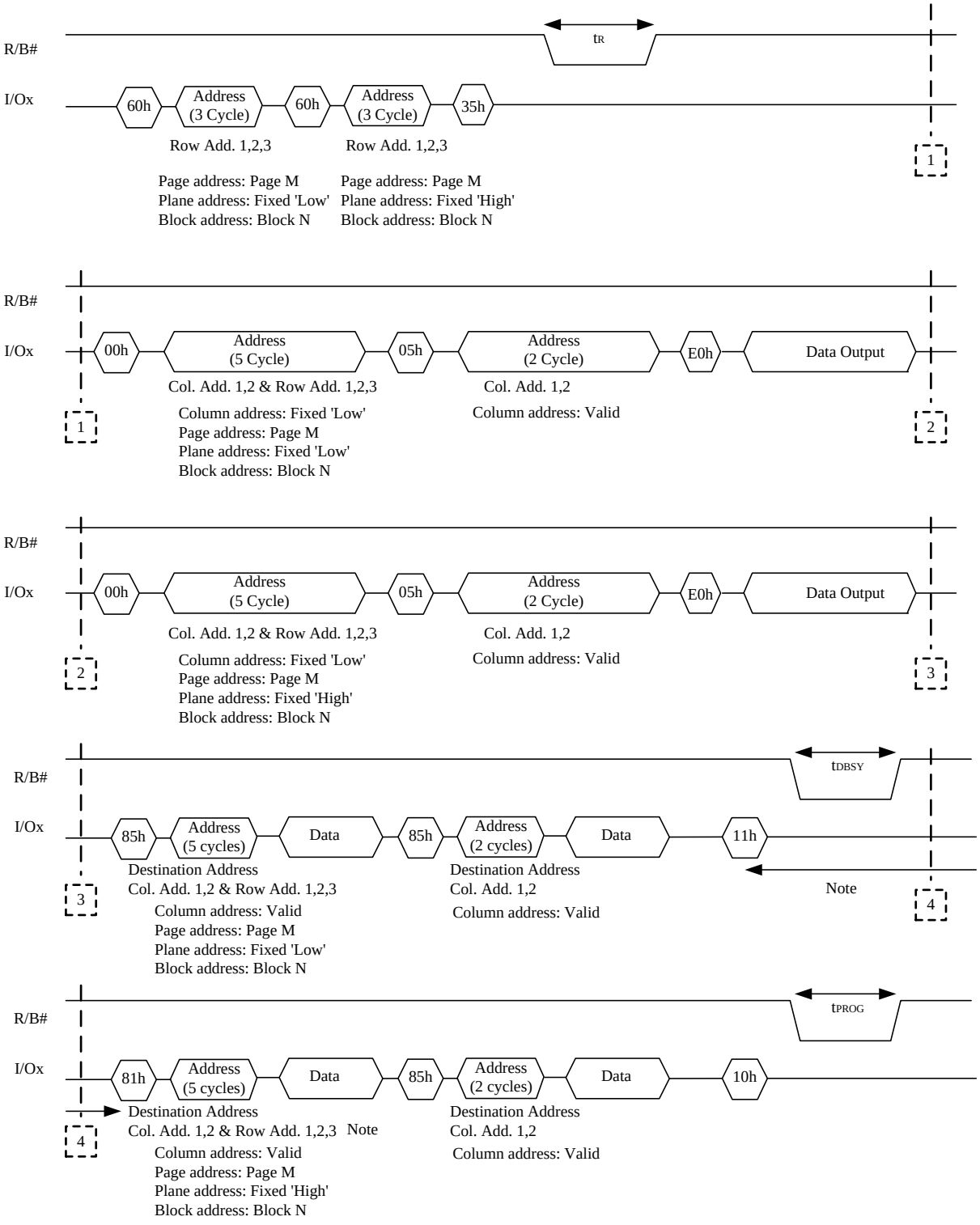
(1): Two-Plane Read for Copy Back
(2): Two-Plane Random Data Out
(3): Two-Plane Copy Back Program

Command Sequence of Two-plane Copy-Back Program

Note: 1. Copy Back Program operation is allowed only within the same memory plane.

2. Any command between 11h and 81h is prohibited except 70h/F1h and FFh.

Two-plane Copy-Back Program with Random Data Input



Two-plane Copy-Back Program with Random Data Input

Note: 1. Copy Back Program operation is allowed only within the same memory plane.

2. Any command between 11h and 81h is prohibited except 70h/F1h and FFh.

ID Definition Table

90 ID : Access command = 90H

Option	Maker Code	Device Code	3rd Cycle	4th Cycle	5th Cycle	6th Cycle	7th ~10th Cycle
X8	C8	D3h	90h	19h	34h	01h	7Fh

	Description
1st Byte	Maker Code (together with the continuation code in the 5th~10th bytes)
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Page, etc
4th Byte	Page Size, Block Size, Redundant Area
5th Byte	Plane Number, ECC level, organization
6th Byte	Device Technology, EDO, Interface
7th Byte	JEDEC Maker Code Continuation Code, 7Fh
8th Byte	JEDEC Maker Code Continuation Code, 7Fh
9th Byte	JEDEC Maker Code Continuation Code, 7Fh
10th Byte	JEDEC Maker Code Continuation Code, 7Fh

3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between Multiple Chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	2KB 4KB 8KB Reserved							0 0 1 1	0 1 0 1
Block Size (w/o redundant area)	128KB 256KB 512KB 1MB Reserved Reserved Reserved Reserved	0 0 0 0 1 1 1 1		0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Redundant Area Size (Byte/Page Size)	Reserved 128B 218B Reserved Reserved Reserved Reserved Reserved		0 0 0 0 1 1 1 1			0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1		

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
ECC Level	1bit/512B 2bit/512B 4bit/512B 8bit/512B 16bit/512B Reserved Reserved Reserved		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 1 0 0 1 0 1				
Reserved		0						0	0

6th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0

Device Version	50nm 40nm Reserved Reserved Reserved Reserved Reserved Reserved						0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 0
EDO	Not Support Support		0 1						
Interface	SDR DDR	0 1							
Reserved				0	0	0			

7th ~10th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
JEDEC Maker Code Continuation Code	7F	0	1	1	1	1	1	1	1

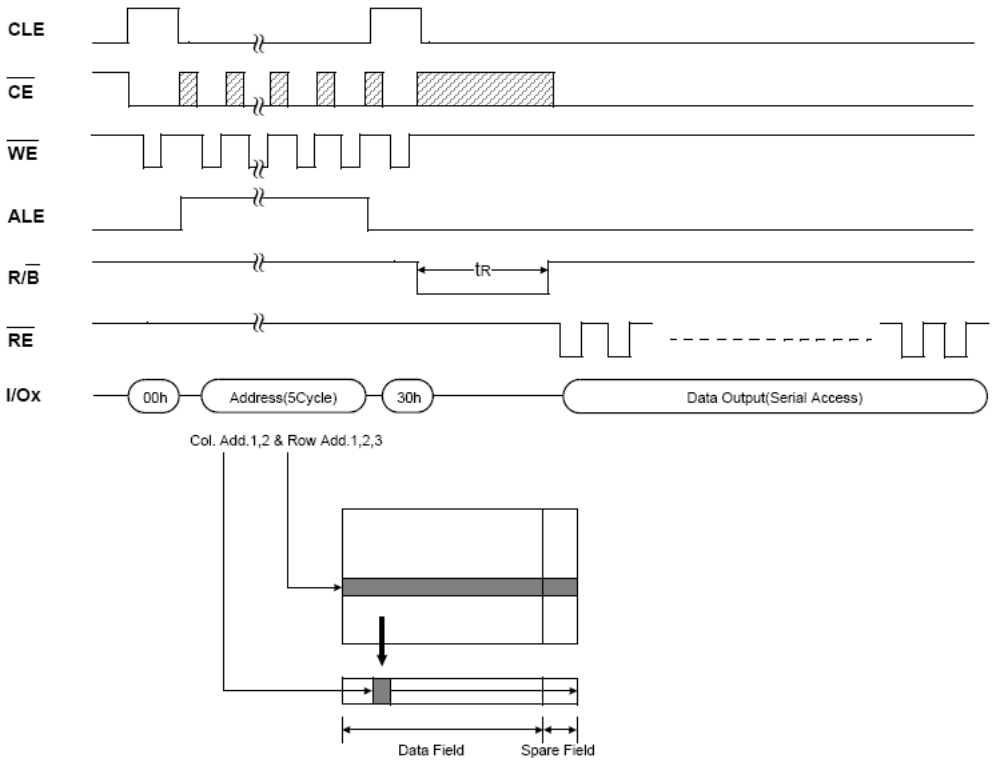
Device Operation

Page Read

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h command, five-cycle address, and 30h command. After initial power up, the 00h command can be skipped because it has been latched in the command register. The 4K Byte of data on a page are transferred to cache registers via data registers within t_R. Host controller can detect the completion of this data transfer by checking the R/B# output. Once data in the selected page have been loaded into cache registers, each Byte can be read out in 30ns cycle time by continuously pulsing RE#. The repetitive high-to-low transitions of RE# clock signal make the device output data starting from the designated column address to the last column address.

The device can output data at a random column address instead of sequential column address by using the Random Data Output command. Random Data Output command can be executed multiple times in a page.

A page read sequence is illustrated in Figure below, where column address, page address are placed in between commands 00h and 30h. After t_R read time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 30h. Host controller can toggle RE# to access data starting with the designated column address and their successive bytes.



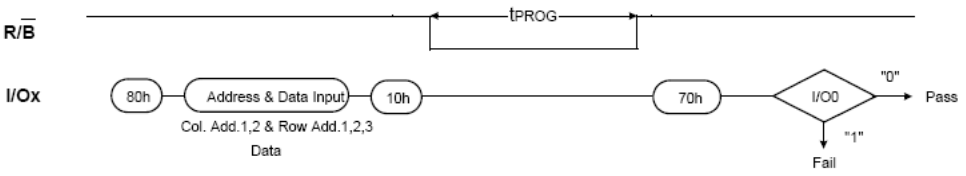
Read Operation

Page Program

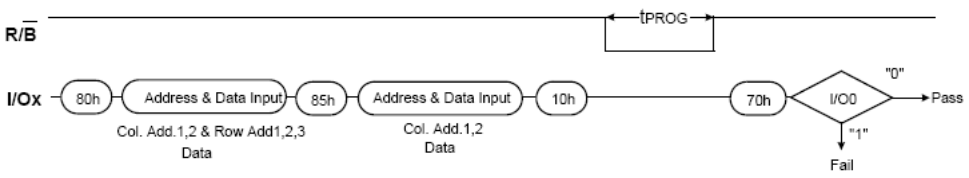
The device is programmed based on the unit of a page, and consecutive partial page programming on one page without intervening erase operation is strictly prohibited. Addressing of page program operations within a block should be in sequential order. A complete page program cycle consists of a serial data input cycle in which up to 4,314byte of data can be loaded into data register via cache register, followed by a programming period during which the loaded data are programmed into the designated memory cells.

The serial data input cycle begins with the Serial Data Input command (80h), followed by a five-cycle address input and then serial data loading. The bytes not to be programmed on the page do not need to be loaded. The column address for the next data can be changed to the address follows Random Data Input command (85h). Random Data Input command may be repeated multiple times in a page. The Page Program Confirm command (10h) starts the programming process. Writing 10h alone without entering data will not initiate the programming process. The internal write engine automatically executes the corresponding algorithm and controls timing for programming and verification, thereby freeing the host controller for other tasks. Once the program process starts, the host controller can detect the completion of a program cycle by monitoring the R/B# output or reading the Status bit (I/O6) using the Read Status command. Only Read Status and Reset commands are valid during programming. When the Page Program operation is completed, the host controller can check the Status bit (I/O0) to see if the Page Program operation is successfully done. The command register remains the Read Status mode unless another valid command is written to it.

A page program sequence is illustrated in Figure below, where column address, page address, and data input are placed in between 80h and 10h. After t_{PROG} program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.



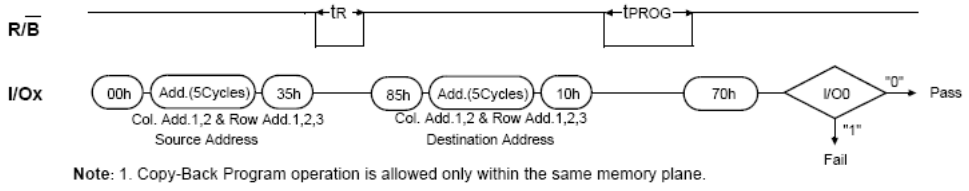
Program & Read Status Operation



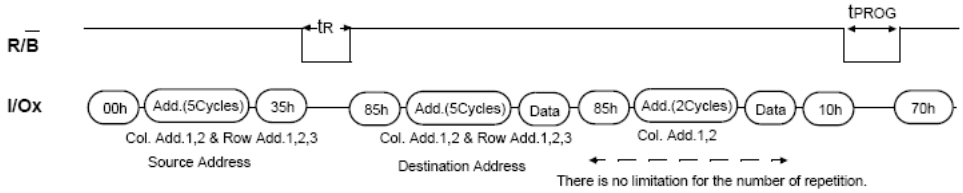
Random Data Input In a Page

Copy-Back Program

Copy-Back Program is designed to efficiently copy data stored in memory cells without time-consuming data reloading when there is no bit error detected in the stored data. The benefit is particularly obvious when a portion of a block is updated and the rest of the block needs to be copied to a newly assigned empty block. Copy-Back operation is a sequential execution of Read for Copy-Back and of Copy-Back Program with Destination address. A Read for Copy-Back operation with “35h” command and the Source address moves the whole 4,314byte data into the internal buffer. The host controller can detect bit errors by sequentially reading the data output. Copy-Back Program is initiated by issuing Page-Copy Data-Input command (85h) with Destination address. If data modification is necessary to correct bit errors and to avoid error propagation, data can be reloaded after the Destination address. Data modification can be repeated multiple times as shown in Figure below. Actual programming operation begins when Program Confirm command (10h) is issued. Once the program process starts, the Read Status command (70h) may be entered to read the status register. The host controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Status Bit (I/O0) may be checked. The command register remains Read Status mode until another valid command is written to it.



Copy-Back Program Operation

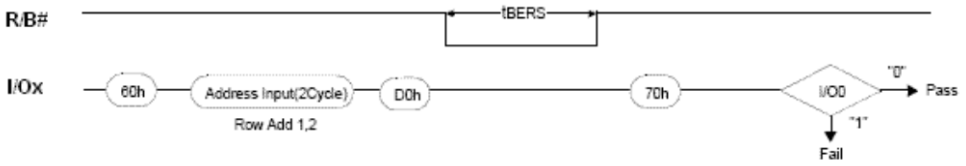


Copy-Back Program Operation with Random Data Input

Block Erase

The block-based Erase operation is initiated by an Erase Setup command (60h), followed by a three-cycle row address, in which only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command (D0h) following the row address starts the internal erasing process. The two-step command sequence is designed to prevent memory content from being inadvertently changed by external noise.

At the rising edge of WE# after the Erase Confirm command input, the internal control logic handles erase and erase-verify. When the erase operation is completed, the host controller can check Status bit (I/O0) to see if the erase operation is successfully done. Figure below illustrates a block erase sequence, and the address input (the first page address of the selected block) is placed in between commands 60h and D0h. After t_{BERASE} erase time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after D0h to check the execution status of erase operation.



Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. These two commands allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycles.

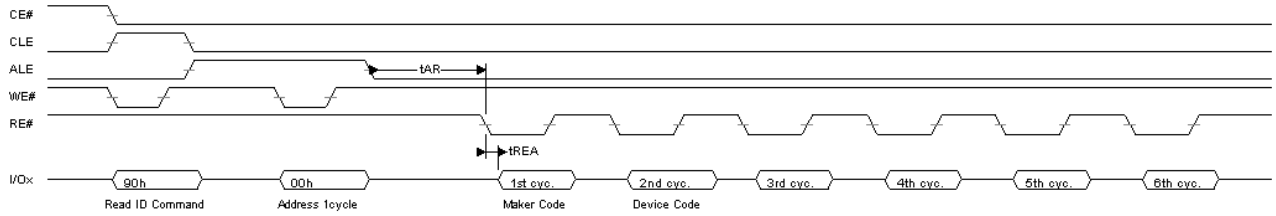
Status Register Coding

I/O	Page Program	Block Erase	Read	Cache Read	Definition
I/O 0	Pass/Fail	Pass/Fail	NA	NA	Pass : 0 Fail : 1
I/O 1	NA	NA	NA	NA	Don't cared
I/O 2	NA	NA	NA	NA	Don't cared
I/O 3	NA	NA	NA	NA	Don't cared
I/O 4	NA	NA	NA	NA	Don't cared
I/O 5	NA	NA	NA	True Read/Busy	Busy : 0

					Ready : 1
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Cache Read/Busy	Busy : 0 Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected :0 Not Protected : 1

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure below shows the operation sequence.



Device ID

Part No.	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle	6th Cycle
PSU8GA30AT	C8h	D3h	90h	19h	34h	01h

Reset

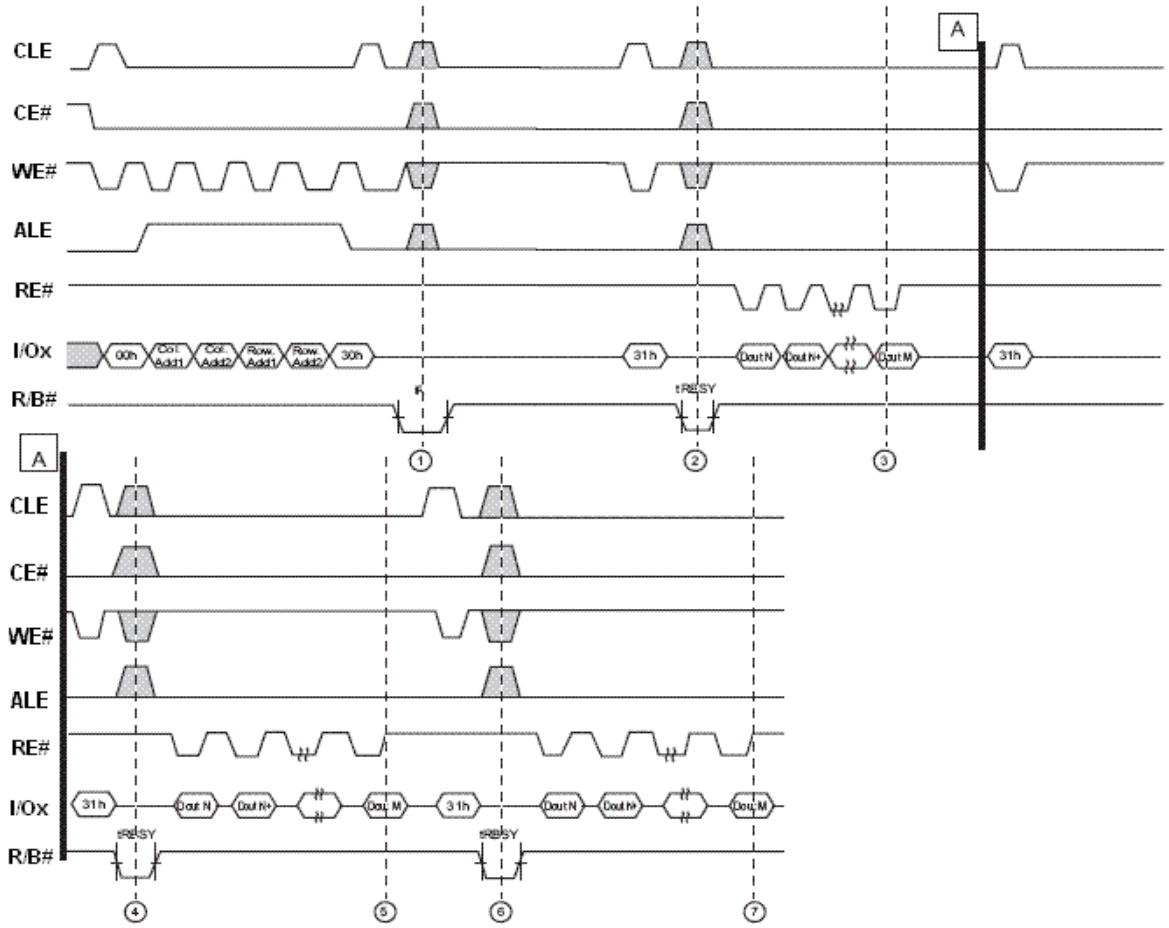
The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin changes to low for t_{RST} after the Reset command is written. Refer to Figure below.

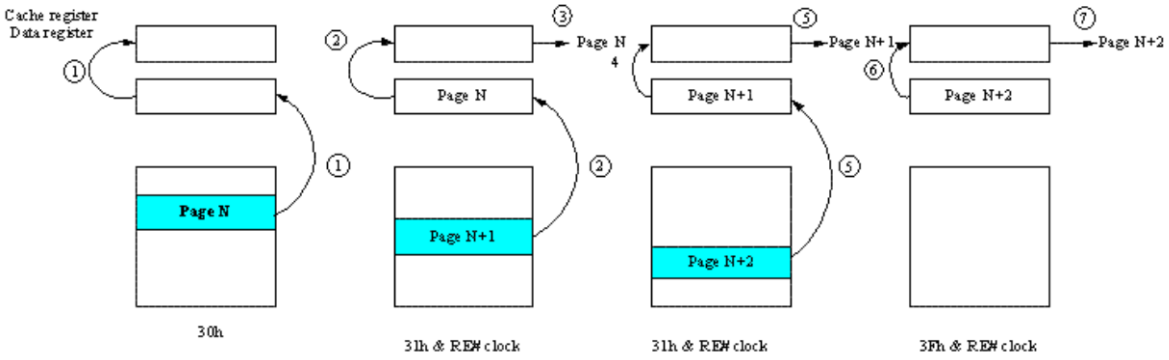
	After Power-up	After Reset
Operation Mode	00h Command is latched	Waiting for next command

Device Status

Cache Read

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of t_{DCBSYR}, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.

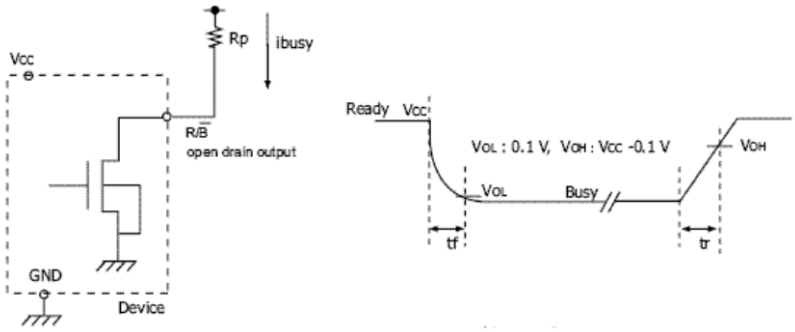


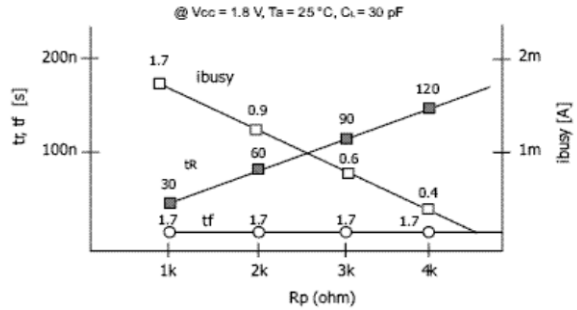


Read/Busy#

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transition to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B#) and current drain during busy (ibusy) , an appropriate value can be obtained with the following reference chart below. Its value can be determined by the following guidance.

Read/Busy# Pin Electrical Specifications





Rp value guidence

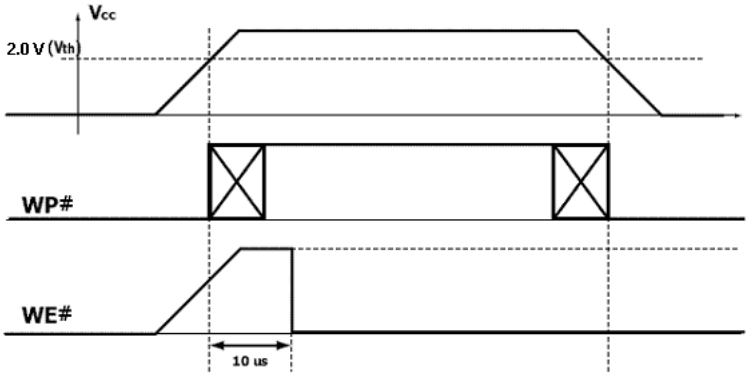
$$Rp\,(min) = \frac{Vcc\,(Max.) - VOL\,(Max.)}{IOL + \sum IL} = \frac{1.85\ V}{3\ mA + \sum IL}$$

where IL is the sum of the iput currents of all devices tied to the R/B# pin

Rp(max) is determined by maximum permissible limit of tr

Data Protection & Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.0V. WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure below. The two steps command sequence for program/erase provides additional software protection.

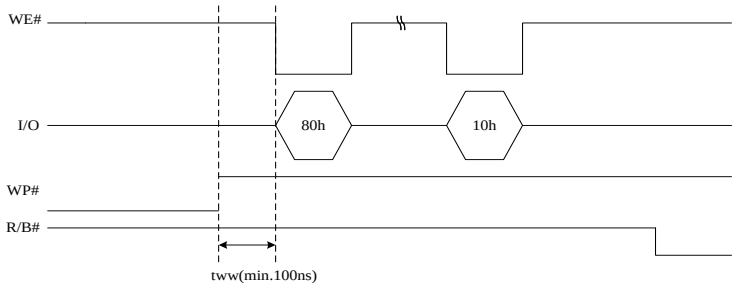


AC Waveforms for Power Transition

Write Protect Operation

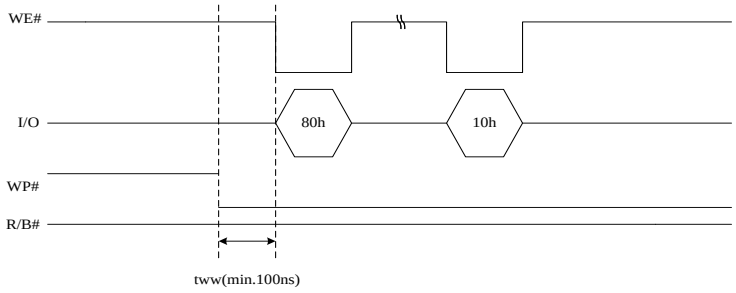
Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Enable Programming

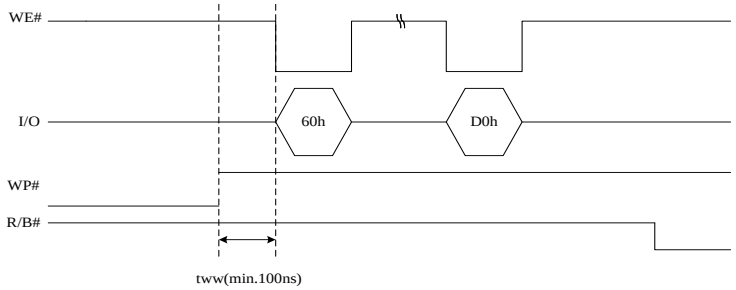


NOTE: WP# keeps “High” until programming finish

Disable Programming



Enable Erasing



NOTE: WP# keeps “High” until erasing finish

Disable Erasing