PSoC® 6 MCU: PSoC 61 Datasheet

Programmable System-on-Chip (PSoC®)

General Description

PSoC® is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with Arm® Cortex® CPUs (single and multi-core). The PSoC 6 product family, based on an ultra low-power 40-nm platform, is a combination of a dual-core microcontroller with low-power Flash technology and digital programmable logic, high-performance analog-to-digital and digital-to-analog conversion, low-power comparators, and standard communication and timing peripherals.

Features

32-bit Dual Core CPU Subsystem

- 150-MHz Arm Cortex-M4F CPU with single-cycle multiply (Floating Point and Memory Protection Unit) for user application
- 100-MHz Cortex M0+ CPU with single-cycle multiply and MPU for System functions (not user programmable)
- User-selectable core logic operation at either 1.1 V or 0.9 V
- Inter-processor communication supported in hardware
- 8 KB 4-way set-associative Instruction Caches for the M4 and M0+ CPUs respectively
- Active CPU power consumption slope with 1.1-V core operation for the Cortex M4 is 40 µA/MHz and 20 µA/MHz for the Cortex M0+, both at 3.3-V chip supply voltage with the internal buck regulator
- Active CPU power consumption slope with 0.9-V core operation for the Cortex M4 is 22 µA/MHz and 15 µA/MHz for the Cortex M0+, both at 3.3-V chip supply voltage with the internal buck regulator
- Two DMA controllers with 16 channels each

Flexible Memory Subsystem

- 1 MB Application Flash with 32 KB EEPROM area and 32 KB Secure Flash
- 128-bit wide Flash accesses reduce power
- SRAM with Selectable Retention Granularity
- 288 KB integrated SRAM
- 32 KB retention boundaries (can retain 32 KB to 288 KB in 32 KB increments)
- OTP E-Fuse memory for validation and security

Low-Power 1.7-V to 3.6-V Operation

- Active, Low-power Active, Sleep, Low-power Sleep, Deep Sleep, and Hibernate modes for fine-grained power management
- Deep Sleep mode current with 64 KB SRAM retention is 7 µA with 3.3-V external supply and internal buck
- On-chip Single-In Multiple Out (SIMO) DC-DC Buck converter, <1 µA quiescent current
- Backup domain with 64 bytes of memory and Real-time Clock (RTC)

Flexible Clocking Options

- On-chip crystal oscillators (High-speed, 4 to 33 MHz, and Watch crystal, 32 kHz)
- Phase-locked Loop (PLL) for multiplying clock frequencies
- 8 MHz Internal Main Oscillator (IMO) with ±2% accuracy
- Ultra low-power 32-kHz Internal Low-speed Oscillator (ILO) with ±10% accuracy
- Frequency Locked Loop (FLL) for multiplying IMO frequency

Serial Communication

- Nine independent run-time reconfigurable serial communication blocks (SCBs), each is software configurable as I^2C, SPI, or UART
- USB Full-Speed Dual-role Host and Device interface

Timing and Pulse-Width Modulation

- Thirty-two Timer/Counter Pulse-Width Modulator (TCPWM) blocks
- Center-aligned, Edge, and Pseudo-random modes
- Comparator-based triggering of Kill signals

Up to 104 Programmable GPIOs

- Drive modes, strengths, and slew rates are programmable
- Six overvoltage tolerant (OVT) pins

Packages

- 124-BGA (Qualification in process)
- 80-WLCSP (in 0.33 and 0.43 mm heights). Thin 80-WLCSP package (0.33 mm height) qualification is in process.

Audio Subsystem

- I2S Interface; up to 192 ksps Word Clock
- Two PDM channels for stereo digital microphones

QSPI Interface

- Execute-In-Place (XIP) from external Quad SPI Flash
- On-the-fly encryption and decryption
- 4 KB QSPI cache for greater XIP performance with lower power
- Supports 1, 2, 4, and Dual-Quad interfaces

Errata: For information on silicon errata, see "Revision History" on page 63. Details include trigger conditions, devices affected, and proposed workaround.

Programmable Analog

- 12-bit 1 Msps SAR ADC with differential and single-ended modes and 16-Channel Sequencer with signal averaging
- One 12-bit voltage mode DAC with < 5-µs settling time
- Two opamps with low-power operation modes
- Two low-power comparators that operate in Deep Sleep and Hibernate modes.
- Built-in temp sensor connected to ADC

Programmable Digital

- 12 programmable logic blocks, each with eight Macrocells and an 8-bit data path (called universal digital blocks or UDBs)
- Usable as drag-and-drop Boolean primitives (gates, registers), or as Verilog programmable blocks
- Cypress-provided peripheral component library using UDBs with common functions such as SDIO, Communication Peripherals such as LIN, UART, SPI, I2C, S/PDIF, Waveform Generator, Pseudo-Random Sequence (PRS) generation, and many other functions.
- Smart I/O (Programmable I/O) blocks enable Boolean operations on signals coming from, and going to, GPIO pins
- Two ports with Smart_IO blocks, capability are provided; these are available during Deep Sleep

Capacitive Sensing

- Cypress Capacitive Sigma-Delta (CSD) provides best-in-class SNR, liquid tolerance, and proximity sensing
- Mutual Capacitance sensing (Cypress CSX) with dynamic usage of both Self and Mutual sensing
- Wake on Touch with very low current
- Cypress-supplied software component makes capacitive sensing design fast and easy
- Automatic hardware tuning (SmartSense™)

Energy Profiler

- Block that provides history of time spent in different power modes
- Allows software energy profiling to observe and optimize energy consumption

PSoC Creator Design Environment

- Integrated Development Environment provides schematic design entry and build (with analog and digital automatic routing) and code development and debugging
- Applications Programming Interface (API Component) for all fixed-function and programmable peripherals

Industry-Standard Tool Compatibility

- After schematic entry, development can be done with Arm-based industry-standard development tools
- Configure in PSoC Creator and export to Arm/Keil or IAR IDEs for code development and debugging
- Supports industry standard Arm Trace Emulation Trace Module

Security Built into Platform Architecture

- Multi-faceted secure architecture based on ROM-based root of trust
- Secure Boot uninterruptible until system protection attributes are established
- Authentication during boot using hardware hashing
- Step-wise authentication of execution images
- Secure execution of code in execute-only mode for protected routines
- All Debug and Test ingress paths can be disabled

Cryptography Accelerators

- Hardware acceleration for Symmetric and Asymmetric cryptographic methods (AES, 3DES, RSA, and ECC) and Hash functions (SHA-512, SHA-256)
- True Random Number Generator (TRNG) function

More Information

Cypress provides a wealth of data at www.cypress.com to help you select the right PSoC device and quickly and effectively integrate it into your design. The following is an abbreviated list of resources for PSoC 6 MCU:

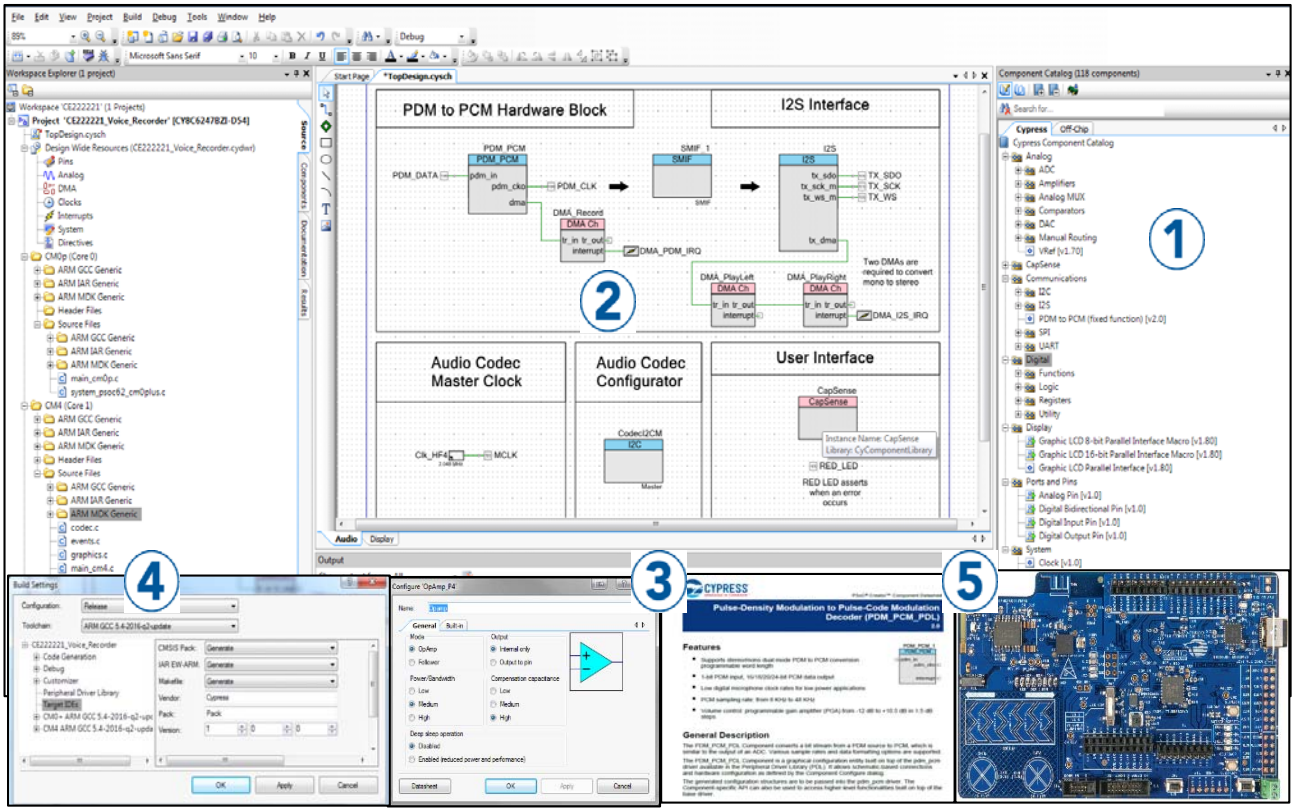
- **Overview**: PSoC Portfolio, PSoC Roadmap
- **Product Selectors**: PSoC 6 MCU Page
- **Application Notes** cover a broad range of topics, from basic to advanced level, and include the following:
  - AN210781: Getting Started with PSoC 6 MCU BLE
  - AN218241: PSoC 6 MCU Hardware Design Considerations
  - AN213924: PSoC 6 MCU Bootloader Guide
  - AN215656: PSoC 6 MCU Dual-Core CPU System Design
  - AN219434: Importing PSoC Creator Code into an IDE
  - AN219528: PSoC 6 MCU Power Reduction Techniques
  - AN221111: PSoC 6 MCU: Creating a Secure System
- Code Examples provides PSoC Creator example projects for different product features and usage.
- Technical Reference Manuals (TRMs) provide detailed descriptions of PSoC 6 MCU architecture and registers.
- Development Tools
  - CY8CKIT-062-Wi-Fi-/BT supports the PSoC 62 series MCU with WiFi and Bluetooth connectivity.
  - CY8CKIT-062-BLE supports the PSoC 63 series MCU with Bluetooth Low-Energy (BLE) connectivity.
- Training Videos: Visit www.cypress.com/training for a wide variety of video training resources on PSoC Creator

PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables you to design hardware and firmware systems concurrently, based on PSoC 6 MCU. As shown below, with PSoC Creator, you can:

1. Explore the library of 200+ Components in PSoC Creator
2. Drag and drop Component icons to complete your hardware system design in the main design workspace
3. Configure Components using the Component Configuration Tools and the Component datasheets
4. Co-design your application firmware and hardware in the PSoC Creator IDE or build project for 3rd party IDE
5. Prototype your solution with the PSoC 6 Pioneer Kits.If a design change is needed, PSoC Creator and Components enable you to make changes on the fly without the need for hardware revisions.

Figure 1. PSoC Creator Schematic Entry and Components



Contents

Blocks and Functionality

The PSoC 61 block diagram is shown in Figure 2. There are four major subsystems: CPU subsystem, system resources, peripheral blocks, and I/O subsystem.

Figure 2. Block Diagram

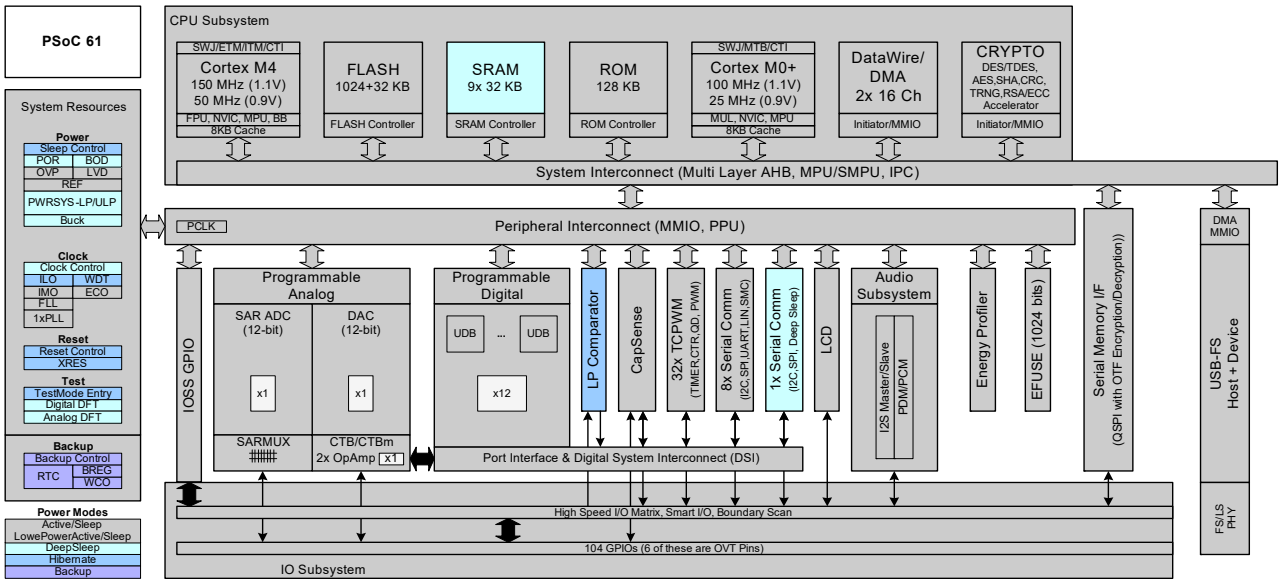


Figure 2 shows the subsystems of the chip and gives a very simplified view of their inter-connections (Multi-layer AHB is used in practice). The color-coding shows the lowest power mode where the particular block is still functional (for example, LP Comparator is functional in Deep Sleep mode).

PSoC 61 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for PSoC 61 devices. The SWJ (SWD and JTAG) interface is fully compatible with industry-standard third party probes. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 61 family provides a very high level of security.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing at-tacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. The security level is a trade-off the customer can make.

Functional Definition

CPU and Memory Subsystem

CPU

The CPU subsystem in the PSoC 61 consists of two Arm Cortex cores and their associated busses and memories: M4 with Floating-point unit and Memory Protection Units (FPU and MPU) and an M0+ with an MPU. The Cortex M4 and M0+ have 8 KB Instruction Caches (I-Cache) with 4-way set associativity. This subsystem also includes independent DMA controllers with 32 channels each, a Cryptographic accelerator block, 1 MB of on-chip Flash, 288 KB of SRAM, and 128 KB of ROM. The Cortex M0+ provides a secure, un-interruptible Boot function. This guarantees that post-Boot, system integrity is checked and privileges enforced. Shared resources can be accessed through the normal Arm multi-layer bus arbitration and exclusive accesses are supported by an Inter-Processor Communication (IPC) scheme, which implements hardware semaphores and protection. Active power consumption for the Cortex M4 is 26 µA/MHz and 17 µA/MHz for the Cortex M0+, both at 3V chip supply voltage with the internal buck enabled and at 0.9 V internal supply. The Cortex M4 is usable for user Application code. The Cortex M0+ is used for System functions (not user programmable). The Cortex M4 can operate at up to 150 MHz and the M0+ up to 100 MHz. Note that for M4 speeds above 100 MHz, the M0+ and Bus peripherals are limited to half the speed of the M4. Thus, for the M4 running at 150 MHz, the M0+ and peripherals are limited to 75 MHz.

DMA Controllers

There are two DMA controllers with 16 channels each. They support independent accesses to peripherals using the AHB Multi-layer bus.

Flash

The PSoC 6 A-M has a 1 MB flash module with additional 32 KB of Flash that can be used for EEPROM emulation for longer retention and a separate 32 KB block of Flash that can be securely locked and is only accessible via a key lock that cannot be changed (One Time Programmable).

SRAM with 32 KB Retention Granularity

There is 288 KB of SRAM memory, which can be fully retained or retained in increments of user-designated 32 KB blocks.

SROM

There is a supervisory 128 KB ROM that contains boot and configuration routines. This ROM will guarantee Secure Boot if authentication of User Flash is required.

One-Time-Programmable (OTP) eFuse

This memory can be used to store a unique and unalterable Identifier on a per-chip basis. It can also be used to store a hash value used to verify authenticity of flash contents, or other user-defined content.

System Resources

Power System

The power system provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (Brown-Out Detect (BOD)) when the power supply drops below specified levels. The design will guaranteed safe chip operation between power supply voltage dropping below specified levels (for example, below 1.7 V) and the Reset occurring. There are no voltage sequencing requirements. The VDD core logic supply (1.7 to 3.6 V) will feed an on-chip buck, which will produce the core logic supply of either 1.1 V or 0.9 V selectable. Depending on the frequency of operation, the buck converter will have a quiescent current of <1 µA. A separate power domain called Backup is provided; note this is not a power mode. This domain is powered from the VBACKUP domain and includes the 32-kHz Watch Crystal Oscillator (WCO), RTC, and backup registers. It is connected to VDD when not used as a backup domain. Port 0 is powered from this supply. Pin 5 of Port 0 (P0.5) can be assigned as a PMIC wakeup output (timed by the RTC); P0.5 is driven to resistive pullup mode by default.

Clock System

The PSoC 61 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 61 consists of the Internal Main Oscillator (IMO) and the Internal Low-speed Oscillator (ILO), crystal oscillators (ECO and WCO), PLL, FLL, and provision for an external clock. An FLL will provide fast wake-up at high clock speeds without waiting for a PLL lock event (which can take up to 50 µs). Clocks may be buffered and brought out to a pin on a Smart I/O port.

The 32-kHz oscillator is trimmable to within 2 ppm using a higher accuracy clock. The ECO will deliver ±20 ppm accuracy and will use an external crystal.

IMO Clock Source

The IMO is the primary source of internal clocking in PSoC 61. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 8 MHz. IMO tolerance is ±2% and its current consumption is less than 10 µA.

ILO Clock Source

The ILO is a very low power oscillator, nominally 32 kHz, which may be used to generate clocks for peripheral operation in Deep Sleep and Hibernate modes. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer (WDT)

A WDT is implemented in the clock block running from the ILO or from the WCO; this allows watchdog operation during Deep Sleep and Hibernate modes, and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Clock Dividers

Integer and Fractional clock dividers are provided for peripheral use and timing purposes. The clock dividers are 16 and 24 bits in length to allow very fine clock control.

Reset

The PSoC 61 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the Reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

Analog Blocks

12-bit SAR ADC

The 12-bit, 1 Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to ±1%) and by providing the choice of three internal voltage references, V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V), as well as an external reference through a GPIO pin. The Sample-and-Hold (S/H) aperture is programmable; it allows the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision provided appropriate references are used and system noise levels permit it. To improve the performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through the selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, the aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware-driven switching. A feature provided by the sequencer is the buffering of each channel to reduce CPU interrupt-service requirements. To accommodate signals with varying source impedances and frequencies, it is possible to have different sample times programmable for each channel. Also, the signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-chip temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 3.6 V.

Temperature Sensor

PSoC 61 has an on-chip temperature sensor. This consists of a diode, which is biased by a current source that can be disabled to save power. The temperature sensor is connected to the ADC, which digitizes the reading and produces a temperature value by using a Cypress-supplied software that includes calibration and linearization.

12-bit DAC

There is a 12-bit voltage mode DAC on the chip, which can settle in less than 5 µs. The DAC may be driven by the DMA controllers to generate user-defined waveforms. The DAC output from the chip can either be the resistive ladder output (highly linear near ground) or a buffered output.

Continuous Time Block (CTBm) with Two Opamps

This block consists of two opamps, which have their inputs and outputs connected to fixed pins and have three power modes and a comparator mode. The outputs of these opamps can be used as buffers for the SAR inputs. The non-inverting inputs of these opamps can be connected to either of two pins, thus allowing independent sensors to be used at different times. The pin selection can be made via firmware. The opamps can be set to one of the four power levels; the lowest level allowing operation in Deep Sleep mode in order to preserve lower performance Continuous-Time functionality in Deep Sleep mode. The DAC output can be buffered through an opamp.

Low-Power Comparators

PSoC 61 has a pair of low-power comparators, which can also operate in Deep Sleep and Hibernate modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during Deep Sleep and Hibernate modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode (Hibernate) where the system wake-up circuit is activated by a comparator-switch event.

Programmable Digital

Smart I/O

There are two Smart I/O blocks, which allow Boolean operations on signals going to the GPIO pins from the subsystems of the chip or on signals coming into the chip. Operation can be synchronous or asynchronous and the blocks operate in low-power modes, such as Deep Sleep and Hibernate. This allows, for example, detection of logic conditions that can indicate that the CPU should wake up instead of waking up on general I/O interrupts, which consume more power and can generate spurious wake-ups.

Universal Digital Blocks (UDBs) and Port Interfaces

The PSoC 61 has 12 UDBs; the UDB array also provides a switched Digital System Interconnect (DSI) fabric that allows signals from peripherals and ports to be routed to and through the UDBs for communication and control.

Fixed-Function Digital

Timer/Counter/PWM Block

The timer/counter/PWM block consists of 32 counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow the use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor-drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention. There are eight 32-bit counters and 24 16-bit counters.

Serial Communication Blocks (SCB)

PSoC 61 has nine SCBs, which can each implement an I^2C, UART, or SPI interface. One SCB will operate in Deep Sleep with an external clock, this SCB will only operate in Slave mode (requires external clock).

I^2C Mode: The hardware I^2C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce the interrupt overhead and latency for the CPU. It also supports EzI^2C that creates a mailbox address range in the memory of PSoC 61 and effectively reduces the I^2C communication to reading from and writing to an array in the memory. In addition, the block supports a 256-byte FIFO for receive and transmit, which, by increasing the time given for the CPU to read the data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I^2C peripheral is compatible with I^2C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. A 256-byte FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI Secure Simple Pairing (SSP) (essentially adds a start pulse that is used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and supports an EzSPI mode in which the data interchange is reduced to reading and writing an array in memory. The SPI interface operates with up to a 48-MHz SPI Clock.

USB Full-Speed Dual Role Host and Device interface

The PSoC 61 incorporates a dual-role USB Host and Device interface. The device can have up to eight endpoints. A 512 byte SRAM buffer is provided and DMA is supported.

QSPI Interface

A Quad SPI (QSPI) interface (selectable 1, 2, or 4 bits width) is provided running at 80 MHz. This block also supports on-the-fly encryption and decryption to support Execute-In-Place operation at reasonable speeds.

GPIO

PSoC 61 has up to 104 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Hold mode for latching previous state (used for retaining the I/O state in Deep Sleep and Hibernate modes)
- Selectable slew rates for dV/dt-related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it. Six GPIO pins are capable of overvoltage tolerant (OVT) operation where the input voltage may be higher than VDD (these may be used for I^2C functionality to allow powering the chip off while maintaining physical connection to an operating I^2C bus without affecting its functionality).

GPIO pins can be ganged to sink 16 mA or higher values of sink current. GPIO pins may not be pulled up higher than 3.6 V.

Special-Function Peripherals

CapSense

CapSense is supported on all pins in the PSoC 61 through a CapSense Sigma Delta (CSD) block that can be connected to an analog multiplexed bus. Any GPIO pin can be connected to this AMUX bus through an analog switch. CapSense function can thus be provided on any pin or a group of pins in a system under software control. Cypress provides a software component for the CapSense block for ease-of-use.

Shield voltage can be driven on another mux bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CapSense block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and ground to null out power-supply related noise.

The CapSense block has two 7-bit IDACs, which can be used for general purposes if CapSense is not being used (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). A (slow) 10-bit Slope ADC may be realized by using one of the IDACs.

The block can implement Swipe, Tap, Wake-up on Touch (< 3 µA at 1.8 V), mutual capacitance, and other types of sensing functions.

Audio Subsystem

This subsystem consists of an I2S block and two PDM channels. The PDM channels interface to a PDM microphone's bit-stream output. The PDM processing channel provides droop correction and can operate with clock speeds ranging from 384 kHz to 3.072 MHz and produce word lengths of 16 to 24 bits at audio sample rates of up to 48 ksps.

The I2S interface supports both Master and Slave modes with Word Clock rates of up to 192 ksps (8-bit to 32-bit words).

Pinouts

Table 1. 124-BGA and 80-WLCSP Pin Description

124-BGA		80-WLCSP	
Pin	Name	Pin	Name
A2	VCCD	A10	VCCD
A1	VDDD	B11	VDDD
D1	VBACKUP	D11	VBACKUP
E3	P0.0	C10	P0.0
E2	P0.1	D9	P0.1
E1	P0.2	E10	P0.2
F3	P0.3	F9	P0.3
F2	P0.4	G8	P0.4
G3	P0.5	F11	P0.5
G3	P0.5	F11	P0.5
F1	XRES	G10	XRES
G2	P1.0	H11	P1.0
G1	P1.1	H9	P1.1
H3	P1.2		
H2	P1.3		
H1	P1.4	K9	P1.4
J3	P1.5	J10	P1.5
B12, C3, D4, D10, K4, K10	VSS	R8	VSS
J1	VDD_NS	K11	VDD_NS
J2	VIND1	L10	VIND1
K2	VIND2	M11	VIND2
K3	VBUCK1	N10	VBUCK1
K1	VRF		
M1	VDDUSB	P11	VDDUSB
L1	USBDM	P9	USBDM
L2	USBDP	R10	USBDP
M2	P2.0		
N2	P2.1		
L3	P2.2		
M3	P2.3		
N3	P2.4		
N1	P2.5		
M4	P2.6		
N4	P2.7		
L5	P3.0		
L4	VDDIOR	K11	VDD_NS
L4	VDDIOR	K11	VDD_NS
M5	P3.1		

Table 1. 124-BGA and 80-WLCSP Pin Description *(continued)*

124-BGA		80-WLCSP	
Pin	Name	Pin	Name
N5	P3.2		
L6	P3.3		
M6	P3.4		
N6	P3.5		
L7	P4.0		
M7	P4.1		
N7	P5.0	M9	P5.0
L8	P5.1	N8	P5.1
M8	P5.2	R6	P5.2
N8	P5.3	P7	P5.3
L9	P5.4	L8	P5.4
M9	P5.5	M7	P5.5
B12, C3, D4, D10, K4, K10	VSS	P5	VSS
N9	P5.6	R4	P5.6
N10	P5.7	N6	P5.7
M10	P6.0	J8	P6.0
L10	P6.1	K7	P6.1
L11	P6.2	L6	P6.2
M11	P6.3	R2	P6.3
N11	P6.4	P3	P6.4
M12	P6.5	N4	P6.5
N12	P6.6	M5	P6.6
M13	P6.7	J6	P6.7
L13	P7.0	N2	P7.0
L12	P7.1	M3	P7.1
K13	P7.2	L4	P7.2
N13	P7.3	K5	P7.3
K11	P7.4		
J13	P7.5		
J12	P7.6		
J11	P7.7	L2	P7.7
K12	VDDIO1	M1	VDDIO1
H13	P8.0	H3	P8.0
H12	P8.1	K1	P8.1
H11	P8.2	K3	P8.2
G13	P8.3	J4	P8.3
G12	P8.4	J2	P8.4
G11	P8.5		
F13	P8.6		
F12	P8.7		

Table 1. 124-BGA and 80-WLCSP Pin Description *(continued)*

124-BGA		80-WLCSP	
Pin	**Name**	**Pin**	**Name**
B12,C3,D4,D10,K4,K10	VSS	D1	VSS
A12	VDDA	F1	VDDA
E11	P9.0	H1	P9.0
E12	P9.1	G2	P9.1
E13	P9.2	E2	P9.2
F11	P9.3	C2	P9.3
D13	P9.4	F3	P9.4
D12	P9.5		
D11	P9.6		
C13	P9.7	A2	P9.7
B13	VREF		
A13	VDDIOA	F1	VDDA
A12	VDDA	F1	VDDA
C12	P10.0	G4	P10.0
A11	P10.1	H5	P10.1
B11	P10.2		
C11	P10.3		
A10	P10.4	B3	P10.4
B10	P10.5	D3	P10.5
C10	P10.6		
A9	P10.7		
B9	P11.0	E4	P11.0
C9	P11.1	F5	P11.1
A8	P11.2	G6	P11.2
B8	P11.3	A4	P11.3

Table 1. 124-BGA and 80-WLCSP Pin Description *(continued)*

124-BGA		80-WLCSP	
Pin	**Name**	**Pin**	**Name**
C8	P11.4	C4	P11.4
A7	P11.5	B5	P11.5
B12, C3, D4, D10, K4, K10	VSS	A8	VSS
B7	P11.6	D5	P11.6
C7	P11.7	C6	P11.7
C4	VDDIO0	A6	VDDIO0
A6	P12.0	B7	P12.0
B6	P12.1	D7	P12.1
C6	P12.2	C8	P12.2
A5	P12.3	B9	P12.3
B5	P12.4	E6	P12.4
C5	P12.5	E8	P12.5
A4	P12.6	F7	P12.6
B4	P12.7	H7	P12.7
B1	P13.0		
A3	P13.1		
B3	P13.2		
B2	P13.3		
C2	P13.4		
C1	P13.5		
D3	P13.6		
D2	P13.7		

The correspondence of power supplies to ports by package type is as follows:

- P0: VBACKUP
- P1: VDDD. Port 1 GPIO Pins are Over-Voltage Tolerant (OVT).
- P2, P3, P4: VDDIOR
- P5, P6, P7, P8: VDDIO1
- P9, P10: VDDIO, VDDA (VDDIO and VDDA must be connected together on the PCB)
- P11, P12, P13: VDDIO0
- P14: VDDUSB

Each Port Pin has multiple alternate functions. These are defined in Table 2.

Table 2. Multiple Alternate Functions[1]

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P0.0	tcpwm[0].line[0]:0	tcpwm[1].line[0]:0		srss.ext_clk:0				scb[0].spi_select1:0			peri.tr_io_input[0]:0						
P0.1	tcpwm[0].line_compl[0]:0	tcpwm[1].line_compl[0]:0						scb[0].spi_select2:0			peri.tr_io_input[1]:0					cpuss.swj_trstn	
P0.2	tcpwm[0].line[1]:0	tcpwm[1].line[1]:0				scb[0].uart_rx:0	scb[0].i2c_scl:0	scb[0].spi_mosi:0									
P0.3	tcpwm[0].line_compl[1]:0	tcpwm[1].line_compl[1]:0				scb[0].uart_tx:0	scb[0].i2c_sda:0	scb[0].spi_miso:0									
P0.4	tcpwm[0].line[2]:0	tcpwm[1].line[2]:0				scb[0].uart_rts:0		scb[0].spi_clk:0				peri.tr_io_output[0]:2					
P0.5	tcpwm[0].line_compl[2]:0	tcpwm[1].line_compl[2]:0		srss.ext_clk:1		scb[0].uart_cts:0		scb[0].spi_select0:0				peri.tr_io_output[1]:2					
P1.0	tcpwm[0].line[3]:0	tcpwm[1].line[3]:0				scb[7].uart_rx:0	scb[7].i2c_scl:0	scb[7].spi_mosi:0			peri.tr_io_input[2]:0						
P1.1	tcpwm[0].line_compl[3]:0	tcpwm[1].line_compl[3]:0				scb[7].uart_tx:0	scb[7].i2c_sda:0	scb[7].spi_miso:0			peri.tr_io_input[3]:0						
P1.2	tcpwm[0].line[4]:4	tcpwm[1].line[12]:1				scb[7].uart_rts:0		scb[7].spi_clk:0									
P1.3	tcpwm[0].line_compl[4]:4	tcpwm[1].line_compl[12]:1				scb[7].uart_cts:0		scb[7].spi_select0:0									
P1.4	tcpwm[0].line[5]:4	tcpwm[1].line[13]:1						scb[7].spi_select1:0									
P1.5	tcpwm[0].line_compl[5]:4	tcpwm[1].line_compl[14]:1						scb[7].spi_select2:0									
P14.0																	
P14.1																	
P2.0	tcpwm[0].line[6]:4	tcpwm[1].line[15]:1				scb[1].uart_rx:0	scb[1].i2c_scl:0	scb[1].spi_mosi:0			peri.tr_io_input[4]:0				bless.mxd_dpslp_ret_switch_hv		
P2.1	tcpwm[0].line_compl[6]:4	tcpwm[1].line_compl[15]:1				scb[1].uart_tx:0	scb[1].i2c_sda:0	scb[1].spi_miso:0			peri.tr_io_input[5]:0				bless.mxd_dpslp_ret_ldo_ol_hv		

Note

1. The notation for a signal is of the form IPName[x].signal_name[u]:y.
   IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
   For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 2. Multiple Alternate Functions[1] *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P2.2	tcpwm[0].line[7]:4	tcpwm[1].line[16]:1				scb[1].uart_rts:0		scb[1].spi_clk:0							bless.mxd_dpslp_buck_en		
P2.3	tcpwm[0].line_compl[7]:4	tcpwm[1].line_compl[16]:1				scb[1].uart_cts:0		scb[1].spi_select0:0							bless.mxd_dpslp_reset_n		
P2.4	tcpwm[0].line[0]:5	tcpwm[1].line[17]:1						scb[1].spi_select1:0							bless.mxd_dpslp_clk_en		
P2.5	tcpwm[0].line_compl[0]:5	tcpwm[1].line_compl[17]:1						scb[1].spi_select2:0							bless.mxd_dpslp_isolate_n		
P2.6	tcpwm[0].line[1]:5	tcpwm[1].line[18]:1						scb[1].spi_select3:0							bless.mxd_dpslp_act_ldo_en		
P2.7	tcpwm[0].line_compl[1]:5	tcpwm[1].line_compl[18]:1													bless.mxd_dpslp_xtal_en		
P3.0	tcpwm[0].line[2]:5	tcpwm[1].line[19]:1				scb[2].uart_rx:1	scb[2].i2c_scl:1	scb[2].spi_mosi:1			peri.tr_io_input[6]:0				bless.mxd_dpslp_dig_ldo_en		
P3.1	tcpwm[0].line_compl[2]:5	tcpwm[1].line_compl[19]:1				scb[2].uart_tx:1	scb[2].i2c_sda:1	scb[2].spi_miso:1			peri.tr_io_input[7]:0		bless.mxd_act_dbus_rx_en				
P3.2	tcpwm[0].line[3]:5	tcpwm[1].line[20]:1				scb[2].uart_rts:1		scb[2].spi_clk:1					bless.mxd_act_dbus_tx_en				
P3.3	tcpwm[0].line_compl[3]:5	tcpwm[1].line_compl[20]:1				scb[2].uart_cts:1		scb[2].spi_select0:1					bless.mxd_act_bpktctl				
P3.4	tcpwm[0].line[4]:5	tcpwm[1].line[21]:1						scb[2].spi_select1:1					bless.mxd_act_txd_rxd				
P3.5	tcpwm[0].line_compl[4]:5	tcpwm[1].line_compl[21]:1						scb[2].spi_select2:1					bless.mxd_dpslp_rcb_data				
P4.0	tcpwm[0].line[5]:5	tcpwm[1].line[22]:1				scb[7].uart_rx:1	scb[7].i2c_scl:1	scb[7].spi_mosi:1			peri.tr_io_input[8]:0		bless.mxd_dpslp_rcb_clk				
P4.1	tcpwm[0].line_compl[5]:5	tcpwm[1].line_compl[22]:1				scb[7].uart_tx:1	scb[7].i2c_sda:1	scb[7].spi_miso:1			peri.tr_io_input[9]:0		bless.mxd_dpslp_rcb_le				

Note

1. The notation for a signal is of the form IPName[x].signal_name[u]:y.
   IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
   For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 2. Multiple Alternate Functions[1] *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P4.2	tcpwm[0].line[6]:5	tcpwm[1].line[23]:1				scb[7].uart_rts:1		scb[7].spi_clk:1									
P4.3	tcpwm[0].line_compl[6]:5	tcpwm[1].line_compl[23]:1				scb[7].uart_cts:1		scb[7].spi_select0:1							bless.mxd_dpslp_mxd_clk_out		
P5.0	tcpwm[0].line[4]:0	tcpwm[1].line[4]:0				scb[5].uart_rx:0	scb[5].i2c_scl:0	scb[5].spi_mosi:0		audioss.clk_i2s_if	peri.tr_io_input[10]:0						
P5.1	tcpwm[0].line_compl[4]:0	tcpwm[1].line_compl[4]:0				scb[5].uart_tx:0	scb[5].i2c_sda:0	scb[5].spi_miso:0		audioss.tx_sck	peri.tr_io_input[11]:0						
P5.2	tcpwm[0].line[5]:0	tcpwm[1].line[5]:0				scb[5].uart_rts:0		scb[5].spi_clk:0		audioss.tx_ws							
P5.3	tcpwm[0].line_compl[5]:0	tcpwm[1].line_compl[5]:0				scb[5].uart_cts:0		scb[5].spi_select0:0		audioss.tx_sdo							
P5.4	tcpwm[0].line[6]:0	tcpwm[1].line[6]:0						scb[5].spi_select1:0		audioss.rx_sck							
P5.5	tcpwm[0].line_compl[6]:0	tcpwm[1].line_compl[6]:0						scb[5].spi_select2:0		audioss.rx_ws							
P5.6	tcpwm[0].line[7]:0	tcpwm[1].line[7]:0						scb[5].spi_select3:0		audioss.rx_sdi							
P5.7	tcpwm[0].line_compl[7]:0	tcpwm[1].line_compl[7]:0						scb[3].spi_select3:0									
P6.0	tcpwm[0].line[0]:1	tcpwm[1].line[8]:0	scb[8].i2c_scl:0			scb[3].uart_rx:0	scb[3].i2c_scl:0	scb[3].spi_mosi:0				cpuss.fault_out[0]					scb[8].spi_mosi:0
P6.1	tcpwm[0].line_compl[0]:1	tcpwm[1].line_compl[8]:0	scb[8].i2c_sda:0			scb[3].uart_tx:0	scb[3].i2c_sda:0	scb[3].spi_miso:0				cpuss.fault_out[1]					scb[8].spi_miso:0
P6.2	tcpwm[0].line[1]:1	tcpwm[1].line[9]:0				scb[3].uart_rts:0		scb[3].spi_clk:0									scb[8].spi_clk:0
P6.3	tcpwm[0].line_compl[1]:1	tcpwm[1].line_compl[9]:0				scb[3].uart_cts:0		scb[3].spi_select0:0									scb[8].spi_select0:0
P6.4	tcpwm[0].line[2]:1	tcpwm[1].line[10]:0	scb[8].i2c_scl:1			scb[6].uart_rx:2	scb[6].i2c_scl:2	scb[6].spi_mosi:2			peri.tr_io_input[12]:0	peri.tr_io_output[0]:1				cpuss.swj_swo_tdo	scb[8].spi_mosi:1
P6.5	tcpwm[0].line_compl[2]:1	tcpwm[1].line_compl[10]:0	scb[8].i2c_sda:1			scb[6].uart_tx:2	scb[6].i2c_sda:2	scb[6].spi_miso:2			peri.tr_io_input[13]:0	peri.tr_io_output[1]:1				cpuss.swj_swdoe_tdi	scb[8].spi_miso:1

Note

1. The notation for a signal is of the form IPName[x].signal_name[u]:y.
   IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
   For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 2. Multiple Alternate Functions[1] *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P6.6	tcpwm[0].line[3]:1	tcpwm[1].line[11]:0				scb[6].uart_rts:2		scb[6].spi_clk:2								cpuss.swj_swdio_tms	scb[8].spi_clk:1
P6.7	tcpwm[0].line_compl[3]:1	tcpwm[1].line_compl[11]:0				scb[6].uart_cts:2		scb[6].spi_select0:2								cpuss.swj_swclk_tclk	scb[8].spi_select0:1
P7.0	tcpwm[0].line[4]:1	tcpwm[1].line[12]:0				scb[4].uart_rx:1	scb[4].i2c_scl:1	scb[4].spi_mosi:1			peri.tr_io_input[14]:0		cpuss.trace_clock				
P7.1	tcpwm[0].line_compl[4]:1	tcpwm[1].line_compl[12]:0				scb[4].uart_tx:1	scb[4].i2c_sda:1	scb[4].spi_miso:1			peri.tr_io_input[15]:0						
P7.2	tcpwm[0].line[5]:1	tcpwm[1].line[13]:0				scb[4].uart_rts:1		scb[4].spi_clk:1									
P7.3	tcpwm[0].line_compl[5]:1	tcpwm[1].line_compl[13]:0				scb[4].uart_cts:1		scb[4].spi_select0:1									
P7.4	tcpwm[0].line[6]:1	tcpwm[1].line[14]:0						scb[4].spi_select1:1					bless.ext_lna_rx_ctl_out	cpuss.trace_data[3]:2			
P7.5	tcpwm[0].line_compl[6]:1	tcpwm[1].line_compl[14]:0						scb[4].spi_select2:1					bless.ext_pa_tx_ctl_out	cpuss.trace_data[2]:2			
P7.6	tcpwm[0].line[7]:1	tcpwm[1].line[15]:0						scb[4].spi_select3:1					bless.ext_pa_lna_chip_en_out	cpuss.trace_data[1]:2			
P7.7	tcpwm[0].line_compl[7]:1	tcpwm[1].line_compl[15]:0						scb[3].spi_select1:0	cpuss.clk_fm_pump					cpuss.trace_data[0]:2			
P8.0	tcpwm[0].line[0]:2	tcpwm[1].line[16]:0				scb[4].uart_rx:0	scb[4].i2c_scl:0	scb[4].spi_mosi:0			peri.tr_io_input[16]:0						
P8.1	tcpwm[0].line_compl[0]:2	tcpwm[1].line_compl[16]:0				scb[4].uart_tx:0	scb[4].i2c_sda:0	scb[4].spi_miso:0			peri.tr_io_input[17]:0						
P8.2	tcpwm[0].line[1]:2	tcpwm[1].line[17]:0				scb[4].uart_rts:0		scb[4].spi_clk:0									
P8.3	tcpwm[0].line_compl[1]:2	tcpwm[1].line_compl[17]:0				scb[4].uart_cts:0		scb[4].spi_select0:0									
P8.4	tcpwm[0].line[2]:2	tcpwm[1].line[18]:0						scb[4].spi_select1:0									

Note
1. The notation for a signal is of the form IPName[x].signal_name[u]:y.
   IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
   For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 2. Multiple Alternate Functions[1] *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P8.5	tcpwm[0].line_compl[2]:2	tcpwm[1].line_compl[18]:0						scb[4].spi_select2:0									
P8.6	tcpwm[0].line[3]:2	tcpwm[1].line[19]:0						scb[4].spi_select3:0									
P8.7	tcpwm[0].line_compl[3]:2	tcpwm[1].line_compl[19]:0						scb[3].spi_select2:0									
P9.0	tcpwm[0].line[4]:2	tcpwm[1].line[20]:0				scb[2].uart_rx:0	scb[2].i2c_scl:0	scb[2].spi_mosi:0			peri.tr_io_input[18]:0			cpuss.trace_data[3]:0			
P9.1	tcpwm[0].line_compl[4]:2	tcpwm[1].line_compl[20]:0				scb[2].uart_tx:0	scb[2].i2c_sda:0	scb[2].spi_miso:0			peri.tr_io_input[19]:0			cpuss.trace_data[2]:0			
P9.2	tcpwm[0].line[5]:2	tcpwm[1].line[21]:0				scb[2].uart_rts:0		scb[2].spi_clk:0		pass.dsi_ctb_cmp0:1				cpuss.trace_data[1]:0			
P9.3	tcpwm[0].line_compl[5]:2	tcpwm[1].line_compl[21]:0				scb[2].uart_cts:0		scb[2].spi_select0:0		pass.dsi_ctb_cmp1:1				cpuss.trace_data[0]:0			
P9.4	tcpwm[0].line[7]:5	tcpwm[1].line[0]:2						scb[2].spi_select1:0									
P9.5	tcpwm[0].line_compl[7]:5	tcpwm[1].line_compl[0]:2						scb[2].spi_select2:0									
P9.6	tcpwm[0].line[0]:6	tcpwm[1].line[1]:2						scb[2].spi_select3:0									
P9.7	tcpwm[0].line_compl[0]:6	tcpwm[1].line_compl[1]:2															
P10.0	tcpwm[0].line[6]:2	tcpwm[1].line[22]:0				scb[1].uart_rx:1	scb[1].i2c_scl:1	scb[1].spi_mosi:1			peri.tr_io_input[20]:0			cpuss.trace_data[3]:1			
P10.1	tcpwm[0].line_compl[6]:2	tcpwm[1].line_compl[22]:0				scb[1].uart_tx:1	scb[1].i2c_sda:1	scb[1].spi_miso:1			peri.tr_io_input[21]:0			cpuss.trace_data[2]:1			
P10.2	tcpwm[0].line[7]:2	tcpwm[1].line[23]:0				scb[1].uart_rts:1		scb[1].spi_clk:1						cpuss.trace_data[1]:1			
P10.3	tcpwm[0].line_compl[7]:2	tcpwm[1].line_compl[23]:0				scb[1].uart_cts:1		scb[1].spi_select0:1						cpuss.trace_data[0]:1			
P10.4	tcpwm[0].line[0]:3	tcpwm[1].line[0]:1						scb[1].spi_select1:1	audioss.pdm_clk								

Note

1. The notation for a signal is of the form IPName[x].signal_name[u]:y.
   IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
   For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 2. Multiple Alternate Functions[1] *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P10.5	tcpwm[0].line_compl[0]:3	tcpwm[1].line_compl[0]:1						scb[1].spi_select2:1	audioss.pdm_data								
P10.6	tcpwm[0].line[1]:6	tcpwm[1].line[2]:2						scb[1].spi_select3:1									
P10.7	tcpwm[0].line_compl[1]:6	tcpwm[1].line_compl[2]:2															
P11.0	tcpwm[0].line[1]:3	tcpwm[1].line[1]:1			smif.spi_select2	scb[5].uart_rx:1	scb[5].i2c_scl:1	scb[5].spi_mosi:1			peri.tr_io_input[22]:0						
P11.1	tcpwm[0].line_compl[1]:3	tcpwm[1].line_compl[1]:1			smif.spi_select1	scb[5].uart_tx:1	scb[5].i2c_sda:1	scb[5].spi_miso:1			peri.tr_io_input[23]:0						
P11.2	tcpwm[0].line[2]:3	tcpwm[1].line[2]:1			smif.spi_select0	scb[5].uart_rts:1		scb[5].spi_clk:1									
P11.3	tcpwm[0].line_compl[2]:3	tcpwm[1].line_compl[2]:1			smif.spi_data3	scb[5].uart_cts:1		scb[5].spi_select0:1				peri.tr_io_output[0]:0					
P11.4	tcpwm[0].line[3]:3	tcpwm[1].line[3]:1			smif.spi_data2			scb[5].spi_select1:1				peri.tr_io_output[1]:0					
P11.5	tcpwm[0].line_compl[3]:3	tcpwm[1].line_compl[3]:1			smif.spi_data1			scb[5].spi_select2:1									
P11.6					smif.spi_data0			scb[5].spi_select3:1									
P11.7					smif.spi_clk												
P12.0	tcpwm[0].line[4]:3	tcpwm[1].line[4]:1			smif.spi_data4	scb[6].uart_rx:0	scb[6].i2c_scl:0	scb[6].spi_mosi:0			peri.tr_io_input[24]:0						
P12.1	tcpwm[0].line_compl[4]:3	tcpwm[1].line_compl[4]:1			smif.spi_data5	scb[6].uart_tx:0	scb[6].i2c_sda:0	scb[6].spi_miso:0			peri.tr_io_input[25]:0						
P12.2	tcpwm[0].line[5]:3	tcpwm[1].line[5]:1			smif.spi_data6	scb[6].uart_rts:0		scb[6].spi_clk:0									
P12.3	tcpwm[0].line_compl[5]:3	tcpwm[1].line_compl[5]:1			smif.spi_data7	scb[6].uart_cts:0		scb[6].spi_select0:0									
P12.4	tcpwm[0].line[6]:3	tcpwm[1].line[6]:1			smif.spi_select3			scb[6].spi_select1:0	audioss.pdm_clk								

Note

1. The notation for a signal is of the form IPName[x].signal_name[u]:y.
   IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
   For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Table 2. Multiple Alternate Functions[1] *(continued)*

Port/ Pin	ACT #0	ACT #1	DS #2	ACT #4	ACT #5	ACT #6	ACT #7	ACT #8	ACT #9	ACT #10	ACT #12	ACT #13	ACT #14	ACT #15	DS #4	DS #5	DS #6
P12.5	tcpwm[0].line_compl[6]:3	tcpwm[1].line_compl[6]:1						scb[6].spi_select2:0	audioss.pdm_data								
P12.6	tcpwm[0].line[7]:3	tcpwm[1].line[7]:1						scb[6].spi_select3:0									
P12.7	tcpwm[0].line_compl[7]:3	tcpwm[1].line_compl[7]:1															
P13.0	tcpwm[0].line[0]:4	tcpwm[1].line[8]:1				scb[6].uart_rx:1	scb[6].i2c_scl:1	scb[6].spi_mosi:1			peri.tr_io_input[26]:0						
P13.1	tcpwm[0].line_compl[0]:4	tcpwm[1].line_compl[8]:1				scb[6].uart_tx:1	scb[6].i2c_sda:1	scb[6].spi_miso:1			peri.tr_io_input[27]:0						
P13.2	tcpwm[0].line[1]:4	tcpwm[1].line[9]:1				scb[6].uart_rts:1		scb[6].spi_clk:1									
P13.3	tcpwm[0].line_compl[1]:4	tcpwm[1].line_compl[9]:1				scb[6].uart_cts:1		scb[6].spi_select0:1									
P13.4	tcpwm[0].line[2]:4	tcpwm[1].line[10]:1						scb[6].spi_select1:1									
P13.5	tcpwm[0].line_compl[2]:4	tcpwm[1].line_compl[10]:1						scb[6].spi_select2:1									
P13.6	tcpwm[0].line[3]:4	tcpwm[1].line[11]:1						scb[6].spi_select3:1									
P13.7	tcpwm[0].line_compl[3]:4	tcpwm[1].line_compl[11]:1															

Note

1. The notation for a signal is of the form IPName[x].signal_name[u]:y.
   IPName = Name of the block (such as tcpwm), x = Unique instance of the IP, Signal_name = Name of the signal, u = Signal number where there are more than one signals for a particular signal name, y = Designates copies of the signal name.
   For example, the name tcpwm[0].line_compl[3]:4 indicates that this is instance 0 of a tcpwm block, the signal is line_compl # 3 (complement of the line output) and this is the fourth occurrence (copy) of the signal. Signal copies are provided to allow flexibility in routing and to maximise utilisation of on-chip resources.

Analog, Smart I/O, and DSI alternate Port Pin functionality is provided in Table 3.

Table 3. Port Pin Analog, Smart I/O, and DSI Functions

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO	USB
P0.0	P0.0	wco_in		dsi[0].port_if[0]		
P0.1	P0.1	wco_out		dsi[0].port_if[1]		
P0.2	P0.2			dsi[0].port_if[2]		
P0.3	P0.3			dsi[0].port_if[3]		
P0.4	P0.4		pmic_wakeup_in hibernate_wakeup[1]	dsi[0].port_if[4]		
P0.5	P0.5		pmic_wakeup_out	dsi[0].port_if[5]		
P1.0	P1.0			dsi[1].port_if[0]		
P1.1	P1.1			dsi[1].port_if[1]		
P1.2	P1.2			dsi[1].port_if[2]		
P1.3	P1.3			dsi[1].port_if[3]		
P1.4	P1.4		hibernate_wakeup[0]	dsi[1].port_if[4]		
P1.5	P1.5			dsi[1].port_if[5]		
P14.0	USBDP					usb.usb_dp_pad
P14.1	USBDM					usb.usb_dm_pad
P2.0	P2.0			dsi[2].port_if[0]		
P2.1	P2.1			dsi[2].port_if[1]		
P2.2	P2.2			dsi[2].port_if[2]		
P2.3	P2.3			dsi[2].port_if[3]		
P2.4	P2.4			dsi[2].port_if[4]		
P2.5	P2.5			dsi[2].port_if[5]		
P2.6	P2.6			dsi[2].port_if[6]		
P2.7	P2.7			dsi[2].port_if[7]		
P3.0	P3.0					
P3.1	P3.1					
P3.2	P3.2					
P3.3	P3.3					
P3.4	P3.4					
P3.5	P3.5					
P4.0	P4.0			dsi[0].port_if[6]		
P4.1	P4.1			dsi[0].port_if[7]		
P4.2	P4.2			dsi[1].port_if[6]		
P4.3	P4.3			dsi[1].port_if[7]		
P5.0	P5.0			dsi[3].port_if[0]		
P5.1	P5.1			dsi[3].port_if[1]		
P5.2	P5.2			dsi[3].port_if[2]		
P5.3	P5.3			dsi[3].port_if[3]		
P5.4	P5.4			dsi[3].port_if[4]		
P5.5	P5.5			dsi[3].port_if[5]		
P5.6	P5.6	lpcomp.inp_comp0		dsi[3].port_if[6]		
P5.7	P5.7	lpcomp.inn_comp0		dsi[3].port_if[7]		
P6.0	P6.0			dsi[4].port_if[0]		

Table 3. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO	USB
P6.1	P6.1			dsi[4].port_if[1]		
P6.2	P6.2	lpcomp.inp_comp1		dsi[4].port_if[2]		
P6.3	P6.3	lpcomp.inn_comp1		dsi[4].port_if[3]		
P6.4	P6.4			dsi[4].port_if[4]		
P6.5	P6.5			dsi[4].port_if[5]		
P6.6	P6.6		swd_data	dsi[4].port_if[6]		
P6.7	P6.7		swd_clk	dsi[4].port_if[7]		
P7.0	P7.0			dsi[5].port_if[0]		
P7.1	P7.1	csd.cmodpadd csd.cmodpads		dsi[5].port_if[1]		
P7.2	P7.2	csd.csh_tankpadd csd.csh_tankpads		dsi[5].port_if[2]		
P7.3	P7.3	csd.vref_ext		dsi[5].port_if[3]		
P7.4	P7.4			dsi[5].port_if[4]		
P7.5	P7.5			dsi[5].port_if[5]		
P7.6	P7.6			dsi[5].port_if[6]		
P7.7	P7.7	csd.cshieldpads		dsi[5].port_if[7]		
P8.0	P8.0			dsi[11].port_if[0]	smartio[8].io[0]	
P8.1	P8.1			dsi[11].port_if[1]	smartio[8].io[1]	
P8.2	P8.2			dsi[11].port_if[2]	smartio[8].io[2]	
P8.3	P8.3			dsi[11].port_if[3]	smartio[8].io[3]	
P8.4	P8.4			dsi[11].port_if[4]	smartio[8].io[4]	
P8.5	P8.5			dsi[11].port_if[5]	smartio[8].io[5]	
P8.6	P8.6			dsi[11].port_if[6]	smartio[8].io[6]	
P8.7	P8.7			dsi[11].port_if[7]	smartio[8].io[7]	
P9.0	P9.0	ctb_oa0+		dsi[10].port_if[0]	smartio[9].io[0]	
P9.1	P9.1	ctb_oa0-		dsi[10].port_if[1]	smartio[9].io[1]	
P9.2	P9.2	ctb_oa0_out		dsi[10].port_if[2]	smartio[9].io[2]	
P9.3	P9.3	ctb_oa1_out		dsi[10].port_if[3]	smartio[9].io[3]	
P9.4	P9.4	ctb_oa1-		dsi[10].port_if[4]	smartio[9].io[4]	
P9.5	P9.5	ctb_oa1+		dsi[10].port_if[5]	smartio[9].io[5]	
P9.6	P9.6	ctb_oa0+		dsi[10].port_if[6]	smartio[9].io[6]	
P9.7	P9.7	ctb_oa1+ or ext_vref		dsi[10].port_if[7]	smartio[9].io[7]	
P10.0	P10.0	sarmux[0]		dsi[9].port_if[0]		
P10.1	P10.1	sarmux[1]		dsi[9].port_if[1]		
P10.2	P10.2	sarmux[2]		dsi[9].port_if[2]		
P10.3	P10.3	sarmux[3]		dsi[9].port_if[3]		
P10.4	P10.4	sarmux[4]		dsi[9].port_if[4]		
P10.5	P10.5	sarmux[5]		dsi[9].port_if[5]		
P10.6	P10.6	sarmux[6]		dsi[9].port_if[6]		
P10.7	P10.7	sarmux[7]		dsi[9].port_if[7]		

Table 3. Port Pin Analog, Smart I/O, and DSI Functions *(continued)*

Port/Pin	Name	Analog	Digital HV	DSI	SMARTIO	USB
P11.0	P11.0			dsi[8].port_if[0]		
P11.1	P11.1			dsi[8].port_if[1]		
P11.2	P11.2			dsi[8].port_if[2]		
P11.3	P11.3			dsi[8].port_if[3]		
P11.4	P11.4			dsi[8].port_if[4]		
P11.5	P11.5			dsi[8].port_if[5]		
P11.6	P11.6			dsi[8].port_if[6]		
P11.7	P11.7			dsi[8].port_if[7]		
P12.0	P12.0			dsi[7].port_if[0]		
P12.1	P12.1			dsi[7].port_if[1]		
P12.2	P12.2			dsi[7].port_if[2]		
P12.3	P12.3			dsi[7].port_if[3]		
P12.4	P12.4			dsi[7].port_if[4]		
P12.5	P12.5			dsi[7].port_if[5]		
P12.6	P12.6	eco_in		dsi[7].port_if[6]		
P12.7	P12.7	eco_out		dsi[7].port_if[7]		
P13.0	P13.0			dsi[6].port_if[0]		
P13.1	P13.1			dsi[6].port_if[1]		
P13.2	P13.2			dsi[6].port_if[2]		
P13.3	P13.3			dsi[6].port_if[3]		
P13.4	P13.4			dsi[6].port_if[4]		
P13.5	P13.5			dsi[6].port_if[5]		
P13.6	P13.6			dsi[6].port_if[6]		
P13.7	P13.7			dsi[6].port_if[7]		

Power

The power system diagram (see Figure 3) shows the general requirements for power pins on the PSoC 61. The PSoC 61 power scheme allows different VDDIO and VDDA connections. Since no sequencing requirements need to be analyzed and specified, customers may bring up the power supplies in any order and the power system is responsible for ensuring power is good in all domains before allowing operation. VDDD, VDDA, and VDDIO may be separate nets, which are not ohmically connected on chip. Depending on different package requirements, these may be required to be connected off chip.

The power system will have a buck regulator in addition to an LDO. A Single Input Multiple Output (SIMO) Buck regulator with multiple outputs allows saving an inductor.

The preliminary diagram is shown in Figure 3.

Figure 3. SOC Power Connections

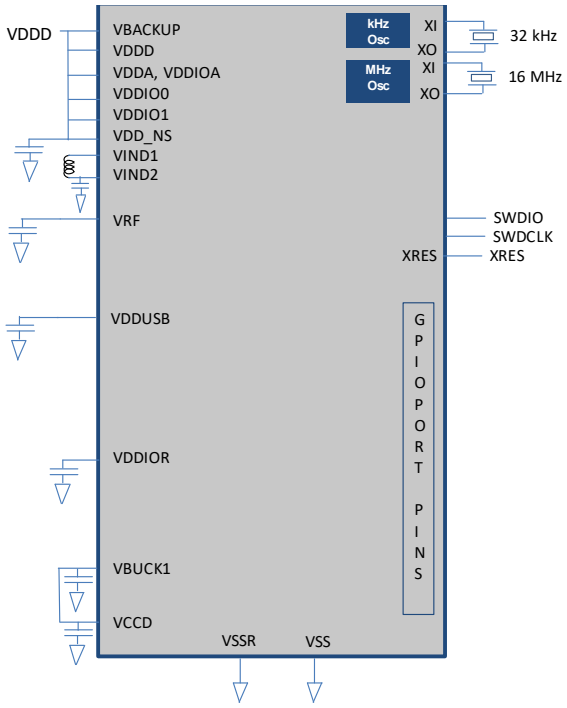


Figure 3 shows the power supply pins to the PSoC 61. It also shows which pins need bypass capacitors.

Description of power pins is as follows:

1. VBACKUP is the supply to the backup domain. The backup domain includes the 32 kHz WCO, RTC, and backup registers. It can generate a wake-up interrupt to the chip via the RTC timers or an external input. It can also generate an output to wakeup external circuitry. It is connected to VDDD when not used as a separate battery backup domain. VBACKUP provides the supply for Port 0.
2. VDDD is the main digital supply input (1.7 to 3.6 V). It provides the inputs for the internal Regulators and for Port 1.
3. VDDA is the supply for analog peripherals (1.7 to 3.6 V). It must be connected to VDDIOA on the PCB.
4. VDDIOA is the supply to for Ports 9 and 10. It must be connected to VDDA on the PCB when present. Ports 9 and 10 are supplied by VDDA when VDDIOA is not present.
5. VDD_NS is the supply input to the Buck and should be at the same potential as VDDD. The bypass capacitor between VDD_NS and ground should be 10 µF.
6. VDDIO0 is the Supply for Ports 11 to 13 when present. When not present, these ports are supplied by VDDD.
7. VDDIO1 is the Supply for Ports 5 to 8 when present. When not present, these ports are supplied by VDDA.
8. VDDIOR is the Supply for Ports 2 to 4 on the BGA 124 only.

All the pins above may be shorted to VDDD as shown in Figure 3.

9. VRF is the second output of the SIMO buck.
10. VBUCK1 is the SIMO buck output to the internal core logic and is to be connected to VCCD.
11. VCCD is the internal core logic and needs to be connected to VBUCK1 and decoupled.

The supply voltage range is 1.71 to 3.6 V with all functions and circuits operating over that range. All grounds must be shorted together on the PCB. Bypass capacitors must be used from VDDD and VDDA to ground and wherever indicated in the diagram. Typical practice for systems in this frequency range is to use a capacitor in the 10 µF range in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing. Recommended Buck output capacitor values are 10 µF for Vrf and 4.7 µF for VBUCK1. The capacitor connected to Vind2 should be 100 nF. All capacitors should be ±20% or better; the recommended inductor value is 2.2 µH ±20% (for example, TDK MLP2012H2R2MT0S1).

Development Support

The PSoC 61 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit http://www.cypress.com/products/32-bit-arm-cortex-m4-psoc-6 to find out more.

Documentation

A suite of documentation supports the PSoC 61 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software User Guide: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

Component Datasheets: The flexibility of PSoC allows the creation of new peripherals (Components) long after the device has gone into production. Component datasheets provide all of the information needed to select and use a particular Component, including a functional description, API documentation, example code, and AC/DC specifications.

Technical Reference Manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at http://www.cypress.com/products/32-bit-arm-cortex-m4-psoc-6.

Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 61 family is part of a development tool ecosystem. Visit us at www.cypress.com/products/psoc-creator-integrated-design-environment-ide for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

Electrical Specifications

Note: These are preliminary and subject to change.

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings[2]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID1	V_{DD_ABS}	Analog or digital supply relative to V_{SS} (V_{SSD} = V_{SSA})	–0.5	–	4	V	Absolute Maximum
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to Vssd	–0.5	–	1.2	V	Absolute Maximum
SID3	V_{GPIO_ABS}	GPIO voltage; V_{DDD} or V_{DDA}	–0.5	–	V_{DD} + 0.5	V	Absolute Maximum
SID4	I_{GPIO_ABS}	Current per GPIO	–25	–	25	mA	Absolute Maximum
SID5	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5	–	0.5	mA	Absolute Maximum
SID3A	ESD_HBM	Electrostatic discharge Human Body Model	2200	–	–	V	Absolute Maximum
SID3B	ESD_HBM_ ANT	Electrostatic discharge Human Body Model; Antenna Pin	500	–	–	V	Absolute Maximum; RF pin
SID4A	ESD_CDM	Electrostatic discharge Charged Device Model	500	–	–	V	Absolute Maximum
SID4B	ESD_CDM_ ANT	Electrostatic discharge Charged Device Model; Antenna Pin	200	–	–	V	Absolute Maximum; RF pin
SID5A	LU	Pin current for latchup-free operation	–100	–	100	mA	Absolute Maximum

Note: All specifications are valid for –40 °C ≤ TA ≤ 85 °C and for 1.71 V to 3.6 V except where noted.

Device-Level Specifications

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC Specifications							
SID6	V_{DDD}	Internal regulator and Port 1 GPIO supply.	1.7	–	3.6	V	–
SID7	V_{DDA}	Analog power supply voltage. Shorted to V_{DDIOA} on PCB.	1.7	–	3.6	V	Internally unregulated supply
SID7A	V_{DDIO1}	GPIO supply for Ports 5 to 8 when present	1.7	–	3.6	V	V_{DDIO_1} must be ≥ to V_{DDA}.
SID7B	V_{DDIO0}	GPIO supply for Ports 11 to 13 when present	1.7	–	3.6	V	–
SID7E	V_{DDIO0}	Supply for E-Fuse programming	2.38	2.5	2.62	V	E-Fuse programming voltage
SID7C	V_{DDIO2}	GPIO supply for Ports 2 to 4 on BGA 124 only	1.7	–	3.6	V	–
SID7D	V_{DDIOA}	GPIO supply for Ports 9 to 10. Shorted to V_{DDA} on PCB.	1.7	–	3.6	V	–
SID7F	V_{DDUSB}	Supply for Port 14 (USB or GPIO) when present	1.7	–	3.6	V	Min. supply is 2.85 V for USB

Note
2. Usage above the absolute maximum conditions listed in Table 4 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID6B	V_{BACKUP}	Backup Power and GPIO Port 0 supply when present	1.7	–	3.6	V	Min. is 1.4 V in Backup Mode
SID8	V_{CCD1}	Output voltage (for core logic bypass)	–	1.1	–	V	High-speed Mode
SID9	V_{CCD2}	Output voltage (for core logic bypass)	–	0.9	–	V	ULP Mode. Valid for -20 to 85 °C.
SID10	C_{EFC}	External regulator voltage (V_{CCD}) bypass	3.8	4.7	5.6	µF	X5R ceramic or better; Value for 0.8 to 1.2 V
SID11	C_{EXC}	Power supply decoupling capacitor	–	10	–	µF	X5R ceramic or better
LP RANGE POWER SPECIFICATIONS (for V_{CCD} = 1.1 V with Buck and LDO)							
Cortex M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF1	I_{DD1}	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	–	2.3	3.2	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	3.1	3.6	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	5.7	6.5	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDF2	I_{DD2}	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1).	–	0.9	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.2	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.8	3.5	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
Execute with Cache Enabled							
SIDC1	I_{DD3}	Execute from Cache; CM4 Active 150 MHz, CM0+ Sleep 75 MHz. IMO & FLL. Dhrystone.	–	6.3	7	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	9.7	11.2	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	14.4	15.1	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDC2	I_{DD4}	Execute from Cache; CM4 Active 100 MHz, CM0+ Sleep 100 MHz. IMO & FLL. Dhrystone.	–	4.8	5.8	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	7.4	8.4	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	11.3	12	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDC3	I_{DD5}	Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. IMO & FLL. Dhrystone.	–	2.4	3.4	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	3.7	4.1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	6.3	7.2	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDC4	I_{DD6}	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. IMO. Dhrystone.	–	0.9	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.3	1.8	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	3	3.8	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Cortex M0+. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF3	I_{DD7}	Execute from Flash; CM4 Off, CM0+ Active 50 MHz. With IMO & FLL. While (1).	–	2.4	3.3	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	3.2	3.7	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	5.6	6.3	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDF4	I_{DD8}	Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1).	–	0.8	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.1	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.60	3.4	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
Execute with Cache Enabled							
SIDC5	I_{DD9}	Execute from Cache; CM4 Off, CM0+ Active 100 MHz. With IMO & FLL. Dhrystone.	–	3.8	4.5	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	5.9	6.5	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	9	9.7	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDC6	I_{DD10}	Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.8	1.3	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.20	1.7	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.60	3.4	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
Cortex M4. Sleep Mode							
SIDS1	I_{DD11}	CM4 Sleep 100 MHz, CM0+ Sleep 25 MHz. With IMO & FLL.	–	1.5	2.2	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	2.2	2.7	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	4	4.6	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDS2	I_{DD12}	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL	–	1.2	1.9	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.7	2.2	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	3.4	4.3	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDS3	I_{DD13}	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	0.7	1.3	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1	1.5	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.4	3.3	mA	V_{DDD} = 1.8 to 3.3 V, LDO, Max. at 85 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Cortex M0+. Sleep Mode							
SIDS4	IDD14	CM4 Off, CM0+ Sleep 50 MHz. With IMO & FLL.	–	1.3	2	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.9	2.4	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	3.80	4.6	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDS5	IDD15	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.7	1.3	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1	1.5	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.4	3.3	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85°C
Cortex M4. Minimum Regulator Current Mode							
SIDLPA1	IDD16	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1).	–	0.9	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.2	1.7	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.8	3.5	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDLPA2	IDD17	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.9	1.5	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.3	1.8	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.9	3.7	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85 °C
Cortex M0+. Minimum Regulator Current Mode							
SIDLPA3	IDD18	Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While (1)	–	0.8	1.4	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.1	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.7	3.6	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85 °C
SIDLPA4	IDD19	Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.8	1.4	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.2	1.7	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.7	3.6	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85 °C
Cortex M4. Minimum Regulator Current Mode							
SIDLPS1	IDD20	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO.	–	0.7	1.1	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1	1.5	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.4	3.3	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Cortex M0+. Minimum Regulator Current Mode							
SIDLPS3	IDD22	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.6	1.1	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.9	1.5	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
			–	2.4	3.3	mA	VDDD = 1.8 to 3.3 V, LDO, Max. at 85 °C
ULP RANGE POWER SPECIFICATIONS (for V_{CCD} = 0.9 V using the Buck). ULP Mode is valid from –20 to +85 °C.							
Cortex M4. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF5	IDD3	Execute from Flash; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. While(1).	–	1.7	2.2	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	2.1	2.4	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDF6	IDD4	Execute from Flash; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While (1)	–	0.56	0.8	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.75	1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Execute with Cache Enabled							
SIDC8	IDD10	Execute from Cache; CM4 Active 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL. Dhrystone.	–	1.6	2.2	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	2.4	2.7	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDC9	IDD11	Execute from Cache; CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.65	0.8	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.8	1.1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Cortex M0+. Active Mode							
Execute with Cache Disabled (Flash)							
SIDF7	IDD16	Execute from Flash; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Write(1).	–	1	1.4	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.34	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDF8	IDD17	Execute from Flash; CM4 Off, CM0+ Active 8 MHz. With IMO. While(1)	–	0.54	0.75	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.73	1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Execute with Cache Enabled							
SIDC10	IDD18	Execute from Cache; CM4 Off, CM0+ Active 25 MHz. With IMO & FLL. Dhrystone.	–	0.91	1.25	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.34	1.6	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDC11	IDD19	Execute from Cache; CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.51	0.72	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.73	0.95	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Cortex M4. Sleep Mode							
SIDS7	IDD21	CM4 Sleep 50 MHz, CM0+ Sleep 25 MHz. With IMO & FLL	–	0.76	1.1	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	1.1	1.4	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDS8	IDD22	CM4 Sleep 8 MHz, CM0+ Sleep 8 MHz. With IMO	–	0.42	0.65	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.59	0.8	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Cortex M0+. Sleep Mode							
SIDS9	IDD23	CM4 Off, CM0+ Sleep 25 MHz. With IMO & FLL.	–	0.62	0.9	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.88	1.1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDS10	IDD24	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.41	0.6	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.58	0.8	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Cortex M4. Minimum Regulator Current Mode							
SIDLPA5	IDD25	Execute from Flash. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. While(1).	–	0.52	0.75	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.76	1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDLPA6	IDD26	Execute from Cache. CM4 Active 8 MHz, CM0+ Sleep 8 MHz. With IMO. Dhrystone.	–	0.54	0.76	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.78	1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Cortex M0+. Minimum Regulator Current Mode							
SIDLPA7	IDD27	Execute from Flash. CM4 Off, CM0+ Active 8 MHz. With IMO. While (1).	–	0.51	0.75	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.75	1	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
SIDLPA8	IDD28	Execute from Cache. CM4 Off, CM0+ Active 8 MHz. With IMO. Dhrystone.	–	0.48	0.7	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.7	0.95	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Cortex M4. Minimum Regulator Current Mode							
SIDLPS5	IDD29	CM4 Sleep 8 MHz, CM0 Sleep 8 MHz. With IMO.	–	0.4	0.6	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.57	0.8	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Cortex M0+. Minimum Regulator Current Mode							
SIDLPS7	IDD31	CM4 Off, CM0+ Sleep 8 MHz. With IMO.	–	0.39	0.6	mA	V_{DDD} = 3.3 V, Buck ON, Max. at 60 °C
			–	0.56	0.8	mA	V_{DDD} = 1.8 V, Buck ON, Max. at 60 °C
Deep Sleep Mode							
SIDDS1	IDD33A	With internal Buck enabled and 64K SRAM retention	–	7	–	µA	Max. value is at 85 °C

Table 5. Power Supply Range, CPU Current, and Transition Time Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SIDDS1_B	IDD33A_B	With internal Buck enabled and 64K SRAM retention	–	7	–	µA	Max. value is at 60 °C
SIDDS2	IDD33B	With internal Buck enabled and 256K SRAM retention	–	9	–	µA	Max. value is at 85 °C
SIDDS2_B	IDD33B_B	With internal Buck enabled and 256K SRAM retention	–	9	–	µA	Max. value is at 60 °C
Hibernate Mode							
SIDHIB1	IDD34	VDDD = 1.8V	–	300	–	nA	No clocks running
SIDHIB2	IDD34A	VDDD = 3.3V	–	800	–	nA	No clocks running
Power Mode Transition Times							
SID12	TLPACT_ACT	Low Power Active to Active transition time	–	–	35	µs	Including PLL lock time
SID13	TDS_LPACT	Deep Sleep to LP Active transition time. Guaranteed by Design.	–	–	25	µs	Cypress supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With an 8 MHz CPU clock (LP Active), the time before user code executes is 25 + 12.5 = 37.5 µs.
SID13A	TDS_ACT	Deep Sleep to Active transition time. Guaranteed by Design.	–	–	25	µs	Cypress supplied software wakeup routines take approximately 100 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With a 25 MHz CPU clock (FLL), the time before user code executes is 25 + 4 = 29 µs. With a 100 MHz CPU clock, the time is 25 + 1.0 = 26 µs.
SID14	THIB_ACT	Hibernate to Active transition time	–	500	–	µs	Including PLL lock time

XRES

Table 6. XRES

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
XRES (Active Low) Specifications							
XRES AC Specifications							
SID15	T_{XRES_ACT}	POR or XRES release to Active transition time	–	750	–	µs	Normal Mode, 50 MHz M0+
SID16	T_{XRES_PW}	XRES Pulse width	5	–	–	µs	–
XRES DC Specifications							
SID17	T_{XRES_IDD}	IDD when XRES asserted	–	300	–	nA	V_{DDD} = 1.8 V
SID17A	$T_{XRES\_IDD\_1}$	IDD when XRES asserted	–	800	–	nA	V_{DDD} = 3.3 V
SID77	V_{IH}	Input Voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID78	V_{IL}	Input Voltage low threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID80	C_{IN}	Input Capacitance	–	3	–	pF	–
SID81	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	–
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

GPIO

Table 7. GPIO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
GPIO DC Specifications							
SID57	V_{IH}	Input voltage high threshold	0.7 * V_{DD}	–	–	V	CMOS Input
SID57A	I_{IHS}	Input current when Pad > VDDIO for OVT inputs	–	–	10	µA	Per I^2C Spec
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 * V_{DD}	V	CMOS Input
SID241	V_{IH}	LVTTL input, V_{DD} < 2.7 V	0.7 * V_{DD}	–	–	V	–
SID242	V_{IL}	LVTTL input, V_{DD} < 2.7 V	–	–	0.3 * V_{DD}	V	–
SID243	V_{IH}	LVTTL input, V_{DD} ≥ 2.7 V	2.0	–	–	V	–
SID244	V_{IL}	LVTTL input, V_{DD} ≥ 2.7 V	–	–	0.8	V	–
SID59	V_{OH}	Output voltage high level	V_{DD}-0.5	–	–	V	I_{OH} = 8 mA
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 8 mA
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DD} = 3.0 V
SID65A	I_{IL_CTBM}	Input leakage on CTBm input pins	–	–	4	nA	–
SID66	C_{IN}	Input Capacitance	–	–	5	pF	–

Notes
3. Cypress-supplied software wakeup routines take approximately 180 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With an 8-MHz CPU clock (LP Active), the time before user code executes is 25 + 22.5 = 47.5 µs.
4. Cypress-supplied software wakeup routines take approximately 180 CPU clock cycles after hardware wakeup (the 25 µs) before transition to Application code. With a 25-MHz CPU clock (FLL), the time before user code executes is 25 + 7.2 = 32.2 µs. With a 100-MHz CPU clock, the time is 25 + 1.8 = 26.8 µs.

Table 7. GPIO Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID67	V_{HYSTTL}	Input hysteresis LVTTL $V_{DD} > 2.7$ V	100	0	–	mV	–
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 * V_{DD}	–	–	mV	–
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	–
GPIO AC Specifications							
SID70	T_{RISEF}	Rise time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8mA drive strength
SID71	T_{FALLF}	Fall time in Fast Strong Mode. 10% to 90% of V_{DD}.	–	–	2.5	ns	Cload = 15 pF, 8 mA drive strength
SID72	T_{RISES_1}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	52	–	142	ns	Cload = 15 pF, 8 mA drive strength, $V_{DD} \leq 2.7$ V
SID72A	T_{RISES_2}	Rise time in Slow Strong Mode. 10% to 90% of V_{DD}.	48	–	102	ns	Cload = 15 pF, 8 mA drive strength, $2.7 \text{ V} < V_{DD} \leq 3.6$ V
SID73	T_{FALLS_1}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}	44	–	211	ns	Cload = 15 pF, 8 mA drive strength, $V_{DD} \leq$ 2.7 V
SID73A	T_{FALLS_2}	Fall time in Slow Strong Mode. 10% to 90% of V_{DD}.	42	–	93	ns	Cload = 15 pF, 8 mA drive strength, $2.7 \text{ V} < V_{DD} \leq 3.6$ V
SID73G	T_{FALL_I2C}	Fall time (30% to 70% of V_{DD}) in Slow Strong Mode	20 * V_{DDIO} / 5.5	–	250	ns	Cload = 10 pF to 400 pF, 8-mA drive strength
SID74	$F_{GPIOUT1}$	GPIO Fout. Fast Strong Mode.	–	–	100	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO Fout; Slow Strong Mode.	–	–	16.7	MHz	90/10%, 15-pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO Fout; Fast Strong Mode.	–	–	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO Fout; Slow Strong Mode.	–	–	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; $1.71 \text{ V} \leq V_{DD} \leq 3.6$ V	–	–	100	MHz	90/10% V_{IO}

Analog Peripherals

Opamp

Table 8. Opamp Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
	I_{DD}	Opamp Block current. No load.	–	–	–		–
SID269	I_{DD_HI}	Power = Hi	–	1300	1500	µA	–
SID270	I_{DD_MED}	Power = Med	–	450	600	µA	–
SID271	I_{DD_LOW}	Power = Lo	–	250	350	µA	–
	GBW	Load = 20 pF, 0.1 mA. VDDA = 2.7 V	–	–	–		–
SID272	GBW_HI	Power = Hi	6	–	–	MHz	–
SID273	GBW_MED	Power = Med	4	–	–	MHz	–
SID274	GBW_LO	Power = Lo	–	1	–	MHz	–
	I_{OUT_MAX}	VDDA ≥ 2.7 V, 500 mV from rail	–	–	–		–
SID275	$I_{OUT\_MAX\_HI}$	Power = Hi	10	–	–	mA	–
SID276	$I_{OUT\_MAX\_MID}$	Power = Mid	10	–	–	mA	–
SID277	$I_{OUT\_MAX\_LO}$	Power = Lo	–	5	–	mA	–
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail	–	–	–		–
SID278	$I_{OUT\_MAX\_HI}$	Power = Hi	4	–	–	mA	–
SID279	$I_{OUT\_MAX\_MID}$	Power = Mid	4	–	–	mA	–
SID280	$I_{OUT\_MAX\_LO}$	Power = Lo	–	2	–	mA	–
SID281	V_{IN}	Input voltage range	0	–	V_{DDA} – 0.2	V	–
SID282	V_{CM}	Input common mode voltage	0	–	V_{DDA} – 0.2	V	–
	V_{OUT}	VDDA ≥ 2.7V	–	–	–		–
SID283	V_{OUT_1}	Power = hi, Iload = 10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID284	V_{OUT_2}	Power = hi, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID285	V_{OUT_3}	Power = med, Iload = 1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID286	V_{OUT_4}	Power = lo, Iload = 0.1 mA	0.2	–	V_{DDA} – 0.2	V	–
SID287	V_{OS_UNTR}	Offset voltage, untrimmed	–	–	–	mV	–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1	±0.5	1	mV	High Mode, 0.2 to V_{DDA} - 0.2
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	±1	–	mV	Medium Mode
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	±2	–	mV	Low Mode
SID289	$V_{OS\_DR\_UNTR}$	Offset voltage drift, untrimmed	–	–	–	µV/°C	–
SID290	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–10	±3	10	µV/°C	High Mode, 0.2 to V_{DDA}-0.2
SID290A	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Medium Mode
SID290B	$V_{OS\_DR\_TR}$	Offset voltage drift, trimmed	–	±10	–	µV/°C	Low Mode
SID291	CMRR	DC Common mode rejection ratio	67	80	–	dB	V_{DDD} = 3.3 V
SID292	PSRR	Power supply rejection ratio at 1 kHz, 10-mV ripple	70	85	–	dB	V_{DDD} = 3.3 V
Noise			–	–	–		–

Table 8. Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID293	VN1	Input-referred, 1 Hz–1 GHz, power = Hi	–	100	–	µVrms	–
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	180	–	nV/rtHz	–
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	70	–	nV/rtHz	–
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	38	–	nV/rtHz	–
SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Output slew rate	6	–	–	V/µs	Cload = 50 pF, Power = High, $V_{DDA} \geq 2.7$ V
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	25	–	µs	–
	COMP_MODE	Comparator mode; 50-mV overdrive, Trise = Tfall (approx.)	–	–	–		–
SID300	TPD1	Response time; power = hi	–	150	–	ns	–
SID301	TPD2	Response time; power = med	–	400	–	ns	–
SID302	TPD3	Response time; power = lo	–	2000	–	ns	–
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
Deep Sleep Mode		Mode 2 is lowest current range. Mode 1 has higher GBW.					Deep Sleep Mode operation: $V_{DDA} \geq 2.7$ V. VIN is 0.2 to V_{DDA} -1.5
SID_DS_1	$I_{DD\_HI\_M1}$	Mode 1, High current	–	1300	1500	µA	Typ at 25 °C
SID_DS_2	$I_{DD\_MED\_M1}$	Mode 1, Medium current	–	460	600	µA	Typ at 25 °C
SID_DS_3	$I_{DD\_LOW\_M1}$	Mode 1, Low current	–	230	350	µA	Typ at 25 °C
SID_DS_4	$I_{DD\_HI\_M2}$	Mode 2, High current	–	120	–	µA	25 °C
SID_DS_5	$I_{DD\_MED\_M2}$	Mode 2, Medium current	–	60	–	µA	25 °C
SID_DS_6	$I_{DD\_LOW\_M2}$	Mode 2, Low current	–	15	–	µA	25 °C
SID_DS_7	GBW_HI_M1	Mode 1, High current	–	4	–	MHz	25 °C
SID_DS_8	GBW_MED_M1	Mode 1, Medium current	–	2	–	MHz	25 °C
SID_DS_9	GBW_LOW_M1	Mode 1, Low current	–	0.5	–	MHz	25 °C
SID_DS_10	GBW_HI_M2	Mode 2, High current	–	0.5	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5V
SID_DS_11	GBW_MED_M2	Mode 2, Medium current	–	0.2	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5V
SID_DS_12	GBW_LOW_M2	Mode 2, Low current	–	0.1	–	MHz	20-pF load, no DC load 0.2 V to V_{DDA}-1.5V
SID_DS_13	$V_{OS\_HI\_M1}$	Mode 1, High current	–	5	–	mV	With trim 25 °C, 0.2V to V_{DDA}-1.5V
SID_DS_14	$V_{OS\_MED\_M1}$	Mode 1, Medium current	–	5	–	mV	With trim 25 °C, 0.2V to V_{DDA}-1.5V
SID_DS_15	$V_{OS\_LOW\_M1}$	Mode 1, Low current	–	5	–	mV	With trim 25 °C, 0.2V to V_{DDA}-1.5V

Table 8. Opamp Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID_DS_16	$V_{OS\_HI\_M2}$	Mode 2, High current	–	5	–	mV	With trim 25 °C, 0.2V to V_{DDA}-1.5V
SID_DS_17	$V_{OS\_MED\_M2}$	Mode 2, Medium current	–	5	–	mV	With trim 25 °C, 0.2V to V_{DDA}-1.5V
SID_DS_18	$V_{OS\_LOW\_M2}$	Mode 2, Low current	–	5	–	mV	With trim 25 °C, 0.2V to V_{DDA}-1.5V
SID_DS_19	$I_{OUT\_HI\_M1}$	Mode 1, High current	–	10	–	mA	Output is 0.5V to V_{DDA}-0.5V
SID_DS_20	$I_{OUT\_MED\_M1}$	Mode 1, Medium current	–	10	–	mA	Output is 0.5 V to V_{DDA}-0.5V
SID_DS_21	$I_{OUT\_LOW\_M1}$	Mode 1, Low current	–	4	–	mA	Output is 0.5V to V_{DDA}-0.5V
SID_DS_22	$I_{OUT\_HI\_M2}$	Mode 2, High current	–	1	–	mA	Output is 0.5V to V_{DDA}-0.5V
SID_DS_23	$I_{OUT\_MED\_M2}$	Mode 2, Medium current	–	1	–	mA	Output is 0.5V to V_{DDA}-0.5V
SID_DS_24	$I_{OUT\_LOW\_M2}$	Mode 2, Low current	–	0.5	–	mA	Output is 0.5V to V_{DDA}-0.5V

Table 9. Low-Power (LP) Comparator Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
LP Comparator DC Specifications							
SID84	$V_{OFFSET1}$	Input offset voltage for COMP1. Normal power mode.	–10	–	10	mV	COMP0 offset is ±25 mV
SID85A	$V_{OFFSET2}$	Input offset voltage. Low-power mode.	–25	±12	25	mV	–
SID85B	$V_{OFFSET3}$	Input offset voltage. Ultra low-power mode.	–25	±12	25	mV	–
SID86	V_{HYST1}	Hysteresis when enabled in Normal mode	–	–	60	mV	–
SID86A	V_{HYST2}	Hysteresis when enabled in Low-power mode	–	–	80	mV	–
SID87	V_{ICM1}	Input common mode voltage in Normal mode	0	–	V_{DDIO1} – 0.1	V	–
SID247	V_{ICM2}	Input common mode voltage in Low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID247A	V_{ICM3}	Input common mode voltage in Ultra low power mode	0	–	V_{DDIO1} – 0.1	V	–
SID88	CMRR	Common mode rejection ratio in Normal power mode	50	–	–	dB	–
SID89	I_{CMP1}	Block Current, Normal Mode	–	–	150	µA	–
SID248	I_{CMP2}	Block Current, Low power Mode	–	–	10	µA	–
SID259	I_{CMP3}	Block Current in Ultra low-power Mode	–	0.3	0.85	µA	–
SID90	ZCMP	DC Input impedance of comparator	35	–	–	MΩ	–

Table 9. Low-Power (LP) Comparator Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
LP Comparator AC Specifications							
SID91	T_{RESP1}	Response time, Normal Mode, 100 mV overdrive	–	–	100	ns	–
SID258	TRESP2	Response time, Low power Mode, 100 mV overdrive	–	–	1000	ns	–
SID92	TRESP3	Response time, Ultra-low power Mode, 100 mV overdrive	–	–	20	µs	–
SID92E	T_CMP_EN1	Time from Enabling to operation	–	–	10	µs	Normal and Low-power modes
SID92F	T_CMP_EN2	Time from Enabling to operation	–	–	50	µs	Ultra low-power Mode

Table 10. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID93	$T_{SENSACC}$	Temperature sensor accuracy	–5	±1	5	°C	–40 to +85 °C

Table 11. Internal Reference Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID93R	V_{REFBG}		1.188	1.2	1.212	V	–

SAR ADC

Table 12. 12-bit SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID94	A_RES	SAR ADC Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended	–	–	16	–	8 full speed.
SID96	A-CHNKS_D	Number of channels - differential	–	–	8	–	Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–	–	Yes
SID98	A_GAINERR	Gain error	–	–	±0.2	%	With external reference.
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1V reference
SID100	A_ISAR_1	Current consumption at 1 Msps	–	–	1	mA	At 1 Msps. External Bypass Cap.
SID100A	A_ISAR_2	Current consumption at 1 Msps. Reference = V_{DD}	–	–	1.25	mA	At 1 Msps. External Bypass Cap.
SID101	A_VINS	Input voltage range - single-ended	Vss	–	V_{DDA}	V	–
SID102	A_VIND	Input voltage range - differential	Vss	–	V_{DDA}	V	–
SID103	A_INRES	Input resistance	–	–	2.2	kΩ	–
SID104	A_INCAP	Input capacitance	–	–	10	pF	–

Table 13. 12-bit SAR ADC AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
12-bit SAR ADC AC Specifications							
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
One Megasample per second mode:							
SID108	A_SAMP_1	Sample rate with external reference bypass cap.	–	–	1	Msps	–
SID108A	A_SAMP_2	Sample rate with no bypass cap; Reference = V_{DD}	–	–	250	ksps	–
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference.	–	–	100	ksps	–
SID109	A_SINAD	Signal-to-noise and Distortion ratio (SINAD). V_{DDA} = 2.7 to 3.6 V, 1 Msps.	64	–	–	dB	Fin = 10 kHz
SID111A	A_INL	Integral Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–2	–	2	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID111B	A_INL	Integral Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–4	–	4	LSB	Measured with external $V_{REF} \geq 1$ V and V_{IN} common mode < 2 * Vref
SID112A	A_DNL	Differential Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.4	LSB	Measured with internal V_{REF} = 1.2 V and bypass cap.
SID112B	A_DNL	Differential Non Linearity. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–1	–	1.7	LSB	Measured with external $V_{REF} \geq 1$ V and V_{IN} common mode < 2 * V_{REF}
SID113	A_THD	Total harmonic distortion. V_{DDA} = 2.7 to 3.6 V, 1 Msps	–	–	–65	dB	Fin = 10 kHz

Table 14. 12-bit DAC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
12-bit DAC DC Specifications							
SID108D	DAC_RES	DAC resolution	–	–	12	bits	–
SID111D	DAC_INL	Integral Non-Linearity	–4	–	4	LSB	–
SID112D	DAC_DNL	Differential Non Linearity	–2	–	2	LSB	Monotonic to 11 bits.
SID99D	DAC_OFFSET	Output Voltage zero offset error	–10	–	10	mV	For 000 (hex)
SID103D	DAC_OUT_RES	DAC Output Resistance	–	15	–	kΩ	–
SID100D	DAC_IDD	DAC Current	–	–	125	µA	–
SID101D	DAC_QIDD	DAC Current when DAC stopped	–	–	1	µA	–
12-bit DAC AC Specifications							
SID109D	DAC_CONV	DAC Settling time	–	–	2	µs	Driving through CTBm buffer; 25-pF load
SID110D	DAC_Wakeup	Time from Enabling to ready for conversion	–	–	10	µs	–

CSD

Table 15. CapSense Sigma-Delta (CSD) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
CSD V2 Specifications							
SYS.PER#3	I_{TCPWM1}	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DDA} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	I_{TCPWM2}	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DDA} > 1.75 V (with ripple), 25 ° C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	I_{TCPWM3}	Maximum block current	–	–	4500	µA	
SID.CSD#15	I_{TCPWM4}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} – 0.6	V	V_{DDA} - V_{REF} ≥ 0.6V
SID.CSD#15A	$TCPWM_{FREQ}$	External Voltage reference for CSD and Comparator	0.6	–	V_{DDA} – 0.6	V	V_{DDA} - V_{REF} ≥ 0.6V
SID.CSD#16	$I_{DAC1IDD}$	IDAC1 (7-bits) block current	–	–	1900	µA	–
SID.CSD#17	$I_{DAC2IDD}$	IDAC2 (7-bits) block current	–	–	1900	µA	–
SID308	V_{CSD}	Voltage range of operation	1.7	–	3.6	V	1.71 to 3.6 V
SID308A	$V_{COMPIDAC}$	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6	V	V_{DDA} - V_{REF} ≥ 0.6V
SID309	$I_{DAC1DNL}$	DNL	–1	–	1	LSB	–
SID310	$I_{DAC1INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SID311	$I_{DAC2DNL}$	DNL	–1	–	1	LSB	
SID312	$I_{DAC2INL}$	INL	–3	–	3	LSB	If V_{DDA} < 2 V then for LSB of 2.4 µA or less
SNRC of the following is Ratio of counts of finger to noise. Guaranteed by characterization.							
SID313_1A	SNRC_1	SRSS Reference. IMO + FLL Clock Source. 0.1 pF sensitivity.	5	–	–	Ratio	9.5 pF max. capacitance
SID313_1B	SNRC_2	SRSS Reference. IMO + FLL Clock Source. 0.3 pF sensitivity.	5	–	–	Ratio	31 pF max. capacitance
SID313_1C	SNRC_3	SRSS Reference. IMO + FLL Clock Source. 0.6 pF sensitivity.	5	–	–	Ratio	61 pF max. capacitance
SID313_2A	SNRC_4	PASS Reference. IMO + FLL Clock Source. 0.1 pF sensitivity.	5	–	–	Ratio	12 pF max. capacitance
SID313_2B	SNRC_5	PASS Reference. IMO + FLL Clock Source. 0.3 pF sensitivity.	5	–	–	Ratio	47 pF max. capacitance
SID313_2C	SNRC_6	PASS Reference. IMO + FLL Clock Source. 0.6 pF sensitivity.	5	–	–	Ratio	86 pF max. capacitance
SID313_3A	SNRC_7	PASS Reference. IMO + PLL Clock Source. 0.1 pF sensitivity.	5	–	–	Ratio	27 pF max. capacitance
SID313_3B	SNRC_8	PASS Reference. IMO + PLL Clock Source. 0.3 pF sensitivity.	5	–	–	Ratio	86 pF max. capacitance
SID313_3C	SNRC_9	PASS Reference. IMO + PLL Clock Source. 0.6 pF sensitivity.	5	–	–	Ratio	168 pF max. capacitance
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2		5.7	µA	LSB = 37.5 nA typ.

Table 15. CapSense Sigma-Delta (CSD) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
SID314A	$IDAC_{1CRT2}$	Output current of IDAC1(7 bits) in medium range	33.7	–	45.6	µA	LSB = 300 nA typ.
SID314B	$IDAC_{1CRT3}$	Output current of IDAC1(7 bits) in high range	270	–	365	µA	LSB = 2.4 µA typ.
SID314C	$IDAC_{1CRT12}$	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	11.4	µA	LSB = 37.5 nA typ. 2X output stage
SID314D	$IDAC_{1CRT22}$	Output current of IDAC1(7 bits) in medium range, 2X mode	67	–	91	µA	LSB = 300 nA typ. 2X output stage
SID314E	$IDAC_{1CRT32}$	Output current of IDAC1(7 bits) in high range, 2X mode. V_{DDA} > 2 V	540	–	730	µA	LSB = 2.4 µA typ. 2X output stage
SID315	$IDAC_{2CRT1}$	Output current of IDAC2 (7 bits) in low range	4.2	–	5.7	µA	LSB = 37.5 nA typ.
SID315A	$IDAC_{2CRT2}$	Output current of IDAC2 (7 bits) in medium range	33.7	–	45.6	µA	LSB = 300 nA typ.
SID315B	$IDAC_{2CRT3}$	Output current of IDAC2 (7 bits) in high range	270	–	365	µA	LSB = 2.4 µA typ.
SID315C	$IDAC_{2CRT12}$	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	11.4	µA	LSB = 37.5 nA typ. 2X output stage
SID315D	$IDAC_{2CRT22}$	Output current of IDAC2(7 bits) in medium range, 2X mode	67	–	91	µA	LSB = 300 nA typ. 2X output stage
SID315E	$IDAC_{2CRT32}$	Output current of IDAC2(7 bits) in high range, 2X mode. V_{DDA} > 2V	540	–	730	µA	LSB = 2.4 µA typ. 2X output stage
SID315F	$IDAC_{3CRT13}$	Output current of IDAC in 8-bit mode in low range	8	–	11.4	µA	LSB = 37.5 nA typ.
SID315G	$IDAC_{3CRT23}$	Output current of IDAC in 8-bit mode in medium range	67	–	91	µA	LSB = 300 nA typ.
SID315H	$IDAC_{3CRT33}$	Output current of IDAC in 8-bit mode in high range. V_{DDA} > 2V	540	–	730	µA	LSB = 2.4 µA typ.
SID320	$IDAC_{OFFSET}$	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink
SID321	$IDAC_{GAIN}$	Full-scale error less offset	–	–	±15	%	LSB = 2.4 µA typ.
SID322	$IDAC_{MISMATCH1}$	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5 nA typ.
SID322A	$IDAC_{MISMATCH2}$	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	6	LSB	LSB = 300 nA typ.
SID322B	$IDAC_{MISMATCH3}$	Mismatch between IDAC1 and IDAC2 in High mode	–	–	5.8	LSB	LSB = 2.4 µA typ.
SID323	$IDAC_{SET8}$	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	$IDAC_{SET7}$	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Table 16. CSD ADC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
CSDv2 ADC Specifications							
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SID95	A_CHNLS_S	Number of channels - single ended	–	–	–	16	–
SIDA97	A-MONO	Monotonicity	–	–	Yes	–	V_{REF} mode
SIDA98	A_GAINERR_VREF	Gain error	–	0.6	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA98A	A_GAINERR_VDDA	Gain error	–	0.2	–	%	Reference Source: SRSS (V_{REF} = 1.20 V, V_{DDA}< 2.2V), (V_{REF} =1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99	A_OFFSET_VREF	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA99A	A_OFFSET_VDDA	Input offset voltage	–	0.5	–	LSb	After ADC calibration, Ref. Src = SRSS, (V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA100	A_ISAR_VREF	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA100A	A_ISAR_VDDA	Current consumption	–	0.3	–	mA	CSD ADC Block current
SIDA101	A_VINS_VREF	Input voltage range - single ended	V_{SSA}	–	V_{REF}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA101A	A_VINS_VDDA	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	(V_{REF} = 1.20 V, V_{DDA} < 2.2 V), (V_{REF} = 1.6 V, 2.2 V < V_{DDA} < 2.7 V), (V_{REF} = 2.13 V, V_{DDA} > 2.7 V)
SIDA103	A_INRES	Input charging resistance	–	15	–	kΩ	–
SIDA104	A_INCAP	Input capacitance	–	41	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio (DC)	–	60	–	dB	–
SIDA107	A_TACQ	Sample acquisition time	–	10	–	µs	Measured with 50 Ω source impedance. 10 µs is default software driver acquisition time setting. Settling to within 0.05%.
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk / (2"(N + 2)). Clock frequency = 50 MHz.	–	25	–	µs	Does not include acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk / (2"(N + 2)). Clock frequency = 50 MHz.	–	60	–	µs	Does not include acquisition time.
SIDA109	A_SND_VRE	Signal-to-noise and Distortion ratio (SINAD)	–	57	–	dB	Measured with 50 Ω source impedance

Table 16. CSD ADC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SIDA109A	A_SND_VDDA	Signal-to-noise and Distortion ratio (SINAD)	–	52	–	dB	Measured with 50 Ω source impedance
SIDA111	A_INL_VREF	Integral Non Linearity. 11.6 ksps	–	–	2	LSB	Measured with 50 Ω source impedance
SIDA111A	A_INL_VDDA	Integral Non Linearity. 11.6 ksps	–	–	2	LSB	Measured with 50 Ω source impedance
SIDA112	A_DNL_VREF	Differential Non Linearity. 11.6 ksps	–	–	1	LSB	Measured with 50 Ω source impedance
SIDA112A	A_DNL_VDDA	Differential Non Linearity. 11.6 ksps	–	–	1	LSB	Measured with 50 Ω source impedance

Digital Peripherals

Table 17. Timer/Counter/PWM (TCPWM) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.TCPWM.1	I_{TCPWM1}	Block current consumption at 8 MHz	–	–	70	µA	All modes (TCPWM)
SID.TCPWM.2	I_{TCPWM2}	Block current consumption at 24 MHz	–	–	180	µA	All modes (TCPWM)
SID.TCPWM.2A	I_{TCPWM3}	Block current consumption at 50 MHz	–	–	270	µA	All modes (TCPWM)
SID.TCPWM.2B	I_{TCPWM4}	Block current consumption at 100 MHz	–	–	540	µA	All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	100	MHz	Fc max = Fcpu Maximum = 100 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input Trigger Pulse Width for all Trigger Events	2/Fc	–	–	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected. Fc is counter operating frequency.
SID.TCPWM.5	$TPWM_{EXT}$	Output Trigger Pulse widths	1.5/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TC_{RES}	Resolution of Counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM Resolution	1/Fc	–	–	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	2/Fc	–	–	ns	Minimum pulse width between Quadrature phase inputs. Delays from pins should be similar.

Table 18. Serial Communication Block (SCB) Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Fixed I^2C DC Specifications							
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	30	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	80	µA	–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	180	µA	–
SID152	I_{I2C4}	I2C enabled in Deep Sleep Mode	–	–	1.7	µA	At 60 °C
Fixed I^2C AC Specifications							
SID153	F_{I2C1}	Bit Rate	–	–	1	Mbps	–
Fixed UART DC Specifications							
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	30	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps	–	–	180	µA	–
Fixed UART AC Specifications							
SID162A	F_{UART1}	Bit Rate	–	–	3	Mbps	ULP Mode
SID162B	F_{UART2}		–	–	8		LP Mode
Fixed SPI DC Specifications							
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	220	µA	–
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	340	µA	–
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	360	µA	–
SID165A	I_{SP14}	Block current consumption at 25 Mbps	–	–	800	µA	–
Fixed SPI AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID166	F_{SPI}	SPI Operating frequency Master and Externally Clocked Slave	–	–	25	MHz	14 MHz max for ULP (0.9 V) Mode
SID166A	F_{SPI_IC}	SPI Slave Internally Clocked	–	–	15	MHz	5 MHz max for ULP (0.9 V) Mode
SID166B	F_{SPI_EXT}	SPI Operating Frequency master (Fscb is SPI Clock)	–	–	Fscb/4	MHz	Fscb max is 100 MHz in LP Mode, 25 MHz in ULP Mode
Fixed SPI Master mode AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	12	ns	20 ns max for ULP (0.9 V) Mode
SID168	T_{DSI}	MISO Valid before SClock capturing edge	5	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	MOSI data hold time	0	–	–	ns	Referred to Slave capturing edge
SID169A	$T_{SSELMSCK1}$	SSEL Valid to first SCK Valid edge	18	–	–	ns	Referred to Master clock edge
SID169B	$T_{SSELMSCK2}$	SSEL Hold after last SCK Valid edge	18	–	–	ns	Referred to Master clock edge

Table 18. Serial Communication Block (SCB) Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Fixed SPI Slave mode AC Specifications for LP Mode (1.1 V) unless noted otherwise.							
SID170	T_{DMI}	MOSI Valid before Sclock Capturing edge	5	–	–	ns	–
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext. Clk. Mode	–	–	20	ns	35 ns max. for ULP (0.9 V) mode
SID171	T_{DSO}	MISO Valid after Sclock driving edge in Internally Clk. Mode	–	–	T_{DSO_EXT} + 3 * Tscb	ns	Tscb is Serial Comm. Block clock period.
SID171B	T_{DSO}	MISO Valid after Sclock driving edge in Internally Clk. Mode with Median filter enabled.	–	–	T_{DSO_EXT} + 4 * Tscb	ns	Tscb is Serial Comm. Block clock period.
SID172	T_{HSO}	Previous MISO data hold time	5	–	–	ns	–
SID172A	$TSSEL_{SCK1}$	SSEL Valid to first SCK Valid edge	65	–	–	ns	–
SID172B	$TSSEL_{SCK2}$	SSEL Hold after Last SCK Valid edge	65	–	–	ns	–

LCD Specifications

Table 19. LCD Direct Drive DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID154	I_{LCDLOW}	Operating current in low-power mode	–	5	–	µA	16 × 4 small segment display at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25 °C.	–	0.6	–	mA	32 × 4 segments 50 Hz
SID158	I_{LCDOP2}	PWM Mode current. 3.3 V bias. 8 MHz IMO. 25 °C.	–	0.5	–	mA	32 × 4 segments 50 Hz

Table 20. LCD Direct Drive AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Memory

Table 21. Flash Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Flash DC Specifications							
SID173	VPE	Erase and program voltage	1.71	–	3.6	V	–
Flash AC Specifications							
SID174	$T_{ROWWRITE}$	Row (Block) write time (erase & program)	–	–	16	ms	Row (Block) = 512 bytes
SID175	$T_{ROWERASE}$	Row erase time	–	–	11	ms	–
SID176	$T_{ROWPROGRAM}$	Row program time after erase	–	–	5	ms	–
SID178	$T_{BULKERASE}$	Bulk erase time (1024 KB)	–	–	11	ms	–
SID179	$T_{SECTORERASE}$	Sector erase time (256 KB)	–	–	11	ms	512 rows per sector
SID178S	$T_{SSERIAE}$	Sub-sector erase time	–	–	11	ms	8 rows per sub-sector
SID179S	$T_{SSWRITE}$	Sub-sector write time; 1 erase plus 8 program times	_	_	51	ms	–
SID180S	T_{SWRITE}	Sector write time; 1 erase plus 512 program times	_	_	2.6	seconds	–
SID180	$T_{DEVPROG}$	Total device program time	–	–	15	seconds	–
SID181	F_{END}	Flash Endurance	100K	–	–	cycles	–
SID182	F_{RET1}	Flash Retention. Ta ≤ 25 °C, 100 k P/E cycles	10	_	_	years	–
SID182A	F_{RET2}	Flash Retention. Ta ≤ 85 °C, 10 k P/E cycles	10	_	_	years	–
SID182B	F_{RET3}	Flash Retention. Ta ≤ 55 °C, 20 k P/E cycles	20	_	_	years	–
SID256	T_{WS100}	Number of Wait states at 100 MHz	3	–	–		–
SID257	T_{WS50}	Number of Wait states at 50 MHz	2	–	–		–

Note
5. It can take as much as 16 milliseconds to write to flash. During this time, the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

System Resources

Table 22. PSoC 61 System Resources

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Power-On-Reset with Brown-out DC Specifications							
Precise POR (PPOR)							
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes. VDDD.	1.54	–	–	V	BOD Reset guaranteed for levels below 1.54 V.
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep. VDDD.	1.54	–	–	V	–
SID192A	V_{DDRAMP}	Maximum power supply ramp rate (any supply)	–	–	100	mV/µs	Active Mode
POR with Brown-out AC Specification							
SID194A	V_{DDRAMP_DS}	Maximum power supply ramp rate (any supply) in Deep Sleep	–	–	10	mV/µs	BOD operation guaranteed
Voltage Monitors DC Specifications							
SID195R	V_{HVD0}	–	1.18	1.23	1.27	V	–
SID195	V_{HVDI1}	–	1.38	1.43	1.47	V	–
SID196	V_{HVDI2}	–	1.57	1.63	1.68	V	–
SID197	V_{HVDI3}	–	1.76	1.83	1.89	V	–
SID198	V_{HVDI4}	–	1.95	2.03	2.1	V	–
SID199	V_{HVDI5}	–	2.05	2.13	2.2	V	–
SID200	V_{HVDI6}	–	2.15	2.23	2.3	V	–
SID201	V_{HVDI7}	–	2.24	2.33	2.41	V	–
SID202	V_{HVDI8}	–	2.34	2.43	2.51	V	–
SID203	V_{HVDI9}	–	2.44	2.53	2.61	V	–
SID204	V_{HVDI10}	–	2.53	2.63	2.72	V	–
SID205	V_{HVDI11}	–	2.63	2.73	2.82	V	–
SID206	V_{HVDI12}	–	2.73	2.83	2.92	V	–
SID207	V_{HVDI13}	–	2.82	2.93	3.03	V	–
SID208	V_{HVDI14}	–	2.92	3.03	3.13	V	–
SID209	V_{HVDI15}	–	3.02	3.13	3.23	V	–
SID211	LVI_IDD	Block current	–	5	15	µA	–
Voltage Monitors AC Specification							
SID212	$T_{MONTRIP}$	Voltage monitor trip time	–	–	170	ns	–

SWD Interface

Table 23. SWD and Trace Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SWD and Trace Interface							
SID214	F_SWDCLK2	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	25	MHz	LP Mode. V_{CCD} = 1.1 V
SID214L	F_SWDCLK2L	1.7 V ≤ V_{DDD} ≤ 3.6 V	–	–	12	MHz	ULP Mode. V_{CCD} = 0.9 V.
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 * T	–	–	ns	–
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 * T	–	–	ns	–
SID217	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 * T	ns	–
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	–
SID214T	F_TRCLK_LP1	With Trace Data setup/hold times of 2/1 ns respectively	–	–	75	MHz	LP Mode. V_{DD} = 1.1 V
SID215T	F_TRCLK_LP2	With Trace Data setup/hold times of 3/2 ns respectively	–	–	70	MHz	LP Mode. V_{DD} = 1.1 V
SID216T	F_TRCLK_ULP	With Trace Data setup/hold times of 3/2 ns respectively	–	–	25	MHz	ULP Mode. V_{DD} = 0.9 V

Internal Main Oscillator

Table 24. IMO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID218	I_{IMO1}	IMO operating current at 8 MHz	–	9	15	µA	–

Table 25. IMO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID223	$F_{IMOTOL1}$	Frequency variation centered on 8 MHz	–	–	±2	%	–
SID227	T_{JITR}	Cycle-to-Cycle and Period jitter	–	±250	–	ps	–

Internal Low-Speed Oscillator

Table 26. ILO DC Specification

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID231	I_{ILO2}	ILO operating current at 32 kHz	–	0.3	0.7	µA	–

Table 27. ILO AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID234	$T_{STARTILO1}$	ILO startup time	–	–	7	µs	Startup time to 95% of final frequency
SID236	$T_{LIODUTY}$	ILO duty cycle	45	50	55	%	–
SID237	$F_{ILOTRIM1}$	32 kHz trimmed frequency	28.8	32	35.2	kHz	±10% variation

Crystal Oscillator Specifications

Table 28. ECO Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
MHz ECO DC Specifications							
SID316	I_{DD_MHz}	Block operating current with Cload up to 18 pF	–	800	1600	µA	Max = 33 MHz, Type = 16 MHz
MHz ECO AC Specifications							
SID317	F_MHz	Crystal frequency range	4	–	35	MHz	–
kHz ECO DC Specification							
SID318	I_{DD_kHz}	Block operating current with 32 kHz crystal	–	0.38	1	µA	–
SID321E	ESR32K	Equivalent Series Resistance	–	80	–	kΩ	–
SID322E	PD32K	Drive level	–	–	1	µW	–
kHz ECO AC Specification							
SID319	F_kHz	32 kHz trimmed frequency	–	32.768	–	kHz	–
SID320	Ton_kHz	Startup time	–	–	500	ms	–
SID320E	FTOL32K	Frequency tolerance	–	50	250	ppm	–

External Clock Specifications

Table 29. External Clock Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID305	$EXTCLK_{FREQ}$	External Clock input Frequency	0	–	100	MHz	–
SID306	$EXTCLK_{DUTY}$	Duty cycle; Measured at VDD/2	45	–	55	%	–

Table 30. PLL Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID305P	PLL_LOCK	Time to achieve PLL Lock	–	16	35	µs	–
SID306P	PLL_OUT	Output frequency from PLL Block	–	–	150	MHz	–
SID307P	PLL_IDD	PLL Current	–	0.55	1.1	mA	Typ. at 100 MHz out.
SID308P	PLL_JTR	Period Jitter	–	–	150	ps	100 MHz output frequency

Table 31. Clock Source Switching Time

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID262	$TCLK_{SWITCH}$	Clock switching from clk1 to clk2 in clock periods	–	–	4 clk1 + 3 clk2	periods	–

Note
6. The undivided output of the FLL must be a minimum of 2.5X the input frequency.

Table 32. Frequency Locked Loop (FLL) Specifications

SPEC ID#	Parameter	Description	Min	Typ	Max	Unit	Details / Conditions
Frequency Locked Loop (FLL) Specifications							
SID450	FLL_RANGE	Input frequency range.	0.001	–	100	MHz	Lower limit allows lock to USB SOF signal (1 kHz). Upper limit is for External input.
SID451	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 1.1 V	24.00	–	100.00	MHz	Output range of FLL divided-by-2 output
SID451A	FLL_OUT_DIV2	Output frequency range. V_{CCD} = 0.9 V	24.00	–	50.00	MHz	Output range of FLL divided-by-2 output
SID452	FLL_DUTY_DIV2	Divided-by-2 output; High or Low	47.00	–	53.00	%	–
SID454	FLL_WAKEUP	Time from stable input clock to 1% of final value on deep sleep wakeup	–	–	7.50	µs	With IMO input, for <10 C change in temperature while in Deep Sleep and Fout ≥ 50 MHz
SID455	FLL_JITTER	Period jitter (1 sigma)	–	–	35.00	ps	50 ps at 48 MHz, 35 ps at 100 MHz
SID456	FLL_CURRENT	CCO + Logic current	–	–	5.50	µA/MHz	–

Table 33. UDB AC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Data Path Performance							
SID249	$F_{MAX-TIMER}$	Max frequency of 16-bit timer in a UDB pair	–	–	100	MHz	–
SID250	$F_{MAX-ADDER}$	Max frequency of 16-bit adder in a UDB pair	–	–	100	MHz	–
SID251	F_{MAX_CRC}	Max frequency of 16-bit CRC/PRS in a UDB pair	–	–	100	MHz	–
PLD Performance in UDB							
SID252	F_{MAX_PLD}	Max frequency of 2-pass PLD function in a UDB pair	–	–	100	MHz	–
Clock to Output Performance							
SID253	$T_{CLK\_OUT\_UDB1}$	Prop. delay for clock in to data out	–	5	–	ns	–
UDB Port Adaptor Specifications							
Conditions: 10-pF load, 3-V V_{DDIO} and V_{DDD}							
SID263	T_{LCLKDO}	LCLK to Output delay	–	–	11	ns	–
SID264	$T_{DINLCLK}$	Input setup time to LCLCK rising edge	–	–	7	ns	–
SID265	$T_{DINLCLKHLD}$	Input hold time from LCLK rising edge	5	–	–	ns	–
SID266	$T_{LCLKHIZ}$	LCLK to Output tristated	–	–	28	ns	–
SID267	T_{FLCLK}	LCLK frequency	–	–	33	MHz	–
SID268	$T_{LCLKDUTY}$	LCLK duty cycle (percentage high)	40%	–	60%	%	–

Table 34. USB Specifications (USB requires LP Mode 1.1-V internal supply)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
USB Block Specifications							
SID322U	Vusb_3.3	Device supply for USB operation	3.15	–	3.6	V	USB Configured, USB Reg. bypassed
SID323U	Vusb_3.3	Device supply for USB operation (functional operation only)	2.85	–	3.6	V	USB Configured, USB Reg. bypassed
SID325U	Iusb_config	Device supply current in Active Mode	–	8	–	mA	VDDD = 3.3V
SID328	Isub_suspend	Device supply current in Sleep Mode	–	0.5	–	mA	VDDD = 3.3V, PICU wakeup
SID329	Isub_suspend	Device supply current in Sleep Mode	–	0.3	–	mA	VDDD = 3.3V, Device disconnected
SID330U	USB_Drive_Res	USB driver impedance	28	–	44	Ω	Series resistors are on chip
SID331U	USB_Pulldown	USB pull-down resistors in Host Mode	14.25	–	24.8	kΩ	–
SID332U	USB_Pullup_Idle	Idle Mode range	900	–	1575	Ω	Bus idle
SID333U	USB_Pullup	Active Mode	1425	–	3090	Ω	Upstream device transmitting

Table 35. QSPI Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SMIF QSPI Specifications. All specs with 15-pF load.							
SID390Q	Fsmifclock	SMIF QSPI output clock frequency	–	–	80	MHz	LP Mode (1.1 V)
SID390QU	Fsmifclocku	SMIF QSPI output clock frequency	–	–	50	MHz	ULP Mode (0.9 V). Guaranteed by Char.
SID397Q	Idd_qspi	Block current in LP mode (1.1 V)	–	–	1900	µA	LP Mode (1.1 V)
SID398Q	Idd_qspi_u	Block current in ULP mode (0.9 V)	–	–	590	µA	ULP Mode (0.9 V)
SID391Q	Tsetup	Input data set-up time with respect to clock capturing edge	4.5	–	–	ns	–
SID392Q	Tdatahold	Input data hold time with respect to clock capturing edge	0	–	–	ns	–
SID393Q	Tdataoutvalid	Output data valid time with respect to clock falling edge	–	–	3.7	ns	–
SID394Q	Tholdtime	Output data hold time with respect to clock rising edge	3	–	–	ns	–
SID395Q	Tseloutvalid	Output Select valid time with respect to clock rising edge	–	–	7.5	ns	–
SID396Q	Tselouthold	Output Select hold time with respect to clock rising edge	Tsclk	–	–	ns	Tsclk = Fsmifclk cycle time

Table 36. Audio Subsystem Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Audio Subsystem specifications							
PDM Specifications							
SID400P	PDM_IDD1	PDM Active current, Stereo operation, 1 MHz clock	–	175	–	µA	16-bit audio at 16 ksps
SID401	PDM_IDD2	PDM Active current, Stereo operation, 3 MHz clock	–	600	–	µA	24-bit audio at 48 ksps
SID402	PDM_JITTER	RMS Jitter in PDM clock	–200	–	200	ps	–
SID403	PDM_CLK	PDM Clock speed	0.384	–	3.072	MHz	–
SID403A	PDM_BLK_CLK	PDM Block input clock	1.024	–	49.152	MHz	–
SID403B	PDM_SETUP	Data input set-up time to PDM_CLK edge	10	–	–	ns	–
SID403C	PDM_HOLD	Data input hold time to PDM_CLK edge	10	–	–	ns	–
SID404	PDM_OUT	Audio sample rate	8	–	48	ksps	–
SID405	PDM_WL	Word Length	16	–	24	bits	–
SID406	PDM_SNR	SNR (A-weighted)	–	100	–	dB	PDM input, 20 Hz to 20 kHz BW
SID407	PDM_DR	Dynamic Range (A-weighted)	–	100	–	dB	20 Hz to 20 kHz BW, -60 dB FS
SID408	PDM_FR	Frequency Response	–0.2	–	0.2	dB	DC to 0.45f. DC Blocking filter off.
SID409	PDM_SB	Stop Band	–	0.566	–	f	–
SID410	PDM_SBA	Stop Band Attenuation	–	60	–	dB	–
SID411	PDM_GAIN	Adjustable Gain	–12	–	10.5	dB	PDM to PCM, 1.5 dB/step
SID412	PDM_ST	Startup time	–	48	–		WS (Word Select) cycles
I2S Specifications. The same for LP and ULP modes unless stated otherwise.							
SID413	I2S_WORD	Length of I2S Word	8	–	32	bits	–
SID414	I2S_WS	Word Clock frequency in LP Mode	–	–	192	kHz	12.288 MHz bit clock with 32-bit word
SID414M	I2S_WS_U	Word Clock frequency in ULP Mode	–	–	48	kHz	3.072 MHz bit clock with 32-bit word
SID414A	I2S_WS_TDM	Word Clock frequency in TDM Mode for LP	–	–	48	kHz	Eight 32-bit channels
SID414X	I2S_WS_TDM_U	Word Clock frequency in TDM Mode for ULP	–	–	12	kHz	Eight 32-bit channels
I2S Slave Mode							
SID430	TS_WS	WS Setup Time to the Following Rising Edge of SCK for LP Mode	5	–	–	ns	–
SID430U	TS_WS	WS Setup Time to the Following Rising Edge of SCK for ULP Mode	11	–	–	ns	–
SID430A	TH_WS	WS Hold Time to the Following Edge of SCK	TMCLK_SOC + 5	–	–	ns	–

Table 36. Audio Subsystem Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID432	TD_SDO	Delay Time of TX_SDO Transition from Edge of TX_SCK for LP Mode	–(TMCLK_SOC + 25)	–	TMCLK_SOC + 25	ns	Associated clock edge depends on selected polarity
SID432U	TD_SDO	Delay Time of TX_SDO Transition from Edge of TX_SCK for ULP Mode	–(TMCLK_SOC + 70)	–	TMCLK_SOC + 70	ns	Associated clock edge depends on selected polarity
SID433	TS_SDI	RX_SDI Setup Time to the Following Edge of RX_SCK in Lp Mode	5	–	–	ns	–
SID433U	TS_SDI	RX_SDI Setup Time to the Following Edge of RX_SCK in ULP Mode	11	–	–	ns	–
SID434	TH_SDI	RX_SDI Hold Time to the Rising Edge of RX_SCK	TMCLK_SOC + 5	–	–	ns	–
SID435	TSCKCY	TX/RX_SCK Bit Clock Duty Cycle	45	–	55	%	–
I2S Master Mode							
SID437	TD_WS	WS Transition Delay from Falling Edge of SCK in LP Mode	–10	–	20	ns	–
SID437U	TD_WS_U	WS Transition Delay from Falling Edge of SCK in ULP Mode	–10	–	40	ns	–
SID438	TD_SDO	SDO Transition Delay from Falling Edge of SCK in LP Mode	–10	–	20	ns	–
SID438U	TD_SDO	SDO Transition Delay from Falling Edge of SCK in ULP Mode	–10	–	40	ns	–
SID439	TS_SDI	SDI Setup Time to the Associated Edge of SCK	5	–	–	ns	Associated clock edge depends on selected polarity
SID440	TH_SDI	SDI Hold Time to the Associated Edge of SCK	TMCLK_SOC + 5	–	–	ns	T is TX/RX_SCK Bit Clock period. Associated clock edge depends on selected polarity.
SID443	TSCKCY	SCK Bit Clock Duty Cycle	45	–	55	%	–
SID445	FMCLK_SOC	MCLK_SOC Frequency in LP Mode	1.024	–	98.304	MHz	FMCLK_SOC = 8 * Bit-clock
SID445U	FMCLK_SOC_U	MCLK_SOC Frequency in ULP Mode	1.024	–	24.576	MHz	FMCLK_SOC_U = 8 * Bit-clock
SID446	TMCLKCY	MCLK_SOC Duty Cycle	45	–	55	%	–
SID447	TJITTER	MCLK_SOC Input Jitter	–100	–	100	ps	–

Table 37. Smart I/O Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID420	SMIO_BYP	Smart I/O Bypass delay	–	–	2	ns	–
SID421	SMIO_LUT	Smart I/O LUT prop delay	–	TBD	–	ns	–

Table 38. Precision ILO (PILO) Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID 430R	I_{PILO}	Operating current	–	1.2	4	µA	–
SID431	F_PILO	PILO nominal frequency	–	32768	–	Hz	T = 25 °C with 20-ppm crystal
SID432R	ACC_PILO	PILO accuracy with periodic calibration	–500	–	500	ppm	–

Ordering Information

Table 39 lists the PSoC 61 part numbers and features.

Table 39. Marketing Part Numbers

Family	MPN	CPU Speed (M4)	CPU Speed (M0+)	Single Core/Dual Core	ULP/LP	Flash	SRAM	No of CTBMs	No. of UDBs	CapSense	GPIOs	CRYPTO	PDM-PCM	SIMO BUCK	Secure Boot	Package
60	CY8C6036BZI-F04	150	–	Single	LP	512	128	0	0	No	104	No	No	No	No	124-BGA
	CY8C6016BZI-F04	50	–	Single	ULP	512	128	0	0	No	104	No	No	No	No	124-BGA
61	CY8C6116BZI-F54	50	–	Single	ULP	512	128	1	12	Yes	104	Yes	Yes	Yes	No	124-BGA
	CY8C6136BZI-F14	150	–	Single	LP	512	128	0	0	Yes	104	No	Yes	Yes	No	124-BGA
	CY8C6136BZI-F34	150	–	Single	LP	512	128	1	12	Yes	104	No	Yes	Yes	No	124-BGA
	CY8C6137BZI-F14	150	–	Single	LP	1024	288	0	0	Yes	104	No	Yes	Yes	No	124-BGA
	CY8C6137BZI-F34	150	–	Single	LP	1024	288	1	12	Yes	104	No	Yes	Yes	No	124-BGA
	CY8C6137BZI-F54	150	–	Single	LP	1024	288	1	12	Yes	104	Yes	Yes	Yes	No	124-BGA
	CY8C6117BZI-F34	50	–	Single	ULP	1024	288	1	12	Yes	104	No	Yes	Yes	No	124-BGA
	CY8C6136FTI-F42	150	–	Single	LP	512	128	0	0	Yes	62	Yes	Yes	Yes	No	Thin 80-WLCSP
	CY8C6136FDI-F42	150	–	Single	LP	512	128	0	0	Yes	62	Yes	Yes	Yes	No	80-WLCSP
	CY8C6137FDI-F02	150	–	Single	LP	1024	288	0	0	No	62	No	Yes	Yes	No	80-WLCSP
	CY8C6117FDI-F02	50	–	Single	ULP	1024	288	0	0	No	62	No	Yes	Yes	No	80-WLCSP

Note
7. The 124-BGA and Thin 80-WLCSP packages are in the process of qualification.

Table 40 lists the field values.

Table 40. MPN Nomenclature

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
6	Architecture	6	PSoC 6
A	Family	0	Value
		1	Programmable
		2	Performance
		3	Connectivity
B	Speed	1	50 MHz
		2	100 MHz
		3	150 MHz
		4	150/50 MHz
C	Flash Capacity	4	128 KB
		5	256 KB
		6	512 KB
		7	1024 KB
D	Package Code	AX	TQFP I (0.8mm pitch)
		AZ	TQFP II (0.5mm pitch)
		LQ	QFN
		BZ	BGA
		FD	WLCSP
		FT	Thin WLCSP
E	Temperature Range	C	Consumer
		I	Industrial
		Q	Extended Industrial (105 °C)
F	Silicon Family	N/A	PSoC 6A
		S	PSoC 6A-S (Example)
		M	PSoC 6A-M (Example)
		L	PSoC 6A-L (Example)
		BL	PSoC 6A-BLE
G	Core	Z	M0+
		F	M4
		D	Dual-Core M4/M0+
XY	Attributes Code	00 – 99	Code of feature set in the specific family
ES	Engineering sample	ES	Engineering samples or not
T	Tape/Reel Shipment	T	Tape and Reel shipment or not

Packaging

PSoC 61 will be offered in a 124-BGA[8] package and 80-ball WLCSP packages in 0.43 mm and 0.33 mm[8] heights. 124 BGA package qualification is in process.

Table 41. Package Dimensions

Spec ID#	Package	Description	Package Drawing Number
PKG_1	124-BGA	124-BGA, 9 mm × 9 mm × 1 mm height with 0.65-mm pitch	001-97718
PKG_2	80-WLCSP	80-WLCSP, 3.7 mm × 3.2 mm × 0.43 mm height with 0.35-mm pitch	002-20310
PKG_3	Thin 80-WLCSP	Thin 80 -WLCSP, 3.7 mm × 3.3 mm × 0.33mm height with 0.35-mm pitch	002-23411

Table 42. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	–	–40	25	85	°C
T_J	Operating junction temperature	–	–40	–	100	°C
T_{JA}	Package θ_{JA} (124-BGA)	–	–	36	–	°C/watt
T_{JC}	Package θ_{JC} (124-BGA)	–	–	15	–	°C/watt
T_{JA}	Package θ_{JA} (80-WLCSP)	–	–	19.9	–	°C/watt
T_{JC}	Package θ_{JC} (80-WLCSP)	–	–	0.2	–	°C/watt
T_{JA}	Package θ_{JA} (Thin 80-WLCSP)	–	–	18.8	–	°C/watt
T_{JC}	Package θ_{JC} (Thin 80-WLCSP)	–	–	0.2	–	°C/watt

Table 43. Solder Reflow Peak Temperature

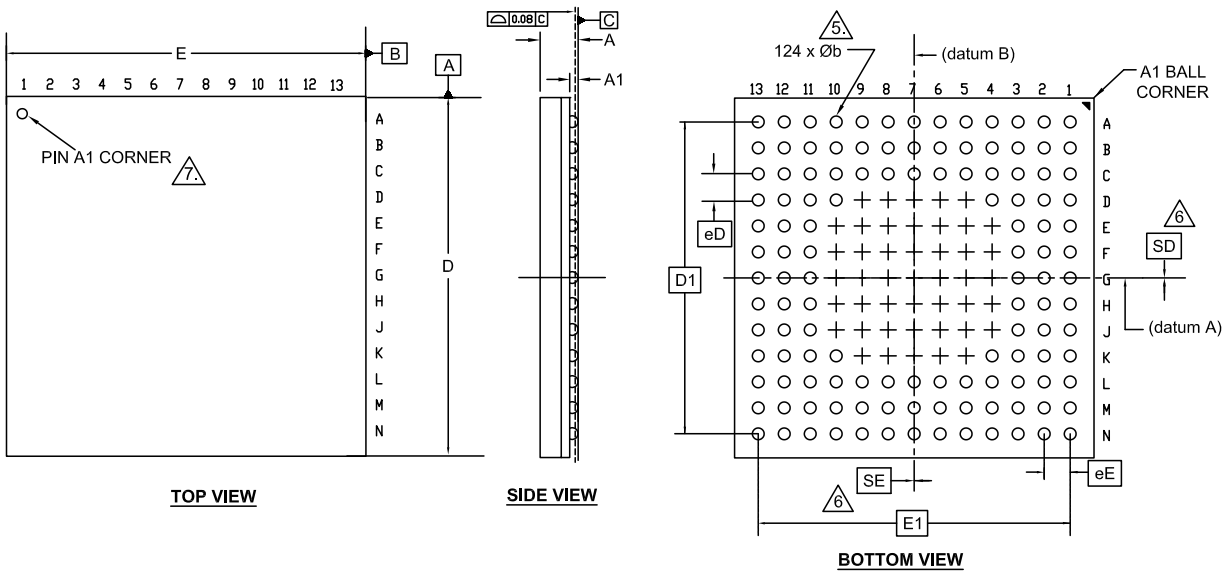
Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
All	260 °C	30 seconds

Table 44. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
124-BGA	MSL 3
80-WLCSP Packages	MSL 1

Note
8. The 124-BGA and Thin 80-WLCSP packages are in the process of qualification.

Figure 4. 124-BGA 9.0 × 9.0 ×1.0 mm



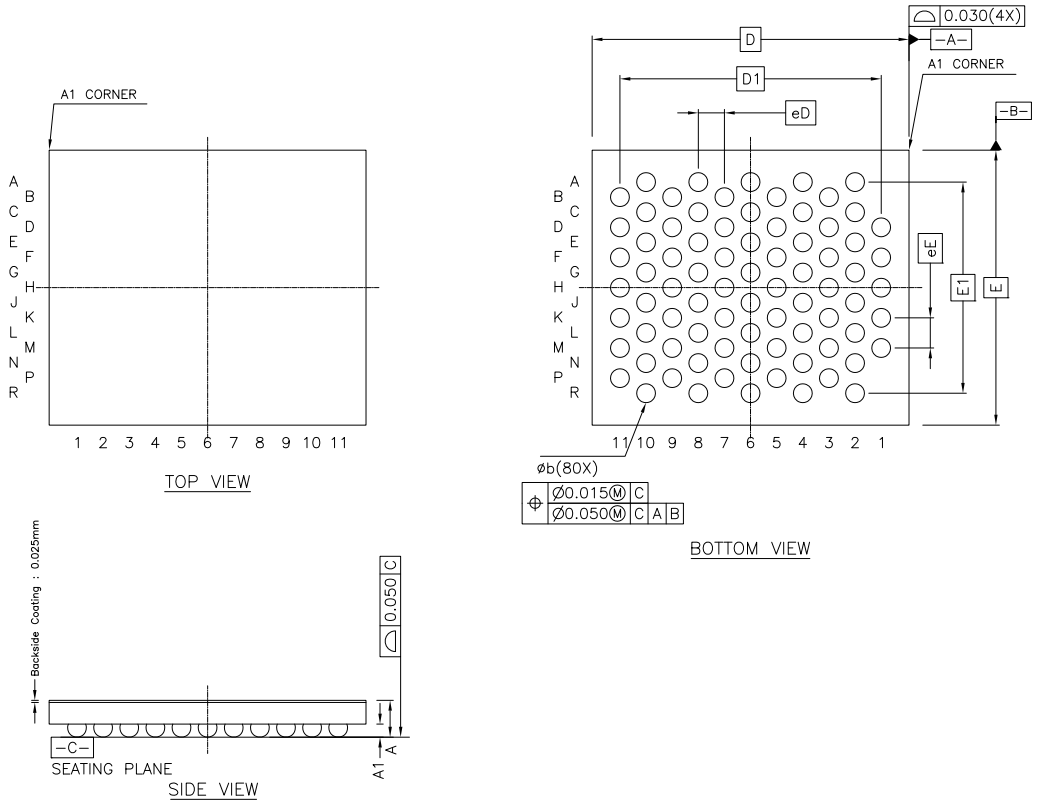
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	0.21	0.26
D	8.90	9.00	9.10
E	8.90	9.00	9.10
D1	7.80 BSC		
E1	7.80 BSC		
MD	13		
ME	13		
N	124		
Ø b	0.25	0.30	0.35
eD	0.65 BSC		
eE	0.65 BSC		
SD	0		
SE	0		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-280.

001-97718 *B

Figure 5. 80-Ball WLCSP 3.676 × 3.190 × 0.467 mm



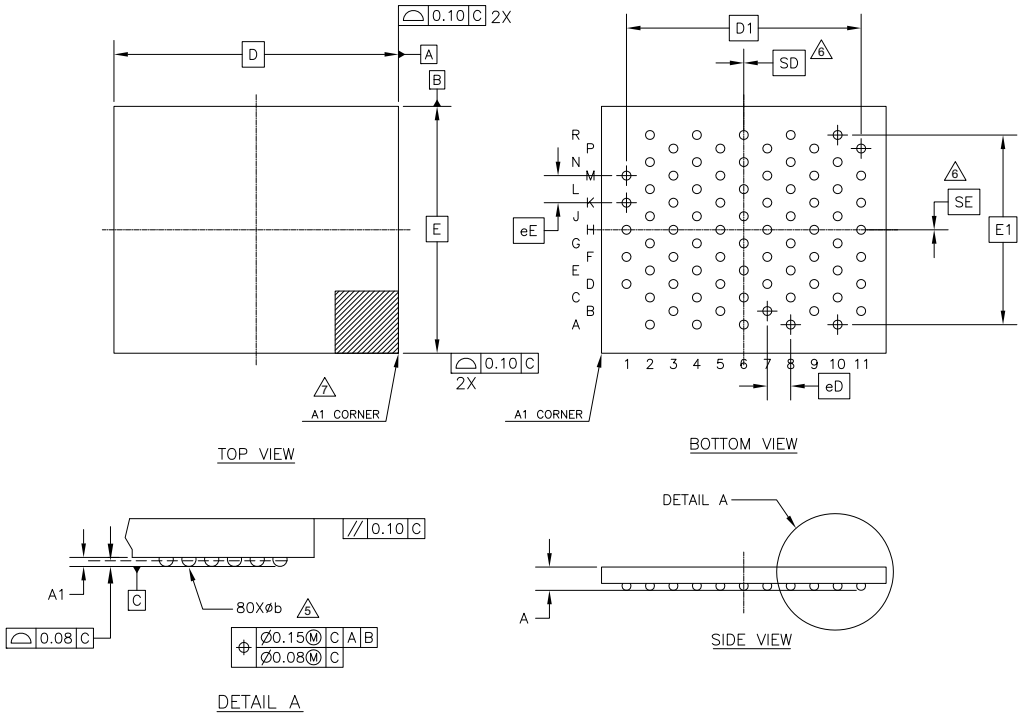
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.387	0.427	0.467
A1	0.122	—	0.182
D	3.676 BSC		
E	3.190 BSC		
D1	3.031 BSC		
E 1	2.450 BSC		
n	80		
Øb	0.188	0.218	0.248
eD	0.303 BSC		
eE	0.350 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.

002-20310 *A

Figure 6. Thin 80-Ball WLCSP 3.676 × 3.190 × 0.33 mm



SYMBOL	DIMENSIONS		
	MIN	NOM	MAX
A	-	-	0.33
A1	0.081	-	-
D	3.676 BSC		
E	3.190 BSC		
D1	3.031 BSC		
E1	2.450 BSC		
MD	11		
ME	15		
N	80		
Øb	0.1035	0.1150	0.1265
eD	0.303 BSC		
eE	0.350 BSC		
SD	0.00 BSC		
SE	0.00 BSC		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. JEDEC SPECIFICATION NO. REF. : N/A

002-23411 **

Acronyms

Table 45. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CSD	CapSense Sigma Delta
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame

Table 45. Acronyms Used in this Document *(continued)*

Acronym	Description
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier

Table 45. Acronyms Used in this Document *(continued)*

Acronym	Description
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset

Table 45. Acronyms Used in this Document *(continued)*

Acronym	Description
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Document Conventions

Units of Measure

Table 46. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision History

Description Title: PSoC® 6 MCU: PSoC 61 Datasheet, Programmable System-on-Chip (PSoC®) Document Number: 002-21414				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5896512	WKA	09/27/2017	New datasheet
*A	5956122	GNKK	11/03/2017	Corrected typo in Development Support.
*B	5974156	WKA	11/29/2017	Updated Table 5. Updated SID84 description and conditions. Updated Table 13. Updated max value for SID223. Updated min and max values of SID432R. Updated Table 39. Updated Revision History
*C	6065337	WKA	02/10/2018	Updated Active CPU power consumption in 32-bit Dual Core CPU Subsystem. Updated Table 5, Table 6, Table 16, Table 21, Table 32, and Table 35. Updated min value for SID4B and SID291. Updated Fixed UART AC specifications. Updated SID190 and removed SID194. Removed SID226. Updated max value for SID234. Updated Revision History.
*D	6190455	WKA	05/29/2018	Corrected typo in the block diagram. Updated 80-ball WLCSP package diagram.
*E	6215538	WKA	06/26/2018	Updated Features and Ordering Information. Updated IMO Clock Source: Corrected the IMO tolerance and locking information and TCPWM and PLL description errors. Updated Packaging: Added Thin 80-WLCSP package dimension and package diagram. Updated Table 39, Table 40, and Table 42.
*F	6221434	WKA	09/08/2018	Removed Preliminary document status. Corrected units usage throughout the document. Added note explaining Fc for the SID.TCPWM.4 parameter. Updated Features, CPU, Flash, ILO Clock Source, Watchdog Timer (WDT), Serial Communication Blocks (SCB), Ordering Information, Packaging, and Acronyms. Removed “Errata” section. Updated package diagram (spec 001-97718 *A to *B) in Packaging. Updated Figure 2. Added a note in Table 2. Updated Table 5, Table 6 through Table 8, Table 15, Table 18, Table 21, Table 30, Table 32, and Table 36.

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