Crystal Image through Imaging Innovation

PIXELPLUS

Multi-Standard Analog HD/SD Video Transmitter

PT1000K

Rev 0.5

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1. General Description

1.1. Product Overview

The PT1000 is Multi-Standard Analog HD/SD Video Transmitter which supports **Any Standard and Resolution of Analog SD/HD video** for Analog DVR System. It accepts various HD digital video input formats such as 16bit BT1120, 8bit interleaved BT1120 and 8bit BT656 format. The PT1000 contains a built-in test pattern generator, input clock jitter reduction and various programmable features such as color space conversion, image adjustment, luminance/ chrominance filter bandwidth. The PT1000 also supports **Bi-Directional Coaxial PTZ** interface so that the information can be transmitted to and received from DVR by host interface.

1.2. Features

- **Video Encoder**
  - ✓ Multi-standard Analog HD and SD Video
    - *All Kind of Analog HD Standard and NTSC/PAL*
  - ✓ Any Resolution of Analog HD and SD Video
    - *1080p25/30, 720p25/30/50/60 and 480i60, 576i50*
  - ✓ Single/Differential Analog Video Output
  - ✓ Input Clock Jitter Reduction
  - ✓ Built-in Video Pattern Generator
  - ✓ Programmable Features
    - *Color Space Conversion*
    - *Contrast/Brightness/Saturation/Hue*
    - *Luminance/Chrominance Filter Bandwidth*
- **Video Input Interface**
  - ✓ 16bit BT1120 @ 37.125/74.25MHz
  - ✓ 8bit/10bit Interleaved BT1120 @ 74.25/148.5MHz
  - ✓ 8bit/10bit BT656 @ 27/36MHz
- **Bi-Directional PTZ Communication**
  - ✓ Flexible Protocol
- **Host Interface**
  - ✓ I2C Serial Interface
- **Low Power Consumption**
  - ✓ 0.26 W

- **Package**
  - ✓ 48 eQFN

1.3. Block Diagram

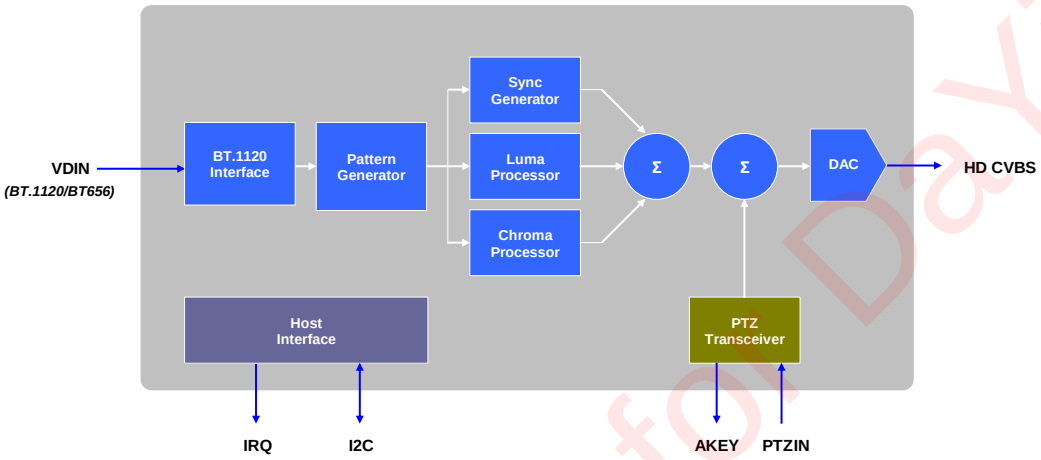


Fig 1. Functional Block Diagram

2. Pin Information

2.1. Pin Diagram

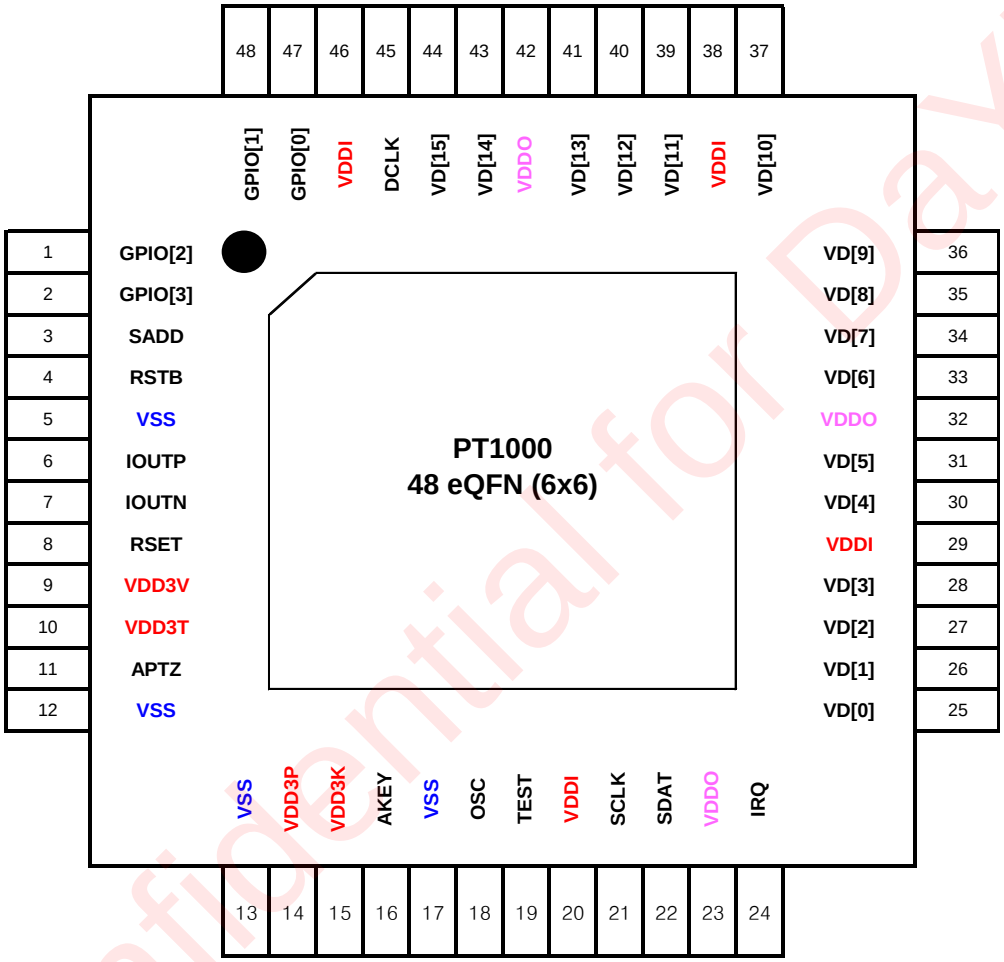


Fig 2. Pin Diagram

2.2. Pin Description

Table 1. Pin Description

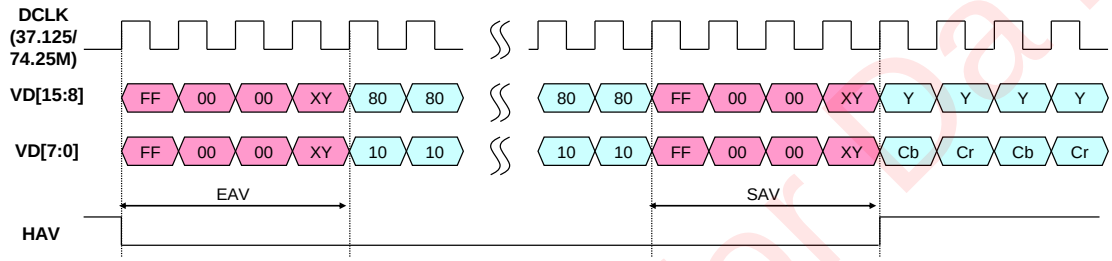
Pin Name	Pin Number	Type	Pin Description
Analog Video Interface (5 Pin)			
IOUTP	6	A	Analog Video Positive Output
IOUTN	7	A	Analog Video Negative Output
RSET	8	A	Video DAC Current Reference
APTZ	11	A	Analog Video Input for PTZ Control
AKEY	16	A	Analog Key Output
Digital Video Interface (17 Pin)			
VD[15:0]	44,43,41,40, 39,37,36,35, 34,33,31,30, 28,27,26,25	I/O	Digital Video Input or GPIO[19:4]
DCLK	45	I	Clock for Digital Video Input
GPIO Interface (4 Pin)			
GPIO[0]	47	O	Multi-Purpose Pin Output 1 or GPIO[0]
GPIO[1]	48	O	Multi-Purpose Pin Output 2 or GPIO[1]
GPIO[2]	1	O	Multi-Purpose Pin Output 3 or GPIO[2]
GPIO[3]	2	O	Multi-Purpose Pin Output 4 or GPIO[3]
System Control Interface (7 Pin)			
TEST	19	I	Reserved Pin for TEST (Should be connected to VSS)
RSTB	4	I	System Reset
OSC	18	I	Crystal (27MHz) Input
SCLK	21	I	I2C Clock Line
SDAT	22	I/O	I2C Data Line
SADD	3	I	I2C Address Control
IRQ	24	O	Interrupt Request Output

Pin Name	Pin Number	Type	Pin Description
Power and Ground (16 Pin)			
VDD3V	9	P	3.0V Power for Analog Video DAC
VDD3P	14	P	3.0V Power for Analog PLL
VDD3T	10	P	3.0V Power for Analog PTZ
VDD3K	15	P	3.0V Power for Analog Key Output
VDDO	23, 32, 42	P	3.0V Power for Digital Output
VDDI	20, 29, 38, 46	P	1.6V Power for Digital Core
VSS	5, 12, 13, 17	G	Ground
Exposed Pad		G	Ground

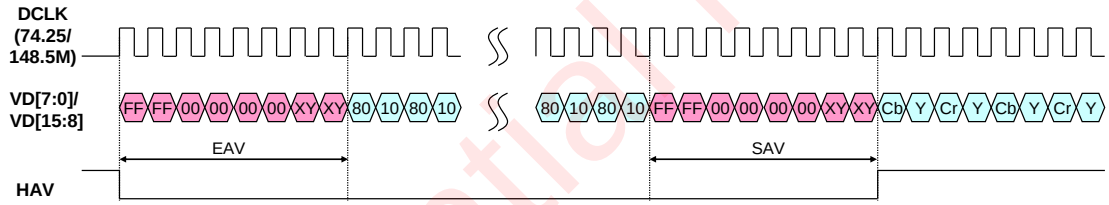
3. Function Description

3.1. Video Input Interface

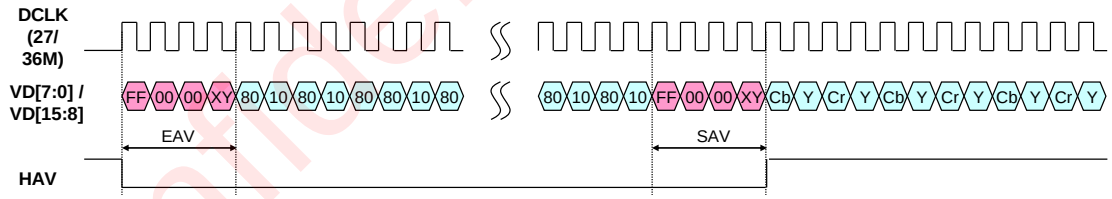
The PT1000 supports 16bits BT1120@37.125/74.25MHz, 8bit/10bit Interleaved BT1120 @74.25/148.5MHz format for HD video input and 8bit/10bit BT656@27/36MHz format for SD video input. The timing diagram of each format is shown in the following



(A) 16bit ITU-R BT.1120 @ 37.125/74.25MHz



(B) 8bit ITU-R BT.1120 @ 74.25/148.5MHz



I ITU-R BT.656 @ 27/36MHz

Fig 3. The Timing Diagram of ITU-R BT.1120/656 Format

The PT1000 also provides a various video input pin configuration like the following table.

Table 2. 16Bit Video Input Pin Configuration

Register/Pin	Value/Data	
IN_PORT_SWAP	**1**	**0**
VD[0]	C[0]	Y[0]
VD[1]	C[1]	Y[1]
VD[2]	C[2]	Y[2]
VD[3]	C[3]	Y[3]
VD[4]	C[4]	Y[4]
VD[5]	C[5]	Y[5]
VD[6]	C[6]	Y[6]
VD[7]	C[7]	Y[7]
VD[8]	Y[0]	C[0]
VD[9]	Y[1]	C[1]
VD[10]	Y[2]	C[2]
VD[11]	Y[3]	C[3]
VD[12]	Y[4]	C[4]
VD[13]	Y[5]	C[5]
VD[14]	Y[6]	C[6]
VD[15]	Y[7]	C[7]

Table 3. 8Bit Video Input Pin Configuration

Register/Pin	Value/Data	
IN_PORT_SWAP	**1**	**0**
VD[0]	YC[0]	-
VD[1]	YC[1]	-
VD[2]	YC[2]	-
VD[3]	YC[3]	-
VD[4]	YC[4]	-
VD[5]	YC[5]	-
VD[6]	YC[6]	-
VD[7]	YC[7]	-
VD[8]	-	YC[0]
VD[9]	-	YC[1]
VD[10]	-	YC[2]
VD[11]	-	YC[3]
VD[12]	-	YC[4]
VD[13]	-	YC[5]
VD[14]	-	YC[6]
VD[15]	-	YC[7]

Table 4. 10Bit Video Input Pin Configuration

Register/Pin	Value/Data	
IN_PORT_SWAP	**1**	**0**
VD[0]	YC[2]	-
VD[1]	YC[3]	-
VD[2]	YC[4]	-
VD[3]	YC[5]	-
VD[4]	YC[6]	-
VD[5]	YC[7]	-
VD[6]	YC[8]	YC[0]
VD[7]	YC[9]	YC[1]
VD[8]	-	YC[2]
VD[9]	-	YC[3]
VD[10]	-	YC[4]
VD[11]	-	YC[5]
VD[12]	-	YC[6]
VD[13]	-	YC[7]
VD[14]	YC[0]	YC[8]
VD[15]	YC[1]	YC[9]

3.2. Video Encoder

The PT1000 supports all existing HD/SD video standard and all video format (1080p@25/30, 720p@25/30/50/60, 480i@60 and 576i@50) by programming registers. The band selected filter adjusts the luminance and chrominance signal processing according to video standard and format. The PT1000 also provides the video control registers such as contrast, brightness, saturation and hue for the picture adjustment and supplies a various color space conversion and an internal video pattern generator.

3.3. Bi-directional Coaxial PTZ

The PT1000 supports any bidirectional Coaxial PTZ protocol that receives and transmits the data between a controller and the PTZ (Pan/Tilt/Zoom) camera. The PT1000 can define the H/V location and line width for PTZ protocol with the register PTZ_RX/TX_HST(0x82/0xB2), PTZ_TX_HPST(0xB9/0xBA) and PTZ_RX/TX_LINE_LEN(0x8B/0xBB). The bit-stream can be comprised of several lines and one line data can be defined via the PTZ_FIFO_WR_DATA (0xA1) register. Each bit width can be controlled by the PTZ_RX/TX_FREQ (0x83~0x88/ 0xB3~0xB8) register. The PTZ_RX/TX data transfer can be programmed easily with IRQ interface in PT1000. After one channel PTZ TX data is programmed and the transfer is done, the PT1000 sends the IRQ data to host, then the host will program the other channel. Likewise, if all predefined quantity of PTZ Rx data is filled in the embedded FIFO, the IRQ data is sent to host, then the host will read the PTZ Rx data from it.

3.4. Host Interface

3.4.1. I2C Interface

The PT1000 supports serial interface consisting of two signals, serial data line SDAT (Pin 22) and clock line SCLK (Pin 21) that should be connected to VDDO via pull up resistors. The PT1000 also provides auto-increment mode of sub-address for multi-byte serial read/write operation. The input pin SADD (Pin 3) is used to select the slave address which are 7'h42 for SADD = 0, 7'h43 for SADD = 1. The maximum data transfer rate on the bus is up to 400kbit/s. The detailed I2C protocol is shown in the following Fig 4.

I2C Slave Address							R/W
1	0	0	0	0	1	SADD	1/0

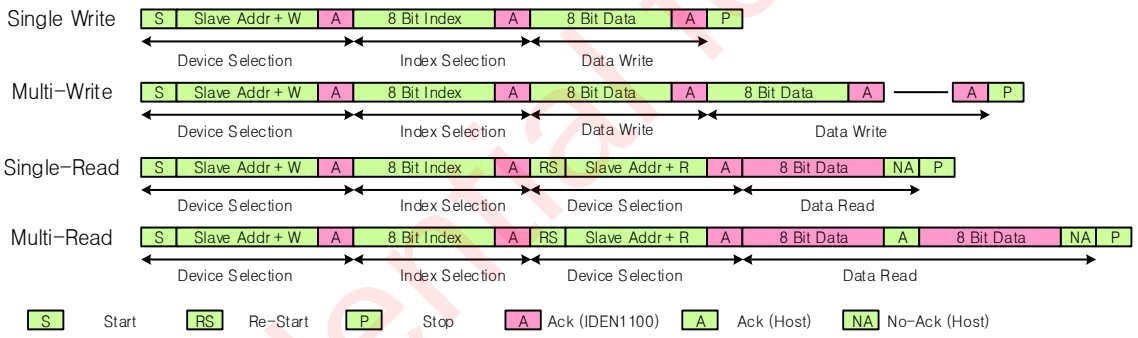


Fig 4. Protocol of I2C Interface

3.4.2. Interrupt Interface

The PT1000 requests the interrupt to host through the IRQ pin. The polarity of IRQ pin is determined by the IRQOUT_POL (0xF0) register. The interrupt is repeated periodically via the IRQOUT_RPT (0xF0) register until the host receives interrupt correctly. The PT1000 requests the interrupt to host when the event of PTZ and GPIO transition happens. Each event can be activated via the IRQENA register. When host receives the interrupt from PT1000, the host should read the IRQCLR register to find out which event requests interrupt service and then write “1” into corresponding bit of the IRQCLR register to clear the interrupt request because the PT1000 maintains the interrupt status until it is cleared. Additionally, the host can read the current state of each event through the IRQ_status register. The event list of interrupt request is described in the following Table 5.

Table 5. Event List of Interrupt Request

Event	Bit Size	Status		Interrupt Mode	
		0	1	Level	Edge
PTZ Tx Done	1	No Operation	PTZ Tx busy	X	Falling
PTZ Tx Empty Error	1	Normal	Tx Empty Error	High	X
PTZ Tx Full Error	1	Normal	Tx Full Error	High	X
PTZ Rx Done	1	Normal	Rx Busy	X	Falling
PTZ Rx Empty Error	1	Normal	Rx Error	High	X
PTZ Rx Full Error	1	Normal	Rx Error	X	Rising
PTZ Rx Start Error	1	Normal	Rx Error	X	Rising
PTZ Rx Data Error	1	Normal	Rx Error	X	Rising
GPIO	4	0	1	O	Rising/Falling/Both

4. Register Description

4.1. Control Register

Addr	Name	R/W	Bits	Descriptions	Default
0x00	ID0	R	[7:0]	Device ID	8'h10
0x01	ID1	R	[7:0]	Device ID	8'h01
~	Reserved			Reserved	
0x08	VID_STATUS	R	[7:3]	Reserved	5'h0E
		R	[2]	Video Field Polarity 0 : Odd Field 1 : Even Field	1'h0
		R	[1]	Video Vertical Locking Status 0 : No Vertical Line is Locked 1 : Vertical Line is Locked	1'h0
		R	[0]	Video Horizontal Line Detection 0 : Horizontal Line is Detected 1 : No Horizontal Line is Detected	1'h0
0x09	VID_HSIZE_ DET_MSB	R	[6:0]	VID_HSIZE_DET[9:3] Detected Active Pixel Size of Video Input (2 Pixel Unit)	7'h0
0x0A	VID_VSIZE_ DET_MSB	R	[6:0]	VID_VSIZE_DET[10:4] Detected Active Line Size of Video Input (1 Line Unit)	7'h0
0x0B	VID_HVSIZE_ DET_LSB	R	[7:5]	VID_HSIZE_DET[2:0]	3'h0
		R	[3:0]	VID_VSIZE_DET[3:0]	4'h0
~	Reserved			Reserved	
0x0E	REV_ID	R	[7:0]	Device Revision Number ID	8'h01
~	Reserved			Reserved	
0x10	IN_PORT_SWAP	R/W	[6]	Swap the Video Input Y/C Port 0 : Normal 1 : Swap the Video Input Port (VD[7:0] <-> VD[15:8])	1'h0

Addr	Name	R/W	Bits	Descriptions	Default
	ENC_LIM_EN	R/W	[4]	Limit Active Data Range 0 : No Limit (1 ~ 254 Range) 1 : 16 ~ 240 Range	1'h0
	RESERVED	R/W	[3]	0 : Normal (Reserved)	1'h0
	HD_IN_MODE	R/W	[2:0]	Select the Video Input Mode [2] : 8/16 Bit or 10/20 Bit Mode 0 : 8/16 Bit Mode 1 : 10/20 Bit Mode [1] : Y/C Multiplexed or Y/C Separate Input Mode 0 : Y/C Time Multiplexed Input 1 : Y/C Separate Input [0] : BT656 or BT1120 0 : BT656 Mode as FF/00/00/XY for SAV/EAV sequence 1 : BT1120 Mode as FFFF/0000/0000/XYXY for SAV/EAV Sequence	3'h0
0x11	TST_PT_EN	R/W	[7]	Enable the Internal Video Test Pattern 0 : Normal 1 : Enable the Internal Video Test Pattern	1'h0
	ENC_CBCR_ SWAP	R/W	[6]	Swap the CB/CR Data 0 : Normal 1 : Swap the CB/CR Data	1'h0
	ENC_FLD_POL	R/W	[5]	Control the Field Polarity 0 : Normal 1 : Field Polarity Inversion	1'h0
	ENC_YC_SWAP	R/W	[4]	Swap the Y/C Data 0 : Normal 1 : Swap the Y/C Data	1'h0

Addr	Name	R/W	Bits	Descriptions	Default
	TST_PT_MODE	R/W	[3:0]	Select the Test Pattern Mode 0 : 720x480i@60Hz, 1 : 720x576i@50Hz 2 : 960x480i@60Hz, 3 : 960x576i@50Hz 4 : 1280x720p@60Hz, 5 : 1280x720p@50Hz 6 : 1280x720p@30Hz, 7 : 1280x720p@25Hz 8 : 1920x1080i@60Hz, 9 : 1920x1080i@50Hz 10 : 1920x1080i@30Hz, 11 : 1920x1080i@25Hz 12 ~ 15 : Reserved	4'h0
0x12	Reserved	R/W	[7:2]	Reserved	
	CSC_MD	R/W	[1:0]	Select the Color Space Conversion Mode [1] : Enable the Color Space Conversion 0 : Bypass CSC 1 : Enable CSC [0] : Color Space Conversion Mode 0 : BT601 to BT709 Conversion 1 : BT709 to BT601 Conversion	2'h0
0x13	TST_PT_SEL	R/W	[7:4]	Select the Video Test Pattern 0 : Black 1 : Blue 2 : Red 3 : Magenta 4 : Green 5 : Cyan 6 : Yellow 7 : White 8 : Color Bar 9 : Gray Bar 10 : Hatch Pattern 11 : Center Box Pattern 12 : H Sweep Pattern 13 : H/V Frequency Sweep Pattern 14 : Mixed Pattern0 15 : Mixed Pattern1	4'h0

Addr	Name	R/W	Bits	Descriptions	Default
	CONT_EN	R/W	[3]	Enable the Contrast Control 0 : Bypass 1 : Enable	1'h0
	BRT_EN	R/W	[2]	Enable the Brightness Control 0 : Bypass 1 : Enable	1'h0
	SAT_EN	R/W	[1]	Enable the Saturation Control 0 : Bypass 1 : Enable	1'h0
	HUE_EN	R/W	[0]	Enable the Hue Control 0 : Bypass 1 : Enable	1'h0
0x14	CONT	R/W	[7:0]	Control the Luminance Contrast 0 : Gain 0 ~ 128 : Gain 1 ~ 255 : Gain 2	8'h80
0x15	BRT	R/W	[7:0]	Control the Luminance Brightness 0 : -50% ~ 128 : 0 ~ 255 : +50%	8'h80
0x16	SAT	R/W	[7:0]	Control the Color Saturation 0 : Gain 0 ~ 128 : Gain 1 ~ 255 : Gain 2	8'h80

Addr	Name	R/W	Bits	Descriptions	Default
0x17	HUE	R/W	[7:0]	Control the Color Hue 0 : - 180 degree ~ 128 : 0 degree ~ 255 : +180 degree	8'h80
0x18	INTERLACE_ MD	R/W	[7]	Select the Interlace Mode 0 : Progressive Mode for HD 1 : Interlace Mode for SD	1'h0
	PHALT	R/W	[6]	Select the Phase Alternation for Color Burst 0 : Normal 1 : Enable the Phase Alternation	1'h0
	PDRST	R/W	[5]	Enable the Color Phase Reset 0 : Normal Operation 1 : Reset the Color Phase Every 4 Frame	1'h0
	Reserved	R/W	[4:0]	Reserved	5'h00
0x19	HSYNC_SLOPE	R/W	[7:6]	Select the HS/VS Transition Time 0 : Slow (32T) ~ 3 : Fast (4T)	2'h0
	BURST_SLOPE	R/W	[5:4]	Select the Burst Transition Time 0 : Slow (32T) ~ 3 : Fast (4T)	2'h0
	VDEL_OFF	R/W	[3]	Control the V Starting Offset 0 : 1 Line Offset 1 : No Offset for PVI Mode (Optional)	1'h0
	Reserved	R/W	[2:0]	Reserved	3'h0
0x1A	HS_STRT_DLY	R/W	[7:0]	HS_STRT_DLY[7:0]	8'h0
0x1B		R/W	[5:0]	HS_STRT_DLY[13:8] Control the H Sync Starting Position from EAV of Input	6'h0

Addr	Name	R/W	Bits	Descriptions	Default
0x1C	Y_GAIN_MSB	R/W	[7:0]	Control the Y Gain MSB [9:2] of Y_GAIN[9:0]	8'h0
0x1D	U_GAIN_MSB	R/W	[7:0]	Control the U Gain MSB [9:2] of U_GAIN[9:0]	8'h0
0x1E	V_GAIN_MSB	R/W	[7:0]	Control the V Gain MSB [9:2] of V_GAIN[9:0]	8'h0
0x1F	V_GAIN_LSB	R/W	[5:4]	Control the V Gain LSB [1:0] of V_GAIN[9:0]	2'h0
	U_GAIN_LSB	R/W	[3:2]	Control the U Gain LSB [1:0] of U_GAIN[9:0]	2'h0
	Y_GAIN_LSB	R/W	[1:0]	Control the Y Gain LSB [1:0] of Y_GAIN[9:0]	2'h0
~	Reserved			Reserved	
0x30	HS_END_POS	R/W	[7:0]	HS_END_POS[7:0]	8'h0
0x31		R/W	[5:0]	HS_END_POS[13:8] Control the H Sync Ending Position	6'h0
0x32	BU_STRT_POS	R/W	[7:0]	BU_STRT_POS[7:0]	8'h0
0x33		R/W	[5:0]	BU_STRT_POS[13:8] Control the Burst Starting Position	6'h0
0x34	BU_END_POS	R/W	[7:0]	BU_END_POS[7:0]	8'h0
0x35		R/W	[5:0]	BU_END_POS[13:8] Control the Burst Ending Position	6'h0
0x36	VE0_END_POS	R/W	[7:0]	VE0_END_POS[7:0]	8'h0
0x37		R/W	[5:0]	VE0_END_POS[13:8] Control the 1st Equalization End Position	6'h0
0x38	VE1_END_POS	R/W	[7:0]	VE1_END_POS[7:0]	8'h0
0x39		R/W	[5:0]	VE1_END_POS[13:8] Control the 2nd Equalization End Position	6'h0
0x3A	VS0_END_POS	R/W	[7:0]	VS0_END_POS[7:0]	8'h0

Addr	Name	R/W	Bits	Descriptions	Default
0x3B		R/W	[5:0]	VS0_END_POS[13:8] Control the 1st Serration Ending Position	6'h0
0x3C	VS1_END_POS	R/W	[7:0]	VS1_END_POS[7:0]	8'h0
0x3D		R/W	[5:0]	VS1_END_POS[13:8] Control the 2nd Serration Ending Position	6'h0
0x3E	VS_HALF_POS	R/W	[7:0]	VS_HALF_POS[7:0]	8'h0
0x3F		R/W	[5:0]	VS_HALF_POS[13:8] Control the Half Line Size for Serration / Equalization	6'h0
0x40	LUMA_ STRT _POS	R/W	[7:0]	LUMA_STRT_POS[7:0]	8'h0
0x41		R/W	[5:0]	LUMA_STRT_POS[13:8] Control the Video Active Luminance Starting Position	6'h0
0x42	LUMA_ END _POS	R/W	[7:0]	LUMA_END_POS[7:0]	8'h0
0x43		R/W	[5:0]	LUMA_END_POS[13:8] Control the Video Active Luminance Ending Position	6'h0
~	Reserved			Reserved	
0x48	CHROMA_ STRT_POS	R/W	[7:0]	CHROMA_STRT_POS[7:0]	8'h0
0x49		R/W	[5:0]	CHROMA_STRT_POS[13:8] Control the Video Active Chrominance Starting Position	6'h0
0x4A	CHROMA_ END_POS	R/W	[7:0]	CHROMA_END_POS[7:0]	8'h0
0x4B		R/W	[5:0]	CHROMA_END_POS[13:8] Control the Video Active Chrominance Ending Position	6'h0
~	Reserved			Reserved	
0x5C	Y_FLT_MD	R/W	[7:4]	Control the Y Filter Bandwidth 0 : Wide ~ 15 : Narrow	4'h0

Addr	Name	R/W	Bits	Descriptions	Default
	C_FLT_MD	R/W	[3:0]	Control the C Filter Bandwidth 0 : Wide ~ 15 : Narrow	4'h0
0x5D	CB_OS	R/W	[7:0]	Control the CB Offset 0 ~ : - CB Offset 128 : Bypass(Default) ~ 256 : + CB Offset	8'h80
0x5E	CR_OS	R/W	[7:0]	Control the CR Offset 0 ~ : - CR Offset 128 : Bypass(Default) ~ 256 : + CR Offset	8'h80
0x5F	SYNC_OS	R/W	[7:0]	Control the Sync Level Offset 0 : No Sync Level Offset (Default) ~ 255 : Max Sync Level Offset	8'h00
0x60	SYNC_LV_LSB	R/W	[7:0]	Control the H/V Sync Amplitude LSB [7:0] of SYNC_LV[9:0]	8'h00
0x61	Reserved	R/W	[7:2]	Reserved	
	SYNC_LV_MSB	R/W	[1:0]	MSB [9:8] of SYNC_LV[9:0]	2'h0
~	Reserved			Reserved	
0x64	PED_OS	R/W	[7:6]	Enable the Pedestal Setup Offset [1] : Enable the Pedestal Offset 0 : Normal 1 : Enable [0] : Control the Pedestal Offset Mode 0 : + 7.5 IRE Setup 1 : - 7.5 IRE Setup	2'h0
	Reserved	R/W	[5:0]	Reserved	
0x65	BURST_LV_LSB	R/W	[7:0]	Control the Color Burst Amplitude LSB [7:0] of BURST_LV[9:0]	8'h0

Addr	Name	R/W	Bits	Descriptions	Default
0x66	FSC_FREE	R/W	[7]	Select the Color Subcarrier Free-Running Mode 0 : Reset Every 4 Frame 1 : Free-running	1'h0
	CHROMA_OFF	R/W	[6]	Select the Chroma Off Mode 0 : Normal 1 : Chroma Off Mode	1'h0
	BURST_LV_LSB	R/W	[1:0]	MSB [9:8] of BURST_LV[9:0]	2'h0
~	Reserved			Reserved	
0x80	PTZ_RX_PATH_EN	R/W	[7]	Enable the PTZ Rx Path 0 : Disable or Initialize for PTZ Rx 1 : Enable the PTZ Rx	1'h0
	PTZ_RX_START	R/W	[6]	Start the PTZ Rx 0 : Null Operation 1 : Start the PTZ Rx	1'h0
	PTZ_RX_IGNORE_LINE_EN	R/W	[5:4]	Enable the PTZ Rx Ignoring Mode 0 : Normal 1 : Line Ignoring Mode 2 : Frame Ignoring Mode for 1st Line PTZ Data	2'h0
	PTZ_RX_IGNORE_FRM_EN	R/W	[3]	Enable the PTZ Rx Frame Ignoring Mode 0 : Normal 1 : Consecutive PTZ Frame Ignoring Mode	1'h0
	PTZ_RX_FLD_POL	R/W	[2]	Control the PTZ Rx Field Polarity 0 : Even Field is High 1 : Odd Field is High	1'h0
	PTZ_RD_FLD_TYPE	R/W	[1:0]	Select the PTZ Rx Field 0 : Both Field 1 : Even 2 : Odd Field 3 : Reserved	2'h0

Addr	Name	R/W	Bits	Descriptions	Default
0x81	PTZ_RX_LINE _CNT	R/W	[7:3]	Select the PTZ Rx Line Size / Frame 0 : Reserved 1 : 1 Line ~ 6 : 6 Line	5'h0
	PTZ_RX_HST _OS	R/W	[2:0]	Select the PTZ Rx Line Starting Offset for Even Fld 0 : + 0 Line Offset 1 : + 1 Line Offset 2 : + 2 Line Offset 3 : + 3 Line Offset 4 : - 0 Line Offset 5 : - 1 Line Offset 6 : - 2 Line Offset 7 : - 3 Line Offset	3'h0
0x82	PTZ_RX_DATA _POL	R/W	[7]	Control the PTZ Rx Data Inversion 0 : Normal 1 : Enable the PTZ Rx Data Inversion	1'h0
	PTZ_RX_HST	R/W	[6:0]	Control the PTZ Rx Valid Line Starting Position	7'h0
0x83	PTZ_RX_ FREQ_FIRST	R/W	[7:0]	MSB [23:16] of PTZ_RX_FREQ_FIRST[23:0]	8'h0
0x84	PTZ_RX_ FREQ_FIRST	R/W	[7:0]	MSB [15:8] of PTZ_RX_FREQ_FIRST[23:0]	8'h0
0x85	PTZ_RX_ FREQ_FIRST	R/W	[7:0]	LSB [7:0] of PTZ_RX_FREQ_FIRST[23:0] PTZ Bit-width for 1st Bit Bit-width = 2^24 / (RX_FREQ_FIRST * 148.5M)	8'h0
0x86	PTZ_RX_FREQ	R/W	[7:0]	MSB [23:16] of PTZ_RX_FREQ [23:0]	8'h0
0x87	PTZ_RX_FREQ	R/W	[7:0]	MSB [15:8] of PTZ_RX_FREQ [23:0]	8'h0
0x88	PTZ_RX_FREQ	R/W	[7:0]	LSB [7:0] of PTZ_RX_FREQ [23:0] PTZ Bit-width for other bits except 1st bit Bit-width = 2^24 / (RX_FREQ * 148.5M)	8'h0

Addr	Name	R/W	Bits	Descriptions	Default
0x89	PTZ_RX_RTZ_EN	R/W	[7]	Select the RX Return-to-Zero Mode 0 : Normal 1 : Return-to-Zero Mode	1'h0
	PTZ_RX_LPF_ LEN	R/W	[5:0]	Select the RX LPF Mode 0 : No Filterring ~ 63 : 63 Taps	6'h0
0x8A	PTZ_RX_H_PIX _OFFSET	R/W	[7:0]	Control the RX H Starting Offset for PTZ Starting Bit 16 Clock Units	8'h0
0x8B	PTZ_RX_ LINE_LEN	R/W	[5:0]	Select the Bit Length / Line for PTZ Data Max 48 bits / Line = 6 Bytes / Line	6'h0
0x8C	PTZ_RX_ VALID_CNT	R/W	[7:0]	Select the All Byte Length / Command for PTZ Data	8'h0
~	Reserved			Reserved	
0x92	PTZ_RX_VO_ AUTO_EN	R/W	[7]	Select the Blanking Level for PTZ Comparator 0 : Manual Mode 1 : Auto Mode	1'h0
	PTZ_RX_VO_ CTRL	R/W	[5:0]	Select the Blanking Level for Manual Setting 0 : 0 Level ~ 63 : Max Level	6'h0
0x93	PTZ_COMP_ BLK_POL	R/W	[7]	Select the Blank Level Output Polarity of PTZ Comparator 0 : Normal 1 : Inversion	1'h0
	PTZ_RX_VL_ CTRL	R/W	[6:4]	Select the Low Level Threshold of PTZ input Vl = blank_level + 100mV * PTZ_RX_VL_CTRL 0 : Low offset ~ 7 : Max Offset	3'h0

Addr	Name	R/W	Bits	Descriptions	Default
	PTZ_COMP_ RXD_POL	R/W	[3]	Select the Data Slicing Output Polarity of PTZ Comparator 0 : Normal 1 : Inversion	1'h0
	PTZ_RX_VH_ CTRL	R/W	[2:0]	Select the High Level Threshold of PTZ input Vh = Vl + 100mV * PTZ_RX_VH_CTRL 0 : Low offset ~ 7 : Max Offset	3'h0
~	Reserved			Reserved	
0x98	AKEY_CMD_EN	R/W	[7]	Select the Auto Mode for PTZ AKEY DAC Output 0 : Manual Mode for PTZ AKEY Output 1 : Auto Mode for PTZ AKEY Output	1'h0
	AKEY_DAC_OUT	R/W	[4:0]	Select the PTZ AKEY DAC Output on Manual Mode for PTZ AKEY Output 5'b00001 : 0 5'b00010 : 1/5 * VDD3T 5'b00100 : 2/5*VDD3T 5'b01000 : 3/5*VDD3T 5'b10000 : 4/5*VDD3T 5'b00000 : VDD3T	5'h0
0x99	AKEY_CLR_EN	R/W	[7]	Enable the Auto Clear Mode for PTZ AKEY 0 : No Clear Mode 1 : Auto Clear Mode	1'h0
	Reserved	R/W	[6]	Reserved	
	PTZ_RX_AKEY_ CLR _TIME	R/W	[3:0]	MSB [11:8] of PTZ_RX_AKEY_CLR_TIME[11:0]	4'h0
0x9A	PTZ_RX_AKEY_ CLR _TIME	R/W	[7:0]	LSB [7:0] of PTZ_RX_AKEY_CLR_TIME[11:0] AKEY Clear Period = 16H period *PTZ_ RX_AKEY_CLR_TIME	8'h0

Addr	Name	R/W	Bits	Descriptions	Default
0xA0	PTZ_WR_ADDR_INIT	R/W	[7]	Initialize the FIFO Write Address 0 : Normal Write 1 : Initialize the Write FIFO Address (Auto Cleared)	1'h0
	PTZ_WR_BIT_SWAP	R/W	[6]	Swap the FIFO Write Data Bit 0 : Write FIFO with host_wr_data[7:0] 1 : Write FIFO with host_wr_data[0:7]	1'h0
	PTZ_FIFO_WR_MD	R/W	[2:0]	Select the Write FIFO Path 0 : Tx Data 1 : Tx Flag Pattern 2 : Tx Flag Data 3 : Reserved 4 : Rx Flag Pattern 5 : Rx Start Flag Pattern 6 : Rx Start Flag Data	3'h0
0xA1	PTZ_FIFO_WR_DATA	R/W	[7:0]	Write FIFO Data	8'h0
0xA2	PTZ_TX_QUEUE_SIZE	R	[7:0]	Status of Remained FIFO size for PTZ Tx Data	8'h0
0xA4	PTZ_RD_ADDR_INIT	R/W	[7]	Initialize the FIFO Read Address 0 : Normal Read 1 : Initialize the Read FIFO Address (Auto Cleared)	1'h0
	PTZ_RD_BIT_SWAP	R/W	[6]	Swap the FIFO Read Data Bit 0 : Read FIFO with host_rd_data[7:0] 1 : Read FIFO with host_rd_data[0:7]	1'h0
	PTZ_PRE_RD_EN	R/W	[4]	Control the Pre Read FIFO 0 : Normal 1 : Pre Read FIFO (Auto Cleared)	1'h0

Addr	Name	R/W	Bits	Descriptions	Default
	PTZ_FIFO_ RD_MD	R/W	[2:0]	Select the Read FIFO Path 0 : Tx Data 1 : Tx Flag Pattern 2 : Tx Flag Data 3 : Rx Data 4 : Rx Flag Pattern 5 : Rx Start Flag Pattern 6 : Rx Start Flag Data	3'h0
0xA5	PTZ_RX_ QUEUE_SIZE	R	[7:0]	Status of Remained FIFO size for PTZ RX Data	8'h0
0xA6	PTZ_RX_DATA	R	[7:0]	Read PTZ FIFO Data	8'h0
0xB0	PTZ_TX_ PATH_EN	R/W	[7]	Enable the PTZ Tx 0 : Disable the PTZ Tx 1 : Enable the PTZ Tx	1'h0
	PTZ_TX_START	R/W	[6]	Start the PTZ Rx 0 : Null Operation 1 : Start the PTZ Rx	1'h0
	PTZ_TX_ FIELD_POL	R/W	[2]	Control the Field Polarity for PTZ Tx 0 : Even Field is High 1 : Odd Field is High	1'h0
	PTZ_TX_ FILED_TYPE	R/W	[1:0]	Select the Field for PTZ Tx 0 : Progressive 1 : Odd Field 2 : Even Field 3 : Reserved	2'h0
0xB1	PTZ_TX_ LINE_CNT	R/W	[7:3]	Select the PTZ Tx Line size per frame 0 : Reserved 1 : 1 Line ~ 31 : 31 Line	5'h0

Addr	Name	R/W	Bits	Descriptions	Default
	PTZ_TX_HST _OS	R/W	[2:0]	Select the PTZ Transmitter Line Starting Offset for Even Fld 0 : + 0 Line Offset 1 : + 1 Line Offset 2 : + 2 Line Offset 3 : + 3 Line Offset 4 : - 0 Line Offset 5 : - 1 Line Offset 6 : - 2 Line Offset 7 : - 3 Line Offset	3'h0
0xB2	PTZ_TX_DATA _POL	R/W	[7]	Select the PTZ Tx Data Polarity 0 : Normal 1 : Data Polarity is Inverted	1'h0
	PTZ_TX_HST	R/W	[6:0]	Control the PTZ Start Line Number	8'h0
0xB3	PTZ_TX_ FREQ_FIRST	R/W	[7:0]	MSB [23:16] of PTZ_TX_FREQ_FIRST[23:0]	8'h0
0xB4		R/W	[7:0]	MSB [15:8] of PTZ_TX_FREQ_FIRST[23:0]	8'h0
0xB5		R/W	[7:0]	MSB [7:0] of PTZ_TX_FREQ_FIRST[23:0] Tx Bit width for 1st PTZ Tx Bit = 1/148.5M x 2^24 / PTZ_TX_FREQ_FIRST	8'h0
0xB6	PTZ_TX_FREQ	R/W	[7:0]	MSB [23:16] of PTZ_TX_FREQ[23:0]	8'h0
0xB7		R/W	[7:0]	MSB [15:8] of PTZ_TX_FREQ [23:0]	8'h0
0xB8		R/W	[7:0]	LSB [7:0] of PTZ_TX_FREQ [23:0] Tx Bit Width of other Bit except 1st PTZ Tx Bit = 1/148.5M x 2^24 / PTZ_TX_FREQ	8'h0
0xB9	PTZ_TX_RTZ_EN	R/W	[7]	Control the PTZ_TX Return-to-Zero Mode 0 : Normal Mode 1 : Return-to-Zero Mode	1'h0
	PTZ_TX_HPST	R/W	[4:0]	MSB [12:8] of PTZ_TX_HPST[12:0]	5'h0
0xBA	PTZ_TX_HPST	R/W	[7:0]	LSB [7:0] of PTZ_TX_HPST[12:0] PTZ Tx Starting Location for Pixel	8'h0

Addr	Name	R/W	Bits	Descriptions	Default
0xBB	PTZ_TX_ LINE_LEN	R/W	[5:0]	Control the PTZ Tx Line Length per frame 0 : Reserved 1 : 1 Line / Frame ~ 63 : 63 Line / Frame	6'h0
0xBC	PTZ_TX_ALL_ DATA _LEN	R/W	[7:0]	Control the All Byte Length / Command for PTZ Data	8'h0
0xBE	PTZ_TX_GRP _EN	R/W	[7]	Enable the Command Repeat Mode 0 : Normal 1 : Enable the Repeat Command Mode with PTZ_TX_CMD_GRP_NUM	1'h0
	PTZ_TX_CMD _GRP _NUM	R/W	[3:0]	Control the PTZ Tx Command Repeat Number 0 : Reserved 1 : 1 Time Transfer ~ 15 : 15 time transfer	4'h0
~	Reserved			Reserved	
0xC0	PTZ_TX_ AUTO_EN	R/W	[7]	Enable the PTZ Tx Auto Restart Mode 0 : Normal 1 : Enable the PTZ Tx Auto Restart Mode Once PTZ Tx is started by PTZ_TX_START, PTZ Tx will be transferred continuously until TX_AUTO_EN is cleared.	1'h0
	PTZ_TX_ MCMD_SIZE	R/W	[6:0]	Select the PTZ Tx Multi-Command Size 0 : Single Command Transfer ~ 127 : 128 Command Transfer	7'h0
~	Reserved			Reserved	
0xC8	PTZ_OUT_EN	R/W	[7]	Enable the PTZ Tx on Video Output 0 : Disable the PTZ Data on Video Output 1 : Enable the PTZ Tx Data on Video Output	1'h0

Addr	Name	R/W	Bits	Descriptions	Default
	Reserved		[6:4]	Reserved	
	PTZ_OUT_LV	R/W	[2:0]	MSB [10:8] of PTZ_OUT_LV[10:0]	3'h0
0xC9	PTZ_OUT_LV	R/W	[7:0]	LSB [7:0] of PTZ_OUT_LV[10:0] Control the PTZ Tx Output Amplitude	8'h0
0xCA	PTZ_REF_HSTRT_OS	R/W	[7:0]	Control the PTZ Reference H Timing	8'h0
0xD0	PLL_PD	R/W	[7]	Enable the PLL Power Down Mode 0 : Normal 1 : PLL Power Down Mode	1'h0
0xD1	CLK_IN_INV	R/W	[7]	Control the Clock Inversion for CLK_IN 0 : Normal 1 : Inversion	1'h0
	CLK_RD_INV	R/W	[6]	Control the Clock Inversion for CLK_RD 0 : Normal 1 : Inversion	1'h0
	Reserved		[5:0]	Reserved	6'h22
0xD4	DAC_PD	R/W	[6]	Control the Video DAC Power Down 0 : Normal 1 : Video DAC Power Down	1'h0
0xD5	APTZ_PD	R/W	[7]	Control the APTZ Power Down 0 : Normal 1 : APTZ Power Down	1'h0
0xD7	IRQ_IOB	R/W	[4]	Control the IRQ Pin Direction 0 : Output Mode 1 : Input Mode	1'h1
	GPIO_IOB	R/W	[3:0]	Control the GPIO Pin Direction 0 : Output Mode 1 : Input Mode	4'hF

Addr	Name	R/W	Bits	Descriptions	Default
0xD8	VD0_IOB	R/W	[7:0]	Control the VD[7:0] Pin Direction 0 : Output Mode 1 : Input Mode	8'hFF
0xD9	VD1_IOB	R/W	[7:0]	Control the VD[15:8] Pin Direction 0 : Output Mode 1 : Input Mode	8'hFF
0xDA	IRQ_OUT_DATA	R/W	[4]	IRQ Output Data	1'h0
	GPIO_OUT_DATA	R/W	[3:0]	GPIO Output Data	4'h0
0xDB	VD0_OUT_DATA	R/W	[7:0]	VD[7:0] Output Data	8'h0
0xDC	VD1_OUT_DATA	R	[7:0]	VD[15:8] Output Data	8'h0
0xDD	IRQ_VALUE	R	[4]	IRQ Input Data	1'h0
	GPIO_VALUE	R	[3:0]	GPIO Input Data	4'h0
0xDE	VD0_VALUE	R	[7:0]	VD[7:0] Input Data	8'h0
0xDF	VD1_VALUE	R	[7:0]	VD[15:8] Input Data	8'h0
0xE0	GPIO_VD0_MD	R/W	[7]	Select the VD0 Pin Mode 0 : Normal VD Mode 1 : GPIO Mode	1'h0
	GPIO_IRQ_MD	R/W	[7]	Select the IRQ Pin Mode 0 : Normal IRQ Mode 1 : GPIO Mode	1'h0
	Reserved		[5:0]	Reserved	
0xF0	IRQ_OUT_MD	R/W	[7:6]	Select the IRQ_OUT Pin Mode 0 : Disable 1 : Output Drive Mode 2 : Pull-up/down Mode	2'h0
	IRQ_OUT_POL	R/W	[5]	Select the IRQ Output Polarity 0 : Active High 1 : Active Low	1'h0

Addr	Name	R/W	Bits	Descriptions	Default
	IRQ_OUT_RPT	R/W	[4]	Enable the IRQ Toggle Mode 0 : No Toggle Mode 1 : Enable the IRQ Toggle Mode	1'h0
	IRQ_GPIO_MD	R/W	[3:0]	Select the interrupt Mode for GPIO Pin 0 : Edge Interrupt 1 : Level Interrupt	4'h0
0xF1	IRQ_GPIO_BOTH	R/W	[7:4]	Select the Interrupt Mode for GPIO @IRQ_GPIO_MD = 0 0 : Interrupt by IRQ_GPIO_LV 1 : Interrupt by Rising or Falling Edge	4'h0
	IRQ_GPIO_LV	R/W	[3:0]	Select the Interrupt Mode of GPIO 0 : Low Level Interrupt 1 : High Level Interrupt	4'h0
0xF2	IRQ_ENA_GPIO	R/W	[3:0]	Enable the IRQ Output for GPIO Event 0 : Disable the IRQ Output for GPIO Event 1 : Enable the IRQ Output for GPIO Event	4'h0
0xF3	IRQ_ENA_PTZ	R/W	[7:0]	Enable the IRQ Output for PTZ Event [7] : PTZ Rx Data Error [6] : PTZ Rx Frame Start Sync Error [5] : PTX Rx FIFO Overflow Error [4] : PTZ Rx FIFO Empty Error [3] : PTZ Rx Done [2] : PTZ Tx FIFO Overflow Error [1] : PTZ Tx FIFO Empty Error [0] : PTZ Tx Done 0 : Disable the IRQ Output for PTZ Event 1 : Enable the IRQ Output for PTZ Event	8'h0
0xF4	IRQ_CLR_GPIO	R/W	[3:0]	Clear the IRQ for GPIO Event 0 : Null 1 : Clear the IRQ for GPIO Event (Auto Cleared)	4'h0

Addr	Name	R/W	Bits	Descriptions	Default
0xF5	IRQ_CLR_PTZ	R/W	[7:0]	Clear the IRQ for PTZ Event [7] : PTZ Rx Data Error Clear [6] : PTZ Rx Frame Start Sync Error Clear [5] : PTX Rx FIFO Overflow Error Clear [4] : PTZ Rx FIFO Empty Error Clear [3] : PTZ Rx Done Clear [2] : PTZ Tx FIFO Overflow Error Clear [1] : PTZ Tx FIFO Empty Error Clear [0] : PTZ Tx Done Clear 0 : Null 1 : Clear the IRQ for PTZ Event (Auto Cleared)	8'h0
0xF6	IRQ_PED_ GPIO	R	[3:0]	Pending Status for GPIO Event 0 : No Event 1 : Pending Event	4'h0
0xF7	IRQ_PED_ PTZ	R	[7:0]	Pending Status for PTZ Event [7] : PTZ Rx Data Error Pending [6] : PTZ Rx Frame Start Sync Error Pending [5] : PTX Rx FIFO Overflow Error Pending [4] : PTZ Rx FIFO Empty Error Pending [3] : PTZ Rx Done Pending [2] : PTZ Tx FIFO Overflow Error Pending [1] : PTZ Tx FIFO Empty Error Pending [0] : PTZ Tx Done Pending 0 : No Event 1 : Pending Event	8'h0
0xF8	IRQ_STATUS_ GPIO	R	[3:0]	Current Status of GPIO Pin	4'h0

Addr	Name	R/W	Bits	Descriptions	Default
0xF9	IRQ_STATUS_ PTZ	R	[7:0]	Current Status of PTZ Event [7] : PTZ Rx Data Error (High Error) [6] : PTZ Rx Frame Start Sync Error (High Error) [5] : PTX Rx FIFO Overflow Error(High Error) [4] : PTZ Rx FIFO Empty Error(High Error) [3] : PTZ Rx Done (High Busy) [2] : PTZ Tx FIFO Overflow Error(High Error) [1] : PTZ Tx FIFO Empty Error(High Error) [0] : PTZ Tx Done(High Busy)	8'h0

5. Electrical Characteristics

5.1. DC Electrical Characteristics

Table 6. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V/3P/3T/3K, VDDO Pin	-0.5		5.4	V	
Voltage for VDDI Pin	-0.5		2.97	V	
Voltage for Digital Input Pin	-0.5		3.8	V	
Storage Temperature	-55		150	°C	
Junction Temperature	-40		125	°C	
Peak Temperature on Reflow Soldering			260	°C	30 Sec

NOTE: Long-term exposure to absolute maximum ratings may affect device reliability, and permanent damage may occur if operate exceeding the rating. The device should be operated under recommended operating condition

Table 7. Recommended Operating Conditions for Power and Temperature

Parameter	Min	Typ	Max	Unit	Condition
Voltage for VDD3V/3P/3T/3K, VDDO	2.8	3.0	3.3	V	
Voltage for VDDI	1.44	1.6	1.76	V	
Ambient Operation Temperature	-40		70	°C	

Table 8. Recommended Operating Conditions for Digital I/O

Parameter	Min	Typ	Max	Unit	Condition
Digital Inputs					
Input High Voltage	2.0		3.6	V	
Input Low Voltage	-0.3		0.8	V	
Input Capacitance		6		pF	
Input Leakage Current			±10	uA	
Digital Output					
Output High Voltage	2.4			V	
Output Low Voltage			0.4	V	
High Level Output Current	9.2	19.6	30.8	mA	Voh = 2.4V
Low Level Output Current	8.0	12.4	15.6	mA	Vol = 0.4V
Tri-state Output Current			±10	uA	
Output Capacitance		6		pF	

Table 9. Supply Current and Power Dissipation

Parameter	Min	Typ	Max	Unit	Condition
Supply Current at VDDI	113	125	138	mA	
Supply Current at VDD3V/3P/3T/3K, VDDO	15	17	19	mA	
Power Dissipation	0.20	0.25	0.30	W	

5.2. AC Electrical Characteristics

Table 10. Analog Input and Output Parameter

Parameter	Symbol	Min	Typ	Max	Unit
Video DAC					
Differential Non-Linearity Error	DLE		± 0.5	± 1	LSB
Integral Non-Linearity Error	ILE		± 1	± 2	LSB
Full Scale Output Voltage	V_{OFULL}		1.2		Vpp
Analog Clock PLL					
RMS Jitter	rms_{pll}		8		Ps
Duty Cycle	dt_{pll}	45		55	%
Lock Time	t_{lock}		50		us
Crystal Input					
Nominal Frequency	$f_{x\text{-}tal}$		27		MHz
Frequency Deviation	$\Delta f_{x\text{-}tal}$	-50		50	ppm
Duty Cycle	$dt_{x\text{-}tal}$			55	%

Table 11. Serial Host Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
Bus free time between STOP and START	t1	1.3			us
Data Hold time	t2	0		0.9	us
Data Setup time	t3	0.1			us
Setup time for a(repeated) START condition	t4	0.6			us
Setup time for a STOP condition	t5	0.6			us
Hold time (repeated) START	t6	0.6			us
Rise time SDA and SCL signal	t7			250	ns
Fall time SDA and SCL signal	t8			250	ns
Capacitive load for each bus line	C_b			400	pF
I^2C Clock frequency	f_{I2C}			400	KHz

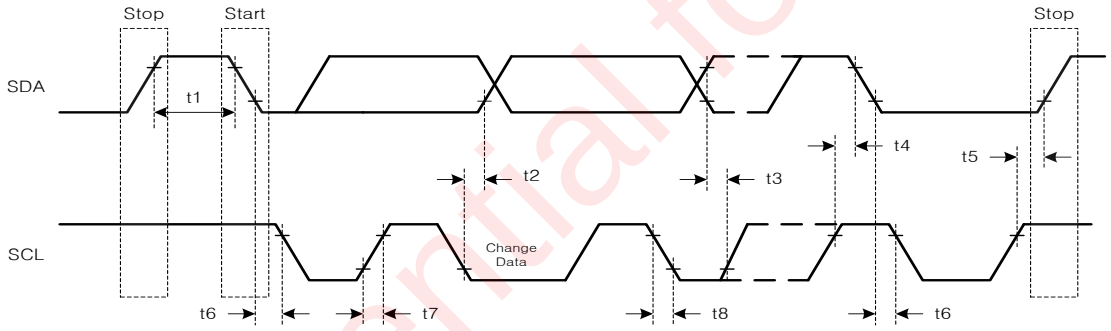
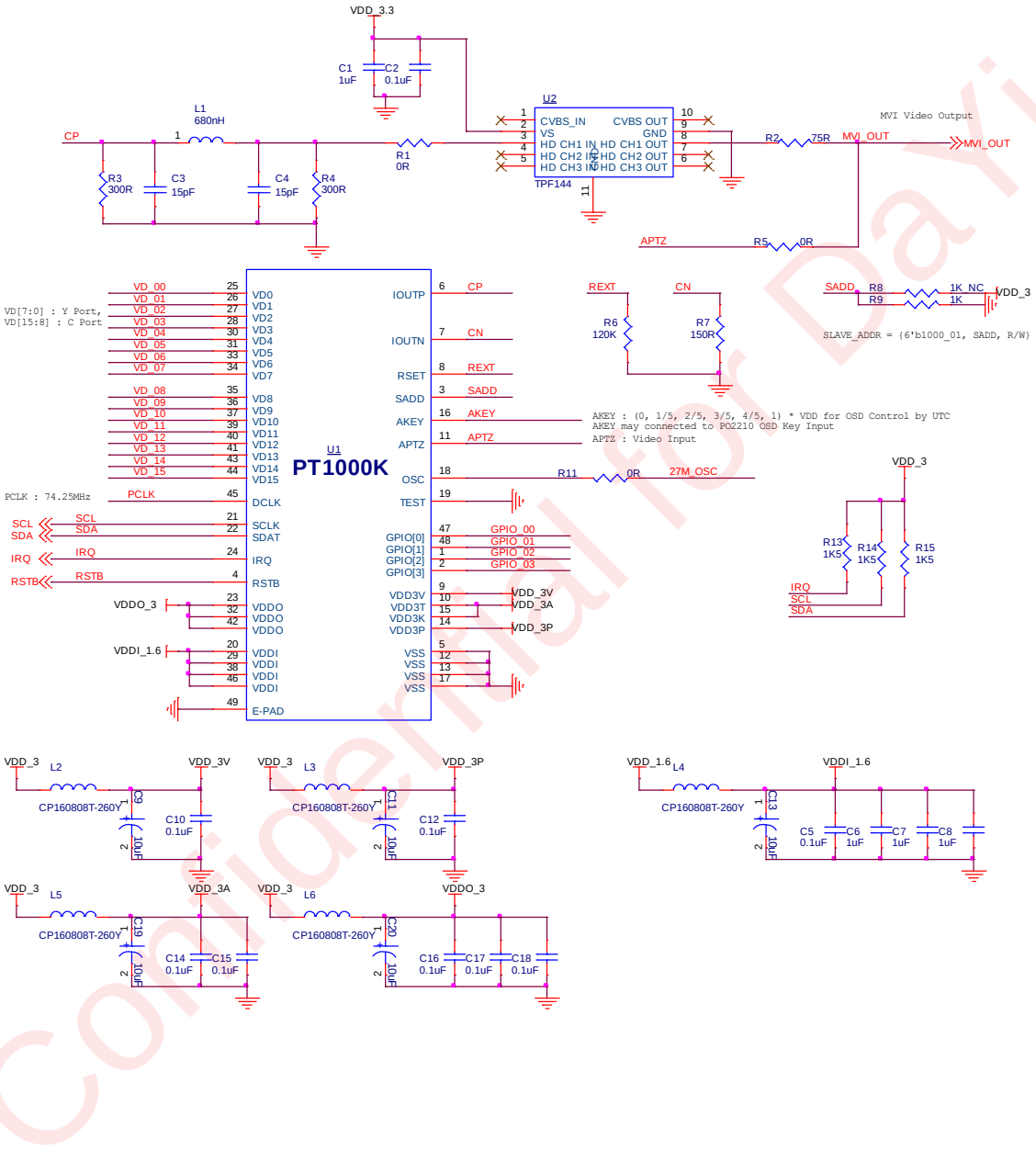


Fig 5. Serial Host Interface Timing Diagram

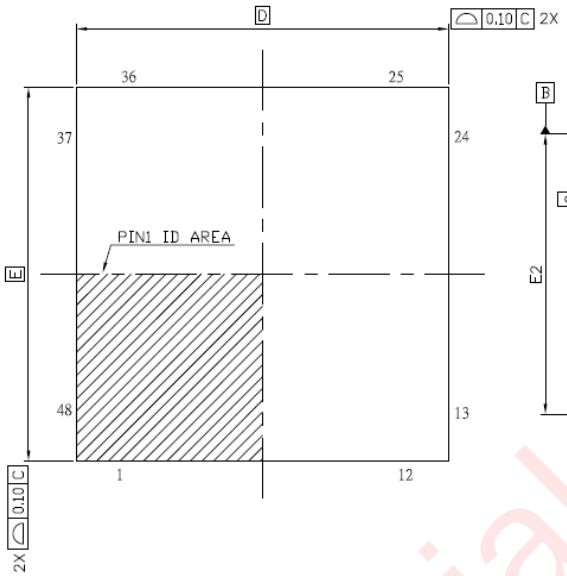
6. Application Schematic



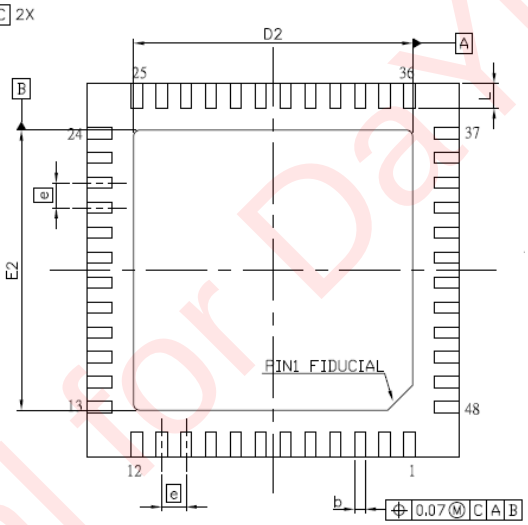
7. Package Specification

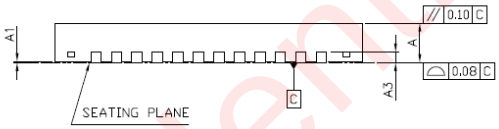
48Pin eQFN Package Mechanical Drawing

TOP VIEW



BOTTOM VIEW





SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	28	30	32
A1	0	0.02	0.05	0	0.8	2.0
A3		0.203 REF			8 REF	
⚠ b	0.15	0.20	0.25	6	8	10
D	5.90	6.00	6.10	232	236	240
D2	4.40	4.50	4.60	173	177	181
E	5.90	6.00	6.10	232	236	240
E2	4.40	4.50	4.60	173	177	181
e		0.40 BSC			16 REF	
L	0.30	0.40	0.50	12	16	20

NOTE:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. REFER TO JEDEC STD. MO-220 ISSUE"K" WJJE
3. LEADFRAME MATERIAL IS OLIN194 AND THICKNESS IS 0.203mm (8 MIL)

8. Revision History

Version	Date	Description
V0.0	2016.01.26	Preliminary Brief Datasheet is Released
V0.1	2016.05.12	Register Descriptions are Added
V0.2	2016.05.16	Change the IN_PORT_INV to IN_PORT_SWAP (P.11 ~ 13)
V0.3	2016.06.16	Recommended Operating Condition of VDD3V/3P/3T/3K, VDDO is Modified (P.38 ~ 39)
V0.4	2016.09.19	Modify the DC Electrical Characteristics (P.38)
V0.41	2017.09.13	Modify the VDDI_1.6 name (P42)
V0.42	2017.09.14	Modify the VDDO_3 name (P42)
V0.5	2018.06.26	Remove IN_BIT_SWAP Function (P.11~P13, P18)