PT1109

1.5A,24V,380KHz Step-Down Converter

GENERAL DESCRIPTION

The PT1109 is a monolithic step-down switch mode regulator with a built in internal power MOSFET. It achieves 1.5A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. In shutdown mode the regulator draws 23μA of supply current.

The PT1109 requires a minimum number of readily available standard external components.

FEATURES

- 1.5A Output Current
- 0.5Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 23μA Shutdown Mode
- Fixed 380KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75V to 24V Operating Input Range
- Output Adjustable from 1.13V to 18V
- Programmable Under Voltage Lockout
- Available in 8-Pin SOP8 Packages

APPLICATION

- PC Monitors
- Distributed Power Systems
- Battery Charger
- Pre-Regulator for Linear Regulators

TYPICAL APPLICATION CIRCUIT

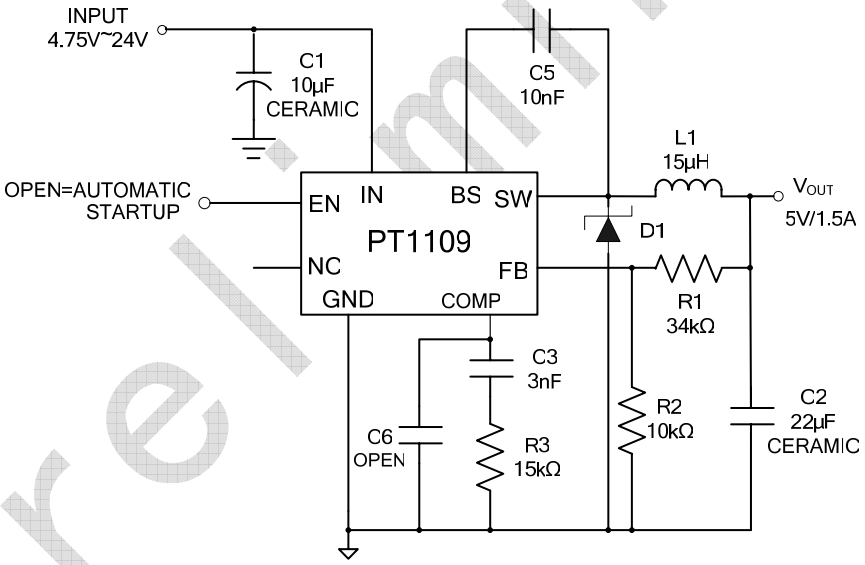
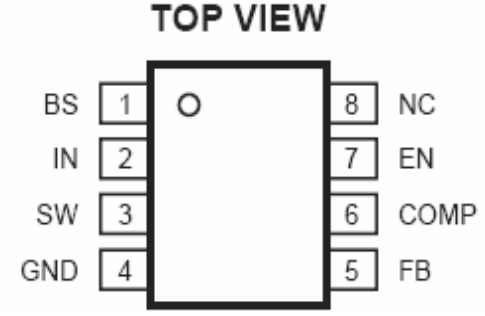


Figure 1

PIN ASSIGNMENT



SOP8

PIN DESCRIPTIONS

SOP8 PIN No.	PIN NAMES	DESCRIPTION
1	BS	Bootstrap (C5) - This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BS pins to forma floating supply across the power switch driver. The voltage across C5 is about 5V and is supplied by the internal +5V supply when the SW pin voltage is low.
2	IN	Supply Voltage - The PT1109 operates from a +4.75V to +24V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
3	SW	Switch - This connects the inductor to either IN through M1 or to GND through M2.
4	GND	Ground - This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
5	FB	Feedback - An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency fold-back comparator lowers the oscillator frequency when the FB voltage is below 700mV.
6	COMP	Compensation - This node is the output of the trans-conductance error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground. See the compensate-on section for exact details.
7	EN	Enable/UVLO - A voltage greater than 2.5V enables operation. Leave EN unconnected if unused. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from VIN to GND. For complete low current shutdown it's the EN pin voltage needs to be less than 0.7V.
8	NC	No connected

ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	ITEMS	VALUE	UNIT
IN	Supply Voltage	-0.3~36	V
SW	Switch Node voltage	-0.3~36	V
BS	Bootstrap Voltage	-0.3~Vsw+5	V
FB	Feedback voltage	-0.3~6	V
EN	Enable/UVLO voltage	-0.3~6	V
COMP	Comp voltage	-0.3~6	V
TOPT	Operation temperature	-20~+85	℃
TSTG	Storage temperature range	-65~+150	℃

RECOMMENDED OPERATING RANGE

SYMBOL	ITEMS	VALUE	UNIT
VIN	Supply voltage	4.75~24	V
TEMP	Operating temperature	-20~+85	℃

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_{IN}=12V, V_{OUT}=5V, load=0.5A, T_A=25 °C, unless specified otherwise.

SYMBOL	ITEMS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ipd	Shutdown supply current	Ven = 0V		23	36	uA
Iq	Supply current	EN floating; Vfb=1.4v		1.1	1.3	mA
Vfb	Feedback voltage		1.098	1.130	1.162	V
Av	Error amplifier voltage gain			400		V/V
Gea	Error amplifier trans-conductance	ΔIcomp=+/-10uA	550	800	1150	uA/V
R_dson1	High side switch on resistance			0.5		Ω
R_dson2	Low side switch on resistance			6.5		Ω
I_leakage	High side switch leakage current	Ven=0V; Vsw=0V		0	10	uA
I_cl	Current limit		1.9	2.8		A
Gcomp	Current sense to COMP trans-conductance			1.5		A/V
Fosc1	Oscillation frequency			380		kHz
Fosc2	Short circuit oscillation frequency	Vfb=0.3V		42		kHz
Dmax	Maximum duty cycle	Vfb=1.0V		90		%
Ven	EN threshold voltage		0.7	1.0	1.4	V
Ien	Enable pull up current	Ven=0V		1.0		uA
TSD	Thermal shutdown			160		ºC

SIMPLIFIED BLOCK DIAGRAM

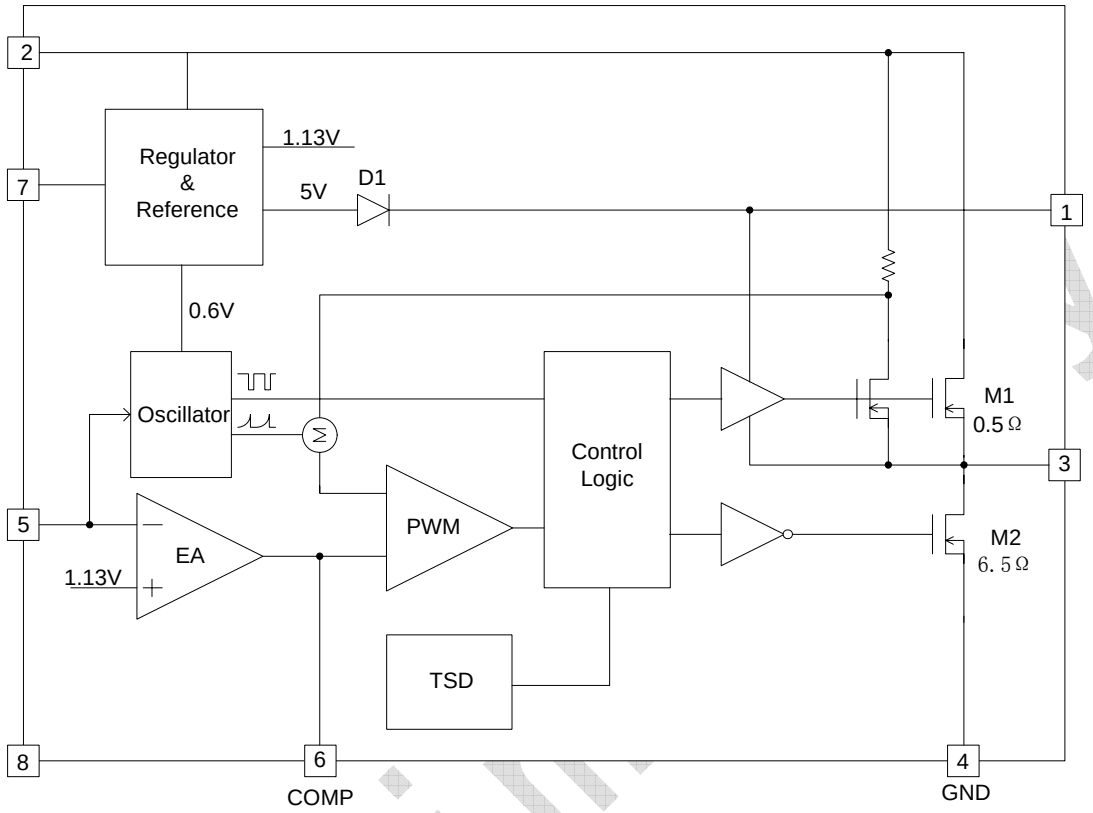


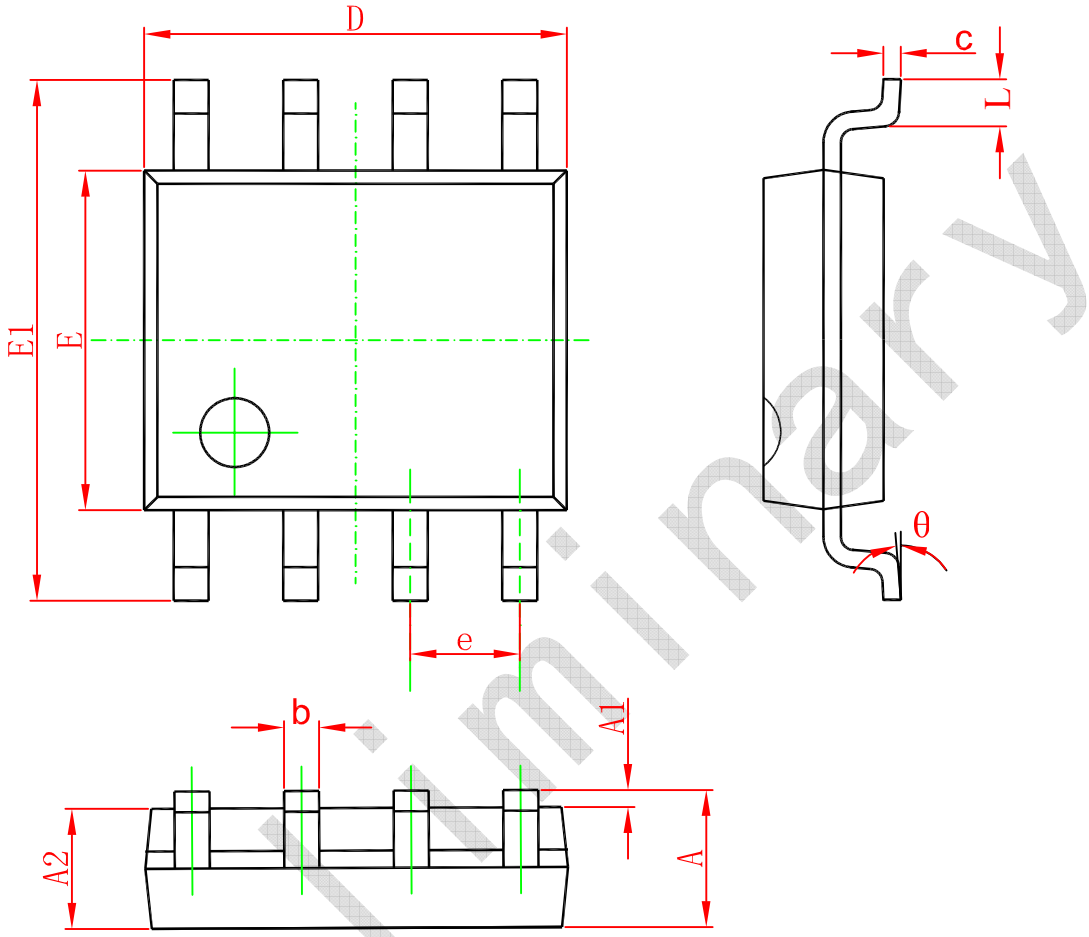
Figure 2

OPERATION DESCRIPTION

The PT1109 is a current mode regulator. That is, the COMP pin voltage is proportional to the peak inductor current. At the beginning of a cycle: the upper transistor M1 is off; the lower transistor M2 is on (refer to Figure 2); the COMP pin voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 380 KHz CLK signal sets a RS Flip-Flop. Its output turns off M2 and turns on M1 thus connecting the SW pin and inductor to the input supply. The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the Current Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the COMP pin voltage, the RS Flip-Flop is reset and the PT1109 reverts to its initial M1 off, M2 on state. If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop. The output of the Error Amplifier integrates the voltage difference between the feedback and the 1.130V bandgap reference. The polarity is such that the FB pin voltage lower than 1.130V increases the COMP pin voltage. Since the COMP pin voltage is proportional to the peak inductor current an increase in its voltage increases current delivered to the output. The lower 6.5Ω switch ensures that the bootstrap capacitor voltage is charged during light load conditions. External Schottky Diode D1 carries the inductor current when M1 is off (see Figure 2)

PACKAGE INFORMATION

SOP-8



SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCH	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°