DESCRIPTION

The PT12465A is a stepping motor driver, the H-bridges output current controlled by PWM constant-current topology. Built-in micro-step sequencer could generate sinusoidal output current to the stepping motor by a single clock input.

The PT12465A support multiple excitation modes such as 2-phase, 1-2-phase, W1-2-phase and 2W1-2 phase mode. The motor rotation revs determinate by the clock frequency applies on CK pin and excitation mode, the CW/CCW pin logic level determinate bipolar stepping motor in forward or reverse direction.

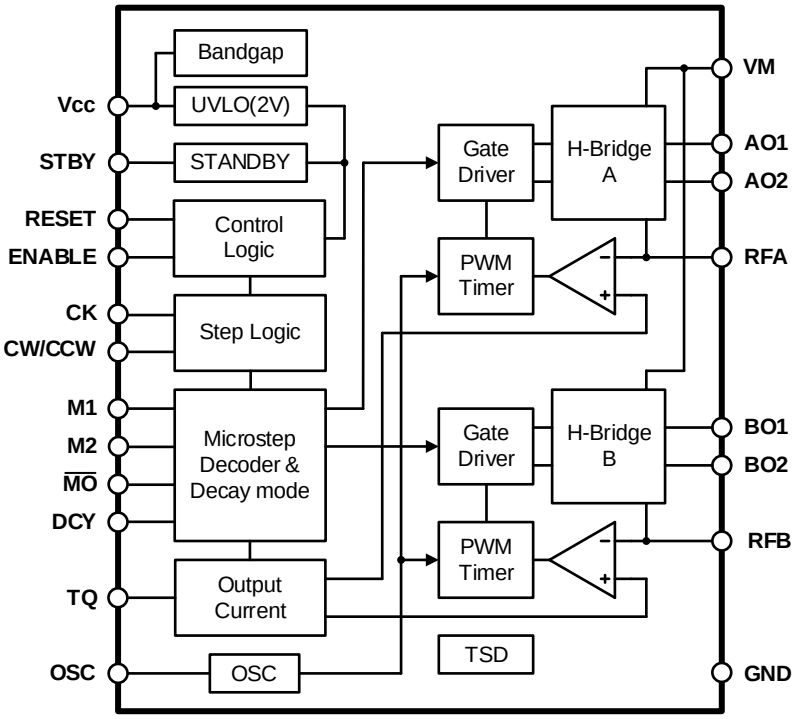
APPLICATIONS

- Camera lens
- Camera peripheral devices
- Low power stepping motors
- HUD reflector

FEATURES

- AEC-Q100 Grade 2 qualified, operation temperature range -40°C~105°C
- Motor power supply voltage range:
  - Control (V_{CC}): 2.7V to 5.5V
  - Motor (VM): 2.5V to 16V
- Maximum output current: 0.8 A
- H-bridge switches on-resistance: Ron = 1.5Ω (high side + low side, VM=7 V)
- Built-in microstep sequencer ticking by CK clock signal
- Programmable phase current excitation modes (2 phase, 1-2 phase, W1-2 phase and 2W1-2 phase)
- Control input pins with internal pull-down resistors
- Motor step monitor output ($\overline{MO}$)
- Thermal shutdown (TSD) protection
- V_{CC} under voltage lock-out (UVLO) function
- 20 pins, thin small surface-mount package (TSSOP-20 173mil, 0.65 mm lead pitch)

BLOCK DIAGRAM



APPLICATION CIRCUIT

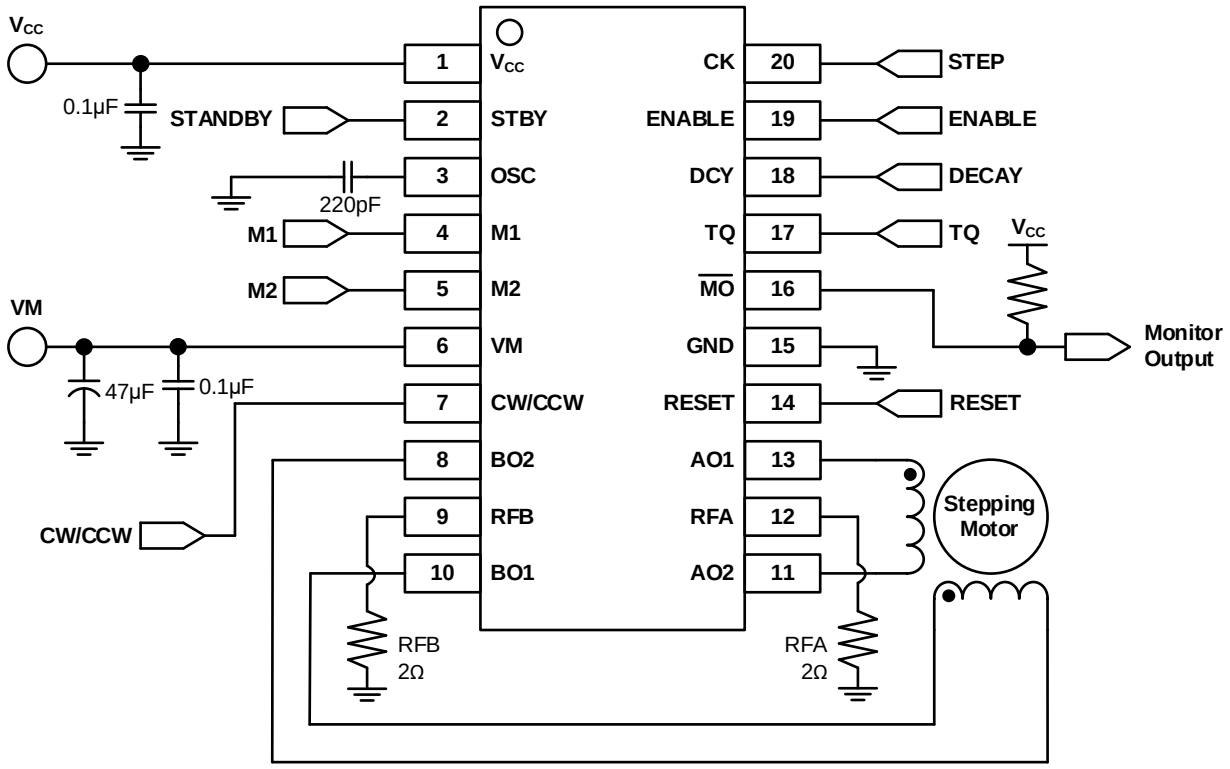


Figure 1, typical application circuit of the PT12465A

APPLICATION NOTE:

1. The bypass capacitors must be placed in between the power input and GND as close as possible.
2. The power rating of the RFA and RFB depends on output current setting, in this application a 0.25W, 0805 (imperial size) was recommended.

SPECIAL NOTICE FOR H-BRIDGE DRIVER OUTPUT

This device does not equip over current protection in the H bridge driver, if the outputs (AO1, AO2, BO1, BO2) has short-circuit event, includes both output of same H bridge shorted, tight to VM, V_{CC} or GND, or both H-bridge connected together, a large current might flow through the IC and causes permanently damage.

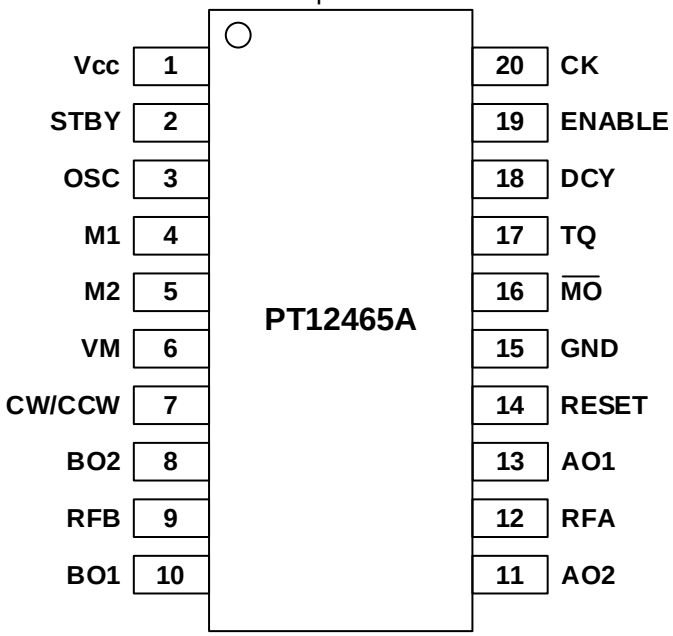
User must consider the PCB layout arrangement to avoid adjacent pin short circuit, or supplies the VM power by a regulator with overcurrent protection.

ORDER INFORMATION

Part Number	Package Type	Top Code
PT12465A-TX	20-PIN, TSSOP, 173MIL	PT12465A-TX

PIN CONFIGURATION

Top View



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	V_{CC}	Power	Power supply pin for logic block
2	STBY	I	Standby input
3	OSC	I	Setting the internal oscillator frequency, connect a capacitor to GND
4	M1	I	Excitation mode setting input 1
5	M2	I	Excitation mode setting input 2
6	VM	Power	Power supply input for H-bridge drivers
7	CW/CCW	I	Motor rotation direction selection
8	BO2	O	B-phase output 2, connect to motor coil
9	RFB	O	B-phase H-bridge current sensing, connector a sense resistor to power GND
10	BO1	O	B-phase output 1, connect to a motor coil
11	AO2	O	A-phase output 2, connect to a motor coil
12	RFA	O	A-phase H-bridge current sensing, connector a sense resistor to power GND
13	AO1	O	A-phase output 1, connect to a motor coil
14	RESET	I	Reset
15	GND	Power	Ground
16	$\overline{MO}$	O	Monitor output (open drain), pulled up by an external resistor Initial state: $\overline{MO}$ = L
17	TQ	I	PWM chopper output current setting (Torque)
18	DCY	I	Decay mode setting
19	ENABLE	I	Enable
20	CK	I	Step clock input

FUNCTION DESCRIPTION

SYSTEM BLOCK OVERVIEW

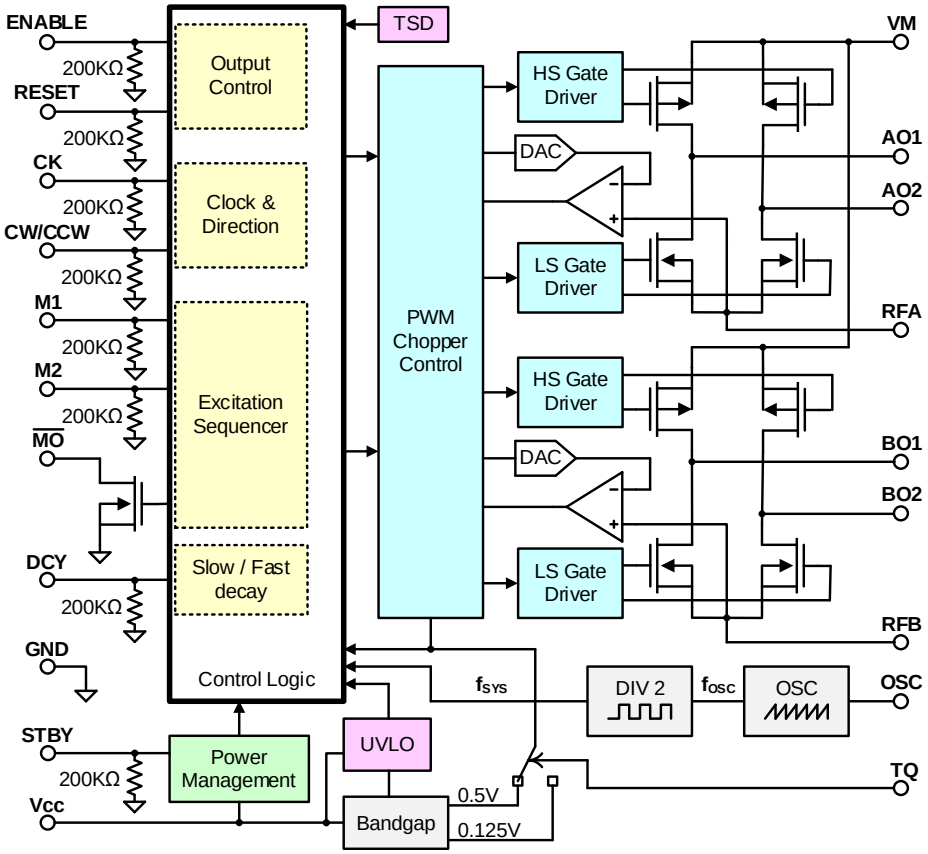


Figure 2, block diagram

RECOMMEND POWER SEQUENCE

The PT12465A does not need special power on-off sequence either Vcc or VM powered in prior to another one. The under voltage locked out (UVLO) circuit inside the Vcc circuit will turn off the H bridge output when the Vcc voltage less than 2V.

Figure 3 shows a recommend power sequence. In power on period (t1), held the STBY and RESET in low state until the Vcc and VM are stabilized (t2) and release them in t3. For power off period, pull the STBY to low state (t4) before supplies voltage removed (t5).

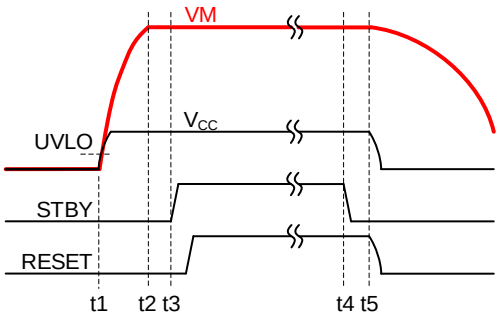


Figure 3, recommend power sequence

SYSTEM CLOCK

The clock oscillator (f_{OSC}) frequency determinate by external capacitance (C_{OSC}) connected on OSC pin, and can be calculated as follows: (for quick refence only, no tolerance guarantee)

$$\text{fosc} = \frac{I}{\Delta V_{osc} \times C_{osc}} = \frac{200uA}{1V \times C_{osc}}$$

The system clock (f_{SYS}) for the PWM chopper is derive from the f_{OSC} and divide by 2.

$$\text{fsys} = \text{fosc}/2$$