DESCRIPTION

The PT12469 is a monolith integrated motor driver designed for printers, scanners, and home and office automated equipment. The two H-bridge drivers can drive a bipolar stepper motor or two DC motors. The output H-bridge driver is consists by all of N-channel MOSFET. The PT12469 is allows driving up to 1.6A maximum output current (VM=24 V, Ta=25°C).

An EN-PH type parallel logic control interface can be configuring the output switches ON-OFF of H-bridge, and motor current decay mode is also programming by the parallel input port.

The PT12469 is available in a 28-pin HTSSOP package with thermal pad and in a 28-pin QFN package thermal pad.

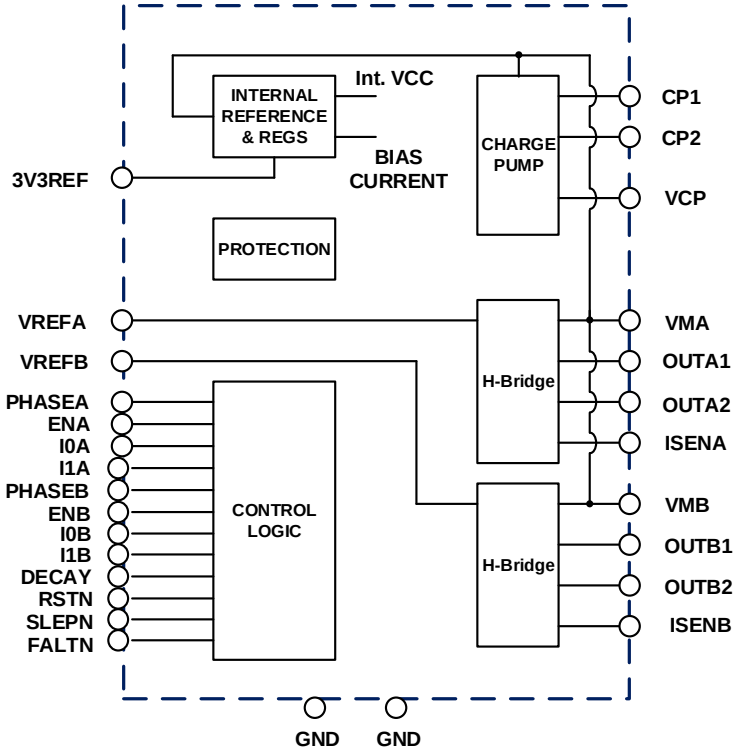
APPLICATIONS

- Automatic Teller Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Amusement Machines
- Factory Automation
- Robotics

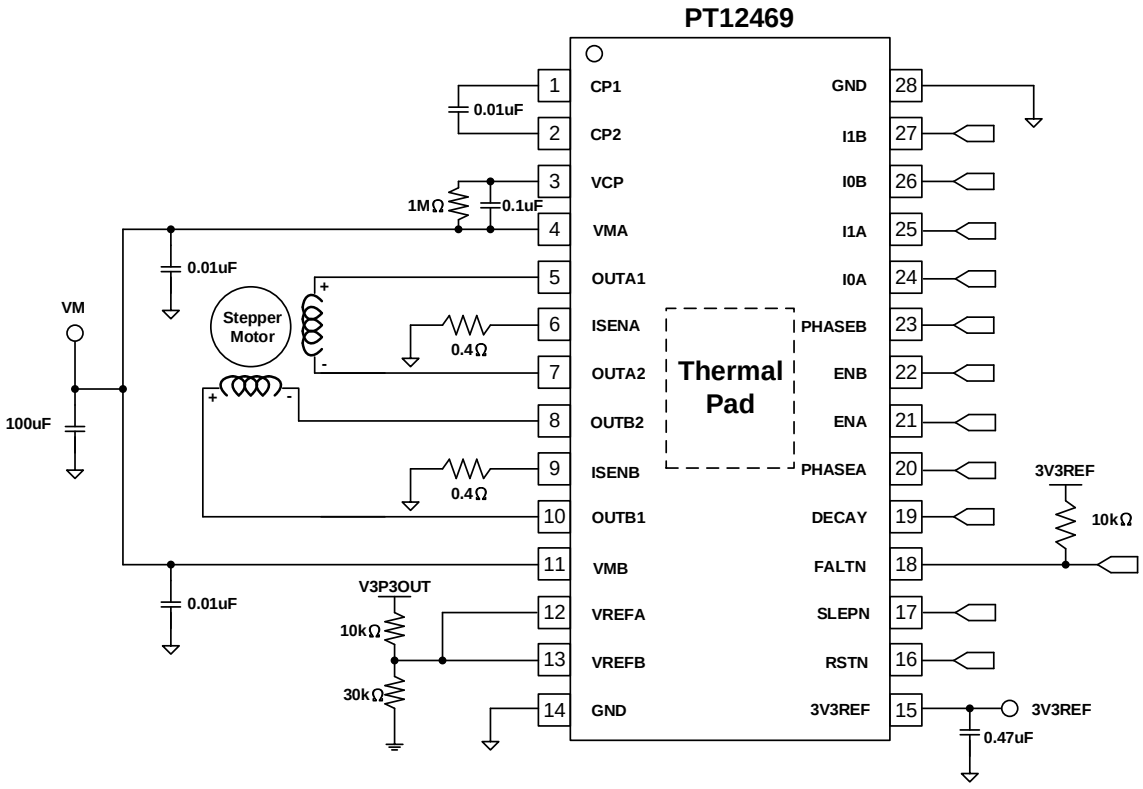
FEATURES

- Automotive AEC-Q100 Grade 1 (-40℃~+125℃) Qualified.
- 8.2-V to 40-V Supply Voltage Range
- 1.6-A Maximum Driving Current at VM=24V (with additional heatsink)
- EN-PH Control Logic Interface
- Dual H-Bridge Driver with 4 Level PWM Current Control.
- Winding Current Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Drives Single Bipolar Stepping Motor or Dual DC Motors
- Built In a 3.3V Reference Voltage Output
- Low-Power Sleep Mode
- Protection Features
  - Over Current Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Under Voltage Lock Out (UVLO)
  - Fault Indication Pin (FAULTN)

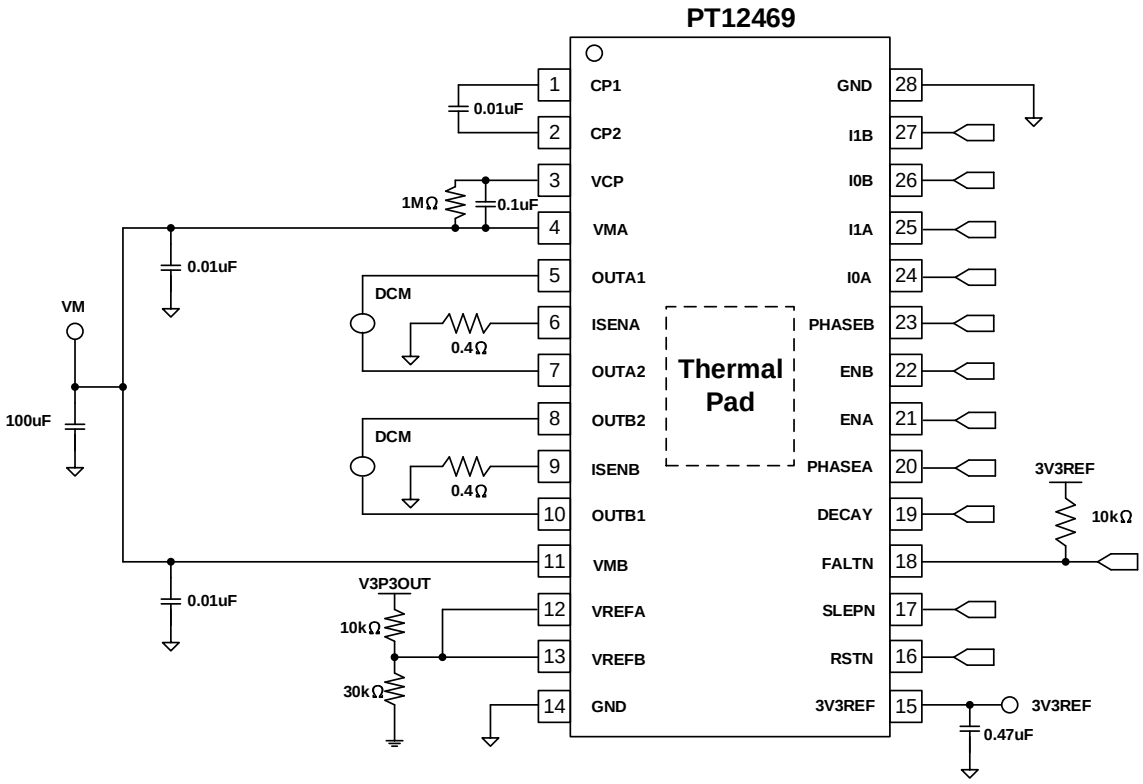
BLOCK DIAGRAM



APPLICATION CIRCUIT



Drives a bipolar stepping motor



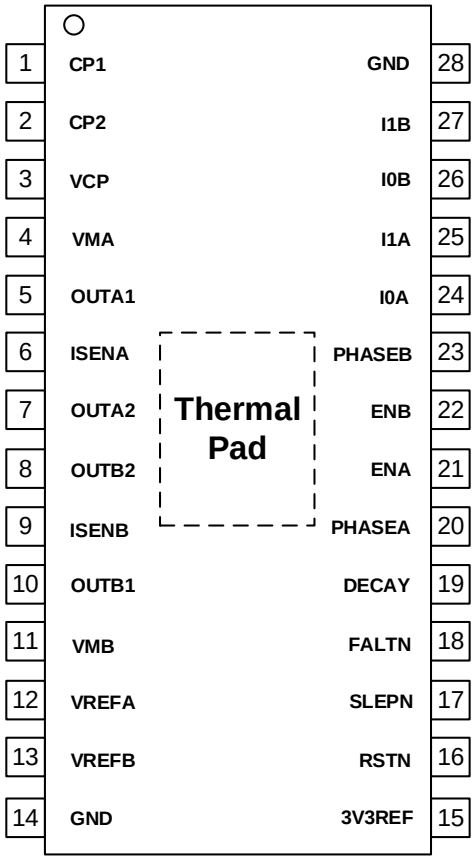
Drives two DC brushed motor

ORDER INFORMATION

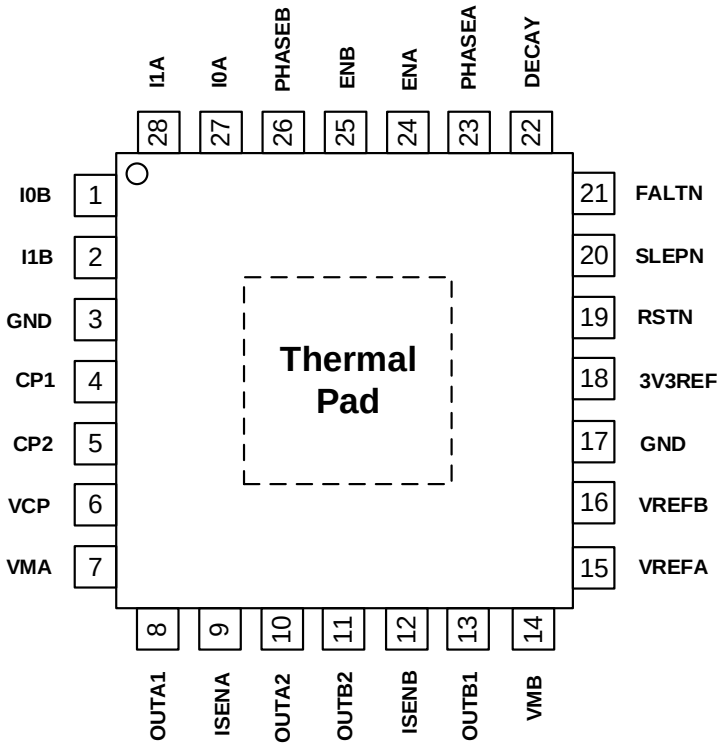
Valid Part Number	Package Type	Top Code
PT12469-HT	28 Pins, HTSSOP	PT12469-HT
PT12469	28 Pins, QFN	PT12469

PIN CONFIGURATION

HTSSOP



QFN



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			HTTSSOP	QFN
CP1	I	External flying capacitor for charge pump, Connect a 0.01μF/50V low-ESR ceramic capacitor between CP1 and CP2.	1	4
CP2	I		2	5
VCP	O	High-side gate drive supply voltage (Connect a 0.1μF/50V ceramic capacitor and a 1MΩ resistor to VM.)	3	6
VMA	-	H-Bridge A power supply	4	7
OUTA1	O	H-Bridge A output 1	5	8
ISENA	I	H-Bridge A current sense / GND	6	9
OUTA2	O	H-Bridge A output 2	7	10
OUTB2	O	H-Bridge B output 2	8	11
ISENB	I	H-Bridge B current sense / GND	9	12
OUTB1	O	H-Bridge B output 1	10	13
VMB	-	H-Bridge B power supply	11	14
VREFA	I	H-Bridge A current set reference input	12	15
VREFB	I	H-Bridge B current set reference input	13	16
GND	-	Device ground	14	17
3V3REF	O	3.3V reference voltage output	15	18
RSTN	I	Reset input (L=Initialize all of internal logic registers and disables H-bridge outputs)	16	19
SLEPN	I	Sleep mode input (H=device enable, L=low-power sleep mode)	17	20
FALTN	O	Fault, Logic low when fault condition appear (OCP, OTP)	18	21
DECAY	I	Decay mode (Low = slow decay, open = mixed decay, high = fast	19	22
PHASEA	I	H-Bridge A phase (H=AOUT1 high, AOUT2 low)	20	23
ENA	I	H-Bridge A enable (H=H-bridge A output active)	21	24
ENB	I	H-Bridge B enable (H=H-bridge B output active)	22	25
PHASEB	I	H-Bridge B phase (H=BOUT1 high, BOUT2 low)	23	26
I0A	I	H-Bridge A current set (Sets H-bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0%)	24	27
I1A	I		25	28
I0B	I	H-Bridge B current set (Sets H-bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0%)	26	1
I1B	I		27	2
GND	-	Device ground	28	3

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
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