DESCRIPTION

The PT12493 is an integrated multi-channel half-bridge drivers with 8 half-bridges. The device features low on- state resistance ($R_{DS(ON)}$) for improved thermal performance during high-current operation. This device can drive brushed-DC (BDC) motors or stepper motors in independent, sequential, or parallel mode. The half-bridges are fully controllable to achieve a forward, reverse, coasting and braking operation of motor.

This device feature standard 16-bit, 5-MHz serial peripheral interface (SPI) with daisy chain capability for complete configuration and detailed diagnostics. The device has eight programmable PWM generators are integrated to allow for current limiting during motor operation or LED dimming control.

The device includes numerous protection and diagnostic features including an FALTN pin to alert the system when a fault occurs. The device features a low-current open load detection (OLD) mode to detect open-load conditions when the nominal load current is small and a passive OLD mode for offline OLD. The device is also fully-protected from short-circuit, under-voltage, and over-temperature conditions.

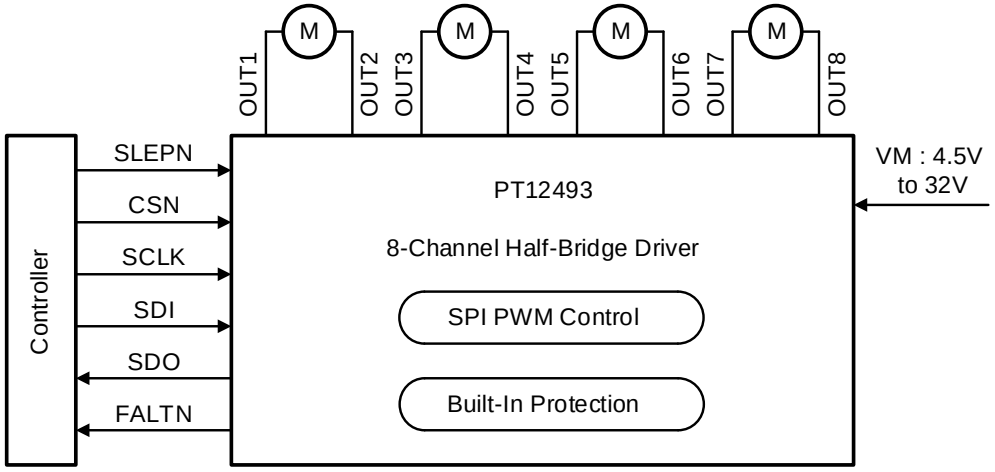
APPLICATIONS

- HVAC flap DC motors
- Side mirror adjustment and mirror fold
- LED applications
- Multiple brushed DC motors and solenoids

FEATURES

- AEC-Q100 qualified for automotive applications
- 8 half-bridge outputs
- 4.5-V to 32-V operating voltage
  - 40-V absolute maximum voltage
- 1-A RMS current for each output
  - 6-A maximum current for paralleled outputs
- Low-power sleep mode (1.5-µA)
- Supports 3.3-V and 5-V logic inputs
- SPI for configuration and diagnostics
  - 5-MHz, 16-Bit SPI communication
  - Daisy chain functionality
- PWM generators programmable over SPI
  - Individual half-bridge PWM operation
  - Configurable for high-side, low-side, and H-bridge load driving
  - Supports 8-bit duty cycle resolution
- Integrated protection features with per channel detailed diagnostics over SPI
  - FALTN pin output
  - VM undervoltage lockout (UVLO)
  - VM overvoltage protection (OVP)
  - Logic supply power on reset (POR)
  - Overcurrent protection (OCP)
  - Enhanced open load detection (OLD)
  - Thermal warning and shutdown (OTW/OTSD)
- HTSSOP 24 pins package with exposed thermal pad

TYPICAL APPLICATION



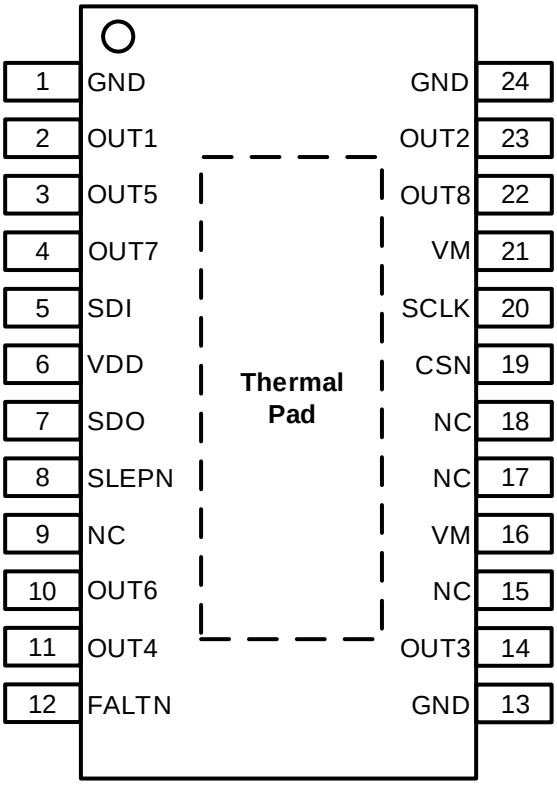
CONTENT

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT12493	24 Pins, HTSSOP	PT12493-HT

PIN CONFIGURATION

PT12493, HTSSOP 24-Pin
Top View



PIN DESCRIPTION

PIN Name	I/O	Description	PIN NO.
GND	PWR	Device power ground. Connect the GND pin to the system ground.	1
OUT1	O	Half-bridge 1 output	2
OUT5	O	Half-bridge 5 output	3
OUT7	O	Half-bridge 7 output	4
SDI	I	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pull-down.	5
VDD	PWR	Logic power supply input. Connect a X5R or X7R, 0.1-μF, VDD-rated ceramic capacitor and greater than or equal to 1-μF bulk capacitance between the VDD and GND pins.	6
SDO	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin.	7
SLEPN	I	Driver enable pin. When this pin is logic low the device goes to a low-power sleep mode. Internal pull-down.	8
NC	—	Not connected	9
OUT6	O	Half-bridge 6 output	10
OUT4	O	Half-bridge 4 output	11
FALTN	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.	12
GND	PWR	Device power ground. Connect the GND pin to the system ground.	13