PT1302

High Efficiency Step-up DC/DC Converter

GENERAL DESCRIPTION

The PT1302 is a compact, high efficiency, and low voltage step-up DC/DC converter with an Adaptive Current Mode PWM control loop. It comprises of an error amplifier, a ramp generator, a PWM comparator, a switch pass element and driver. It provides stable and high efficient operation over a wide range of load currents. It operates in stable wave forms without external compensation. It is suitable for 1~4 battery cells applications to provide up to 800mA output current. The 500KHz high switching rate reduces the size of external components. Besides, the 25 µA low quiescent current together with high efficiency maintains long battery lifetime. The output voltage is set with two external resistors. Both internal 2A switch and 300mA driver for driving external power devices (NMOS or NPN) are provided.

FEATURES

- Low Quiescent (Switch-off) Supply Current: 25µA
- High Supply Capability: Deliver 5V 800mA with lithium cell/ 3.3V 800mA with 2Alkaline Cell
- Zero Shutdown Mode Supply Current
- High efficiency: 92%
- Fixed switching frequency: 500KHz
- Options for internal or external power switches
- MSOP-8 and SOT-89-5 packages are available

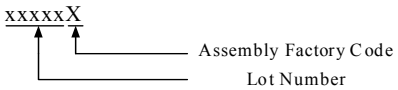
APPLICATION

- LCD Displays
- Handheld Computers and PDAs
- Portable instruments
- Wireless equipment
- Digital Still and Video Cameras

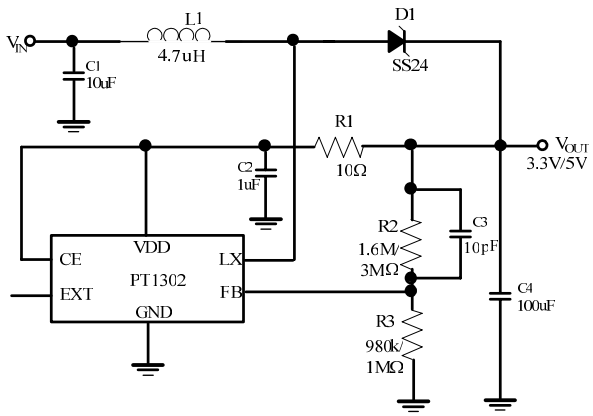
ORDERING INFORMATION

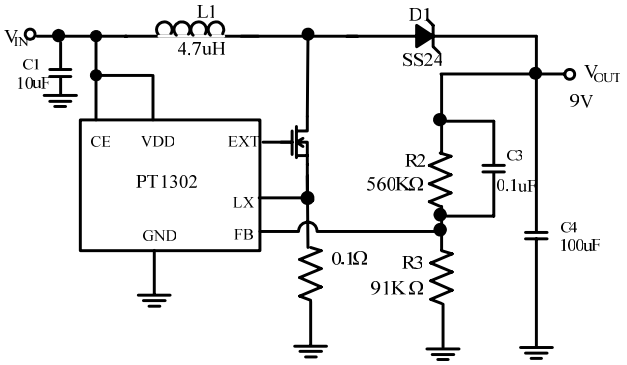
PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
MSOP-8	-40 °C to 85 °C	PT1302EMSH	Tape and Reel 3000 units	PT1302 xxxxxX
SOT-89-5	-40 °C to 85 °C	PT1302E89E	Tape and Reel 1000 units	PT1302 xxxxxX

Note:

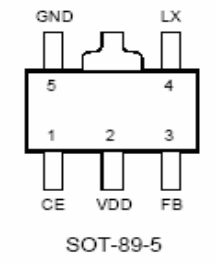


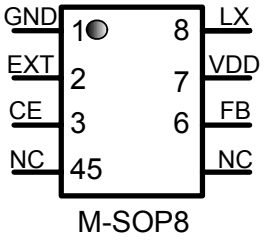
TYPICAL APPLICATION CIRCUIT





PIN ASSIGNMENT





PIN DESCRIPTIONS

Pin No.		PIN NAMES	DESCRIPTION
MSOP-8	SOT-89-5		
1 5		GND	Ground
2		EXT	Output pin for driving external power switch
3 1		CE	Chip en able, PT1302 gets in to shu tdown m ode when CE pin is set to low
4		NC	Not Connected
5		NC	Not Connected
6 3		FB	Feedback input pin
7 2		VDD	Power Supply Pin
8 4		LX	Output of internal power switch

ABSOLUTE MAXIMUM RATINGS (Note 1)

SYMBOL	ITEMS	VALUE	UNIT
V_{DD} Su	pply Voltage	-0.3~7.0	V
V_{LX} LX	Pin Switch Voltage	-0.3~7.0	V
V_{IO}	Voltage on other I/O Pins	-0.3 to (VDD+0.3)	V
I_{OUT}	LX Pin Output Current	2.5 A	
I_{EXT}	EXT Pin Drive Current	300 m	A
P_{TR1}	Package Thermal Resistance, MSOP-8 θ_{JA}	190	°C /W
P_{TR2}	Package The rmal Resistance, SOT -89-5 θ_{JA}	100	°C /W
T_{STG} S	torage Temperature	-65 to 150	°C
T_{Solder}	Lead temperature (Soldering)	260℃, 10s	

RECOMMENDED OPERATING RANGE

SYMBOL	ITEMS	VALUE	UNIT
V_{DD}	V_{DD} Supply Voltage	+2.0 ~ +6.0	V
T_{OPT}	Operating Temperature Range	-40 to +85	°C
	ESD Susceptibility (Note 2)	3	kV

Note 1: Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS (VDD=3.3V) (Note 3, 4)

The following specifications apply for V_{IN}=3.6V, I_{Load} =0 and T_A=25 °C, unless otherwise specified.

SYMBOL	ITEMS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{ST} Start-UP	Voltage	I_{Load} = 1.5mA	1.5		--	V
V_{DD} Ope	rating VDD Range	V_{DD} pin voltage	2 -- 6			V
I_{OFF}	Shutdown Current I(V_{DD})	CE Pin= 0V, V_{IN} = 4.5V	--	0.01	1	µA
$I_{SWITCH\ OFF}$ Switch-off	Current I(V_{DD}) V	$_{IN}$ = 6V	--	25	50	µA
I_{SWITCH}	Continuous Switching Current	V_{IN}=V_{CE}=3.3V, V_{FB}= GND	0.4 0.	55 0.	7 m	A
$I_{NO\ LOAD}$	No Load Current I(V_{DD}) V	$_{IN}$= 1.5V, V_{OUT}= 3.3V	--	75	--	µA
V_{FB}	Feedback Reference Voltage	Closed Loop	1.225	1.25	1.275	V
F_S	Switching Frequency		425 50	0 57	5	kHz
D_{MAX} M	aximum Duty		85	94	--	%
	LX ON Resistance to V_{DD}		--	0.1	0.3	Ω
I_{LIMIT}	Current Limit Setting		--	2	--	A
	EXT ON Resistance to V_{DD}		1.	5		Ω
	EXT ON Resistance to GND		1.	0		Ω
ΔV_{LINE}	Line Regulation	V_{IN} = 1.5 ~ 2.8 V, I_{Load} = 1.5mA	-- 1.	5		mV/V
ΔV_{LOAD}	Load Regulation	V_{IN} = 2.5V, I_{Load} = 1.5 ~ 1200mA	-- 0.	1	--	mV/ mA

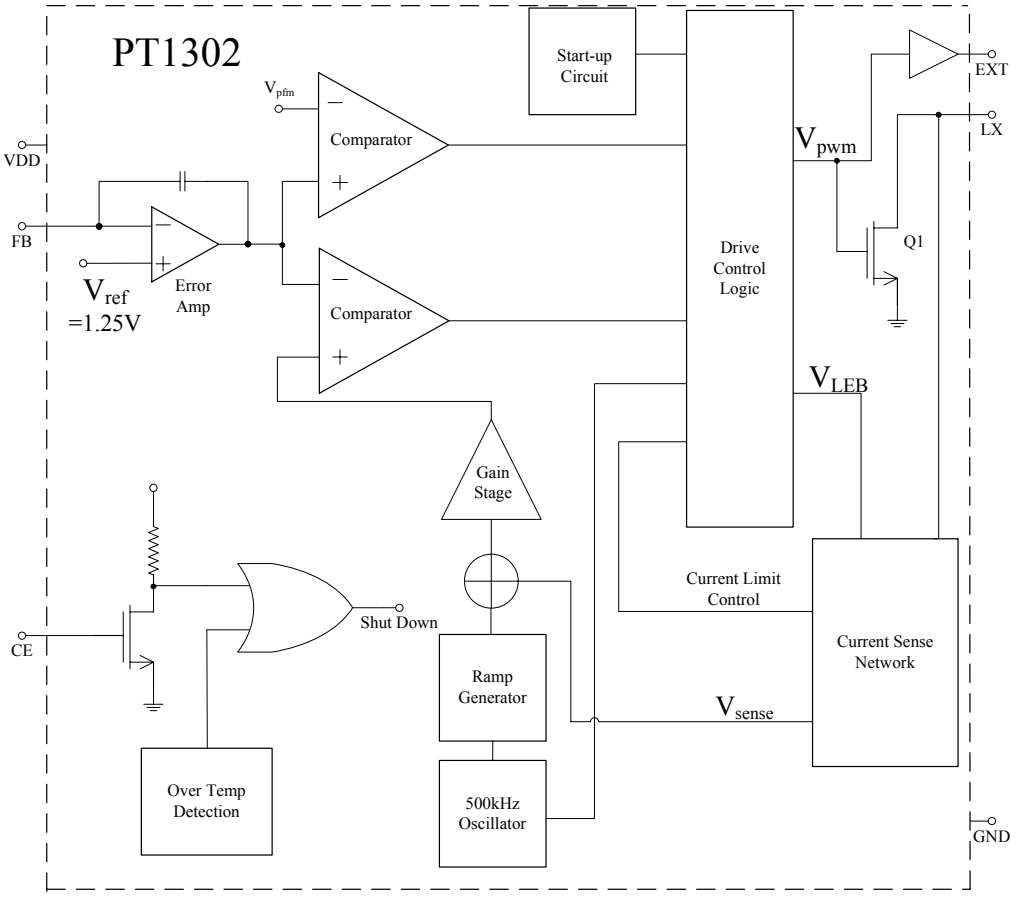
ELECTRICAL CHARACTERISTICS (VDD=3.3V) (Note 3, 4) **(Continued)**

SYMBOL	ITEMS	CONDITIONS	MIN.	TYP.	MAX.	UNIT
	CE Pin Trip Level		0.4	0.8	1.2	V
TS	Temperature Stab ility for VOUT	--		125	--	ppm/℃
ΔTSD	Thermal Shutdown Hysteresis		--	10	--	℃

Note 3: Typical parameters are measured at 25˚C and represent the parametric norm.

Note 4: Datasheet specifications with min/max limits are guaranteed by design, test, or statistical analysis.

SIMPLIFIED BLOCK DIAGRAM

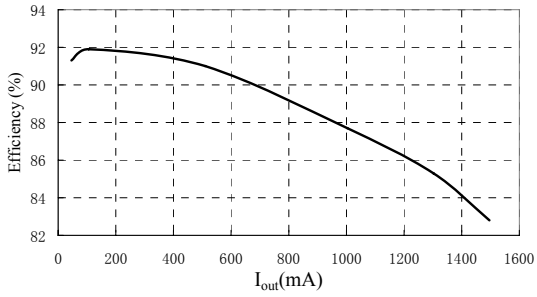


OPERATION DESCRIPTION

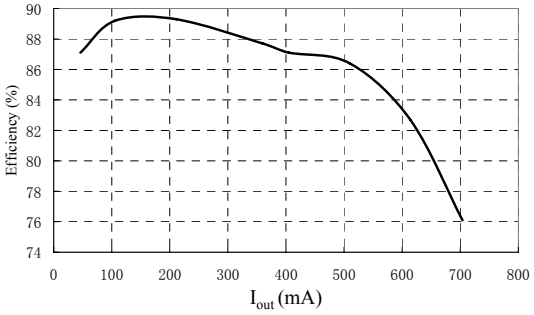
The PT1302 structure is a step-up DC/DC converter. When connected according to Typical Application Circuit, a boost voltage regulator is formed, which produces a required output DC voltage higher than the input voltage. The output voltage is regulated by controlling the Q1 on time t_{on} in a negative-feedback loop. If DC load current increases, the on ti me i s autom atically i ncreased to deli ver t he greater re quired e nergy to the load. I f V_{in} decreases, and if t_{on} were not changed, the peak current and hence also the energy stored in L 1 would decrease and the DC output voltage would decrease. But the negative-feedback loop senses a slightly decreased output voltage and increases t_{on} to maintain output voltage constant.

TYPICAL PERFORMANCE CHARACTERISTICS

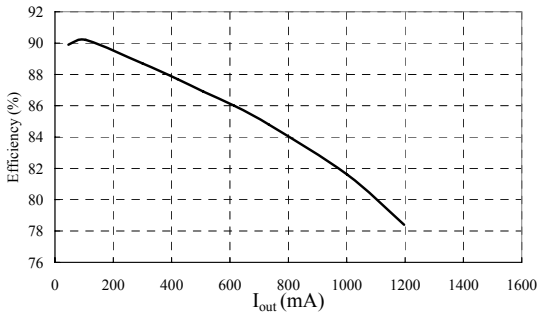
Efficiency @Vin=4.5V Vout=5V



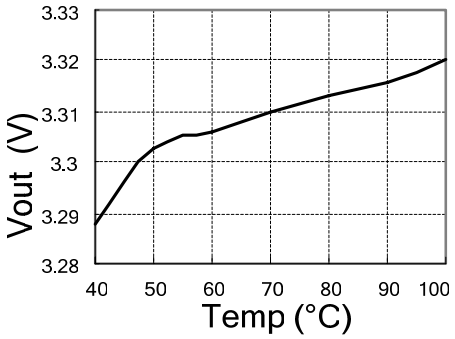
Efficiency@Vin=3V Vout=5V



Efficiency @Vin=3V Vout=3.3V

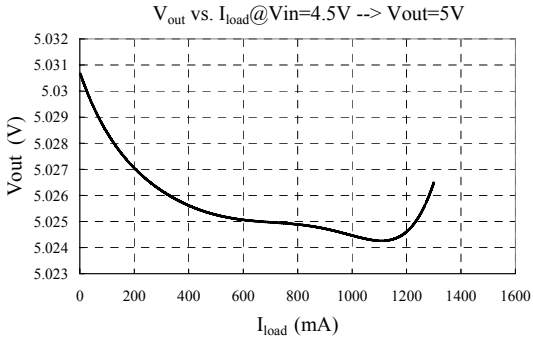


V_{out} vs. Temperature



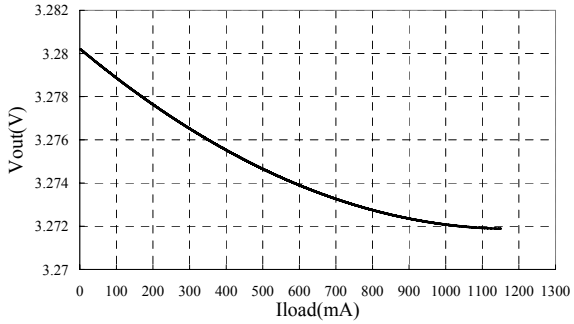
Load Regulation

V_{out} vs. I_{load}@Vin=4.5V --> Vout=5V

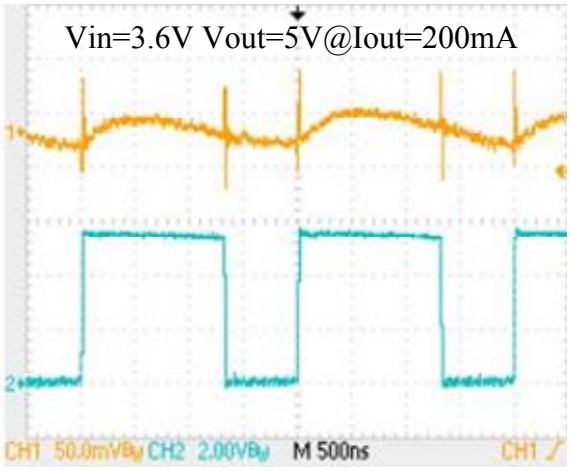


Load Regulation

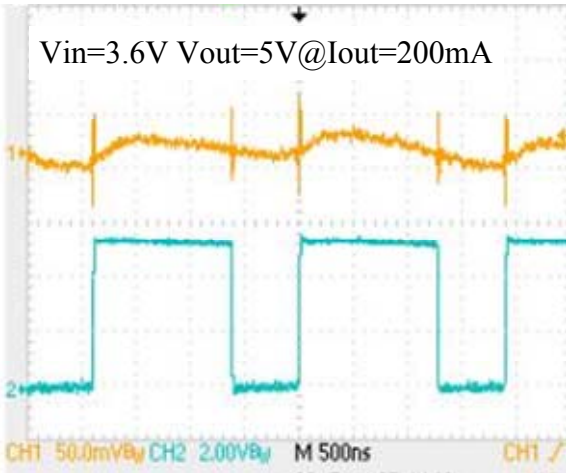
Vout V.S. Iload@Vin=3V ->Vout=3.3V



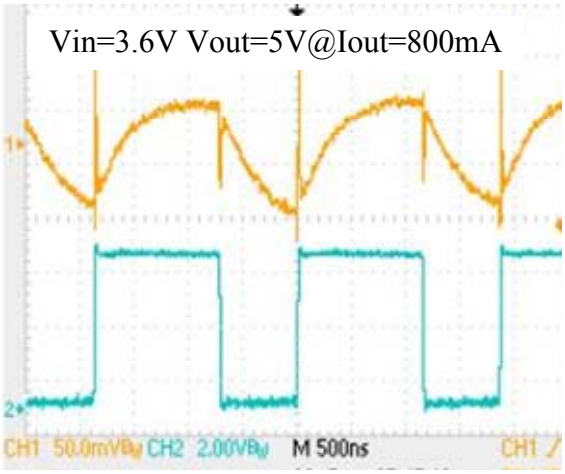
LX & Output Ripple(MSOP8)



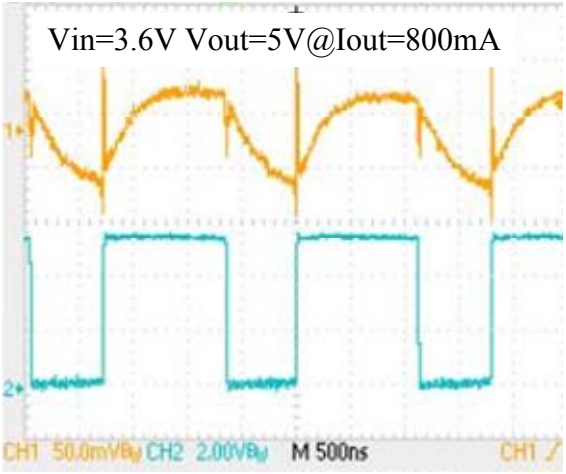
LX & Output Ripple(SOT89-5)



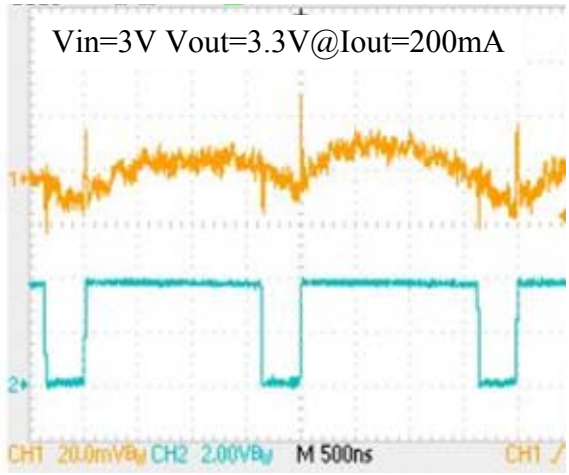
LX & Output Ripple(MSOP8)



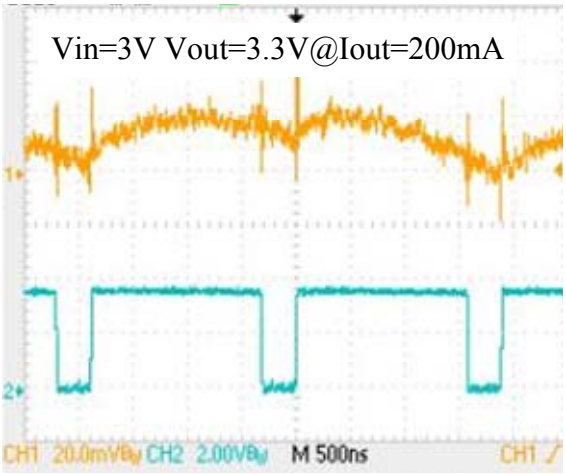
LX & Output Ripple(SOT89-5)



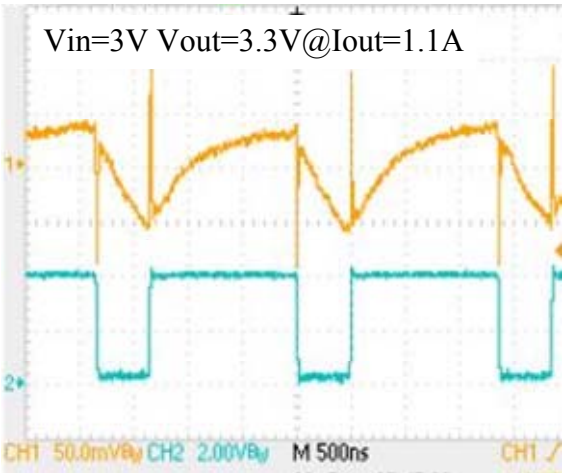
LX & Output Ripple(MSOP8)



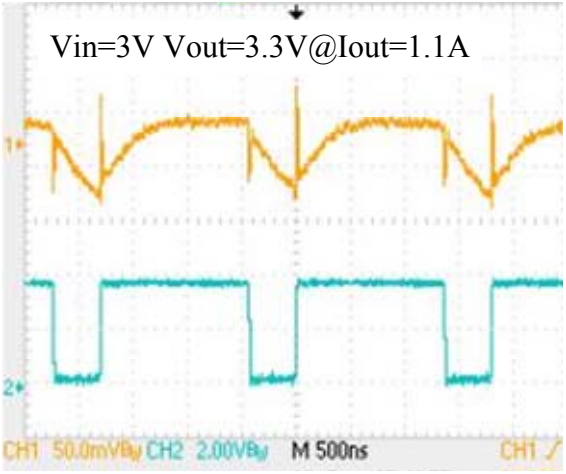
LX & Output Ripple(SOT89-5)



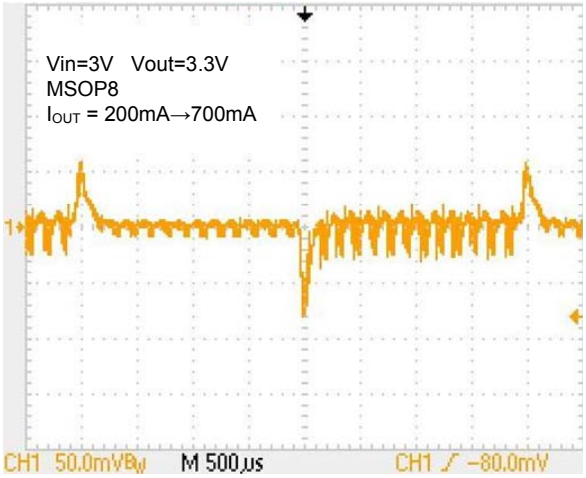
LX & Output Ripple(MSOP8)



LX & Output Ripple(SOT89-5)



Transient



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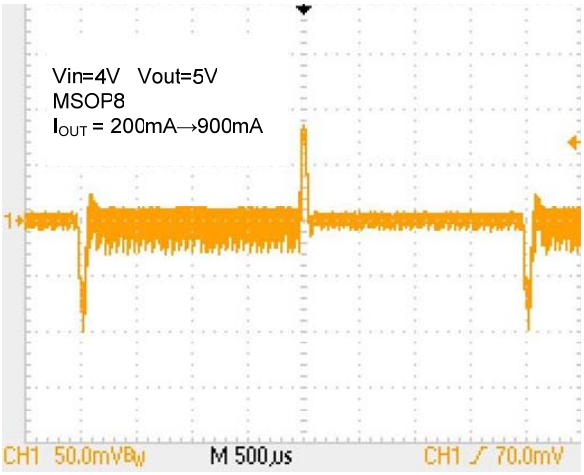

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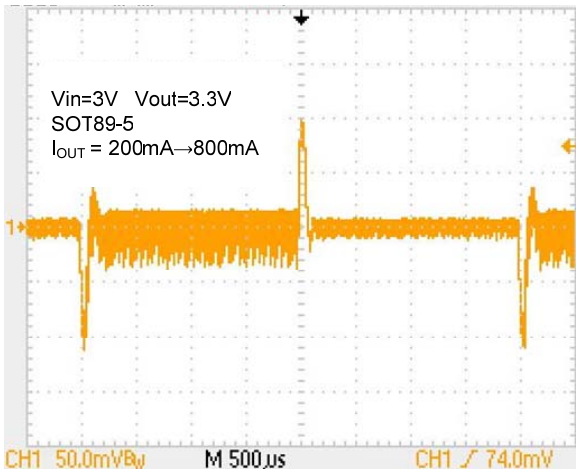

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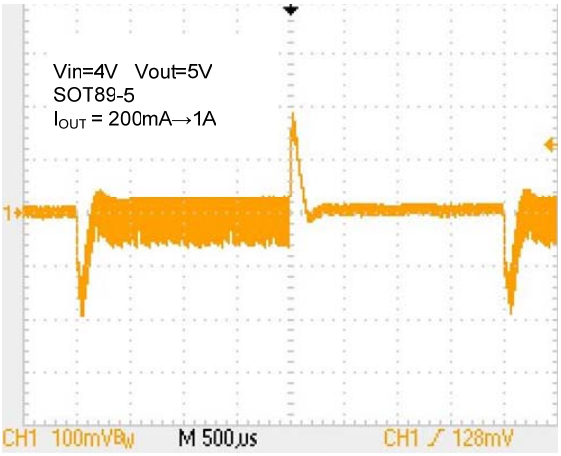


APPLICATION INFORMATION

1) OUTPUT VOLTAGE SETTING

Referring to Typical Application Circuit, the output voltage of switching regulator (V_{out}) is set with following equation:

$V_{out}=(1+R1/R2)*V_{fb}$

2) FEEDBACK LOOP DESIGN

Referring to Typical Application Circuit again, the selection of R1 and R2 is a trade-off between quiescent current consumption and interference immunity besides abiding by the above equation.

- Higher R reduces quiescent current (I=1.25V/R2)
- Lower R gives better interference immunity, and is less sensitive to interference, layout parasitic, FB node leakage, and improper probing to FB pin.

Hence for applications without standby or suspend modes lower R1 and R2 values are preferred, while for applications concerning the current consumption in standby or suspend modes, higher values of R1 and R2 are needed. Such high impedance feedback loop is sensitive to any interference, which requires careful PCB layout and avoid any interference, especially to FB pin.

To improve the system stability, a proper value capacitor between FB pin and Vout is suggested. An empirical suggestion is around 10pF for MΩ feedback resistors and 10nF～0.1uF for lower R values.

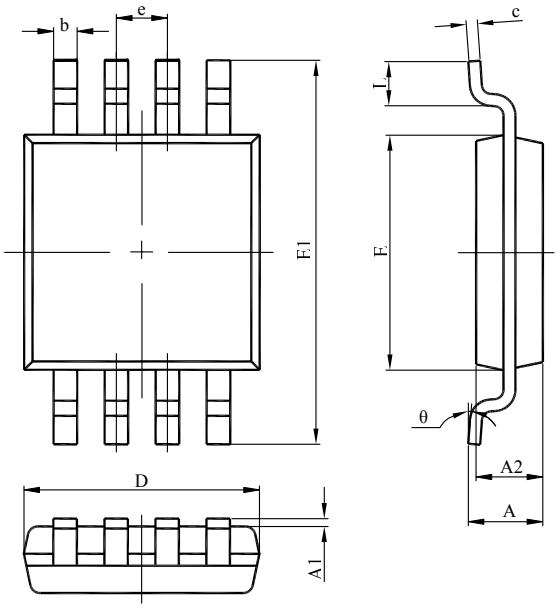
3) PCB Layout Guide

PCB Layout shall follow these guidelines for better system stability:

- A full GND plane without any gap break.
- VDD to GND bypass Cap – The 1 μF MLCC noise bypass Cap between VDD pin (pin 7 for MSOP-8 or pin 2 for SOT-89-5)and GND pin(pin 1 for MSOP-8 or pin 5 for SOT-89-5) shall have short and wide connections.
- V_{in} to GND bypass Cap – Add a Cap close to the inductor when V_{in} is not an ideal voltage source.
- Minimize the FB node copper area and keep it far away from noise sources.
- Minimize the parasitic capacitance connected to LX and EXT nodes to reduce the switch loss.

PACKAGE INFORMATION

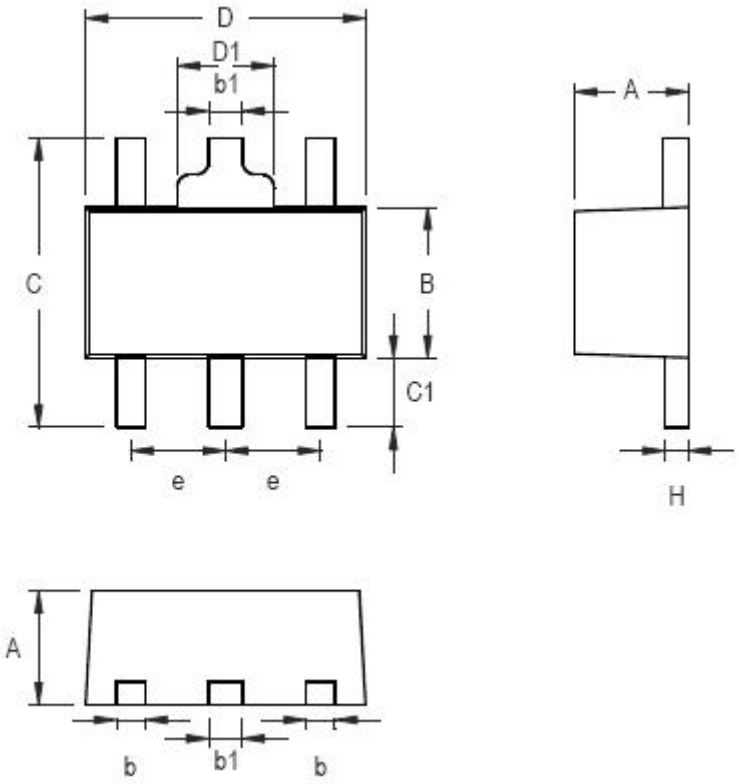
MSOP-8 Package



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A 0.	820	1.100	0.032	0.043
A1 0.	020	0.150	0.001	0.006
A2 0.	750	0.950	0.030	0.037
b 0.	250	0.380	0.010	0.015
c 0.	090	0.230	0.004	0.009
D 2.	900	3.100	0.114	0.122
e 0	.650(BSC)		0.026(BSC)	
E 2.	900	3.100	0.114	0.122
E1 4.	750	5.050	0.187	0.199
L 0.	400	0.800	0.016	0.031
θ 0°		6°	0°	6°

PACKAGE INFORMATION

SOT-89-5 Package



SYMBOL	MILLIMETERS		INCHS	
	MIN	MAX	MIN	MAX
A 1.400		1.600	0.055	0.063
b 0.460		0.520	0.014	0.020
B 2.400		2.600	0.094	0.102
b1 0.406		0.533	0.016	0.021
C		4.250		0.167
C1 0.800			0.031	
D 4.400		4.600	0.173	0.181
D1		1.700		0.067
e 1.400		1.600	0.055	0.063
H 0.380		0.430	0.014	0.017