PT1311

High Efficiency Synchronous Boost DC/DC Converter

GENERAL DESCRIPTION

The PT1311 is a high efficiency synchronous fixed frequency step-up DC/DC converter. The device is available in an adjustable version and fixed output voltages of 3.3V or 5.0V. Supply current during operation is only 25μA and drops to ≤1μA in shutdown. The 0.85V to 4.2V input voltage range makes the PT1311 ideally suited for single Li-Ion battery or single AA battery applications. Automatic Burst Mode operation increases efficiency at light loads, further extending battery life. Switching frequency is internally set at 1.2MHz, allowing the use of small surface mount inductors and capacitors. The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Anti-ringing control circuitry reduces EMI concerns by damping the inductor in DCM mode. The internal short protect circuitry can protect battery when output short to ground. The PT1311 is available in a SOT23-6 package.

FEATURES

- High Efficiency: Up to 93%
- Very Low Quiescent Current: Only 25μA During Operation
- 600mA Output Current
- 0.85V to 4.2V Input Voltage Range
- 1.2MHz Constant Frequency Operation
- No Schottky Diode Required
- Anti-ringing Control Minimizes EMI
- Output Short Protect
- Shutdown Mode Draws≤1μA Supply Current
- Current Mode Operation for Excellent Line and Load Transient Response
- Over temperature Protected
- Feedback Voltage Auto Detect
- SOT23-6 Package

APPLICATIONS

- Li-ion Battery Chargers
- USB Audio Devices
- Wireless Mice
- Digital Still Cameras
- MP3/MP4 Players
- Portable Instruments

TYPICAL APPLICATION DIAGRAM

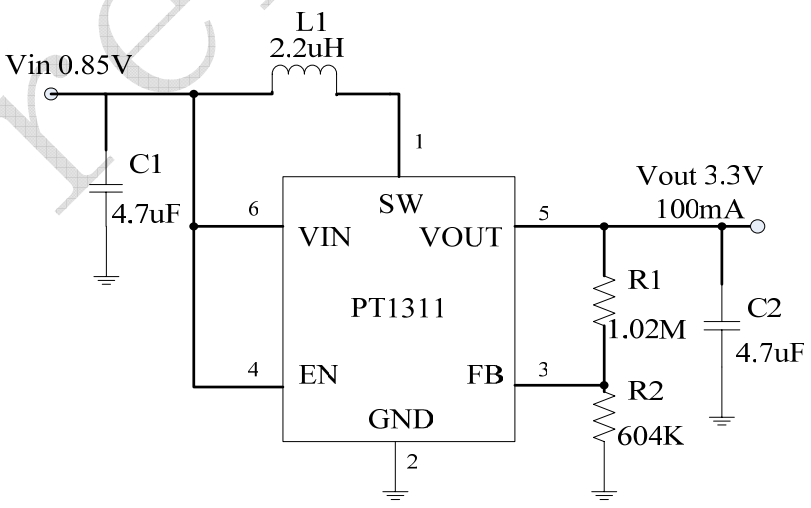
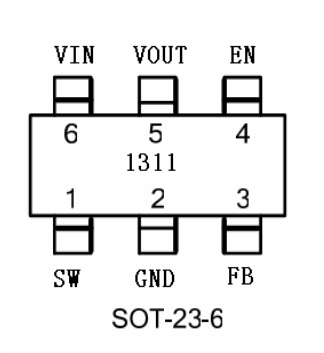


Figure 1. Single Cell to 3.3V Synchronous Boost Converter

PIN ASSIGNMENT



SOT-23-6

PIN DESCRIPTIONS

PIN NUM	PIN NAME	DESCRIPTIONS
1	SW	Output of Internal Switches
2	GND	Chip Ground
3	FB	Regulated Feedback
4	EN	Chip Enable, Active with 'H'
5	VOUT	Output Voltage
6	VIN	Input Voltage

ABSOLUTE MAXIMUM RATINGS (NOTE1)

SYMBOL	ITEM	RATING	UNIT
V_{IN}	Input Voltage	-0.3~7.0V	V
V_{SW}	SW Pin Switch Voltage	-0.3~7.0V	V
V_{OUT}	Output Voltage	-0.3~7.0V	V
V_{FB}	Feedback Voltage	-0.3~7.0V	V
V_{EN}	Enable Voltage	-0.3V to (VIN+0.3V)	V
PTR1	Package Thermal Resistance Θ_{JA}	250	W/℃
T_{OPT}	Operating Temperature Range	-40~85	℃

RECOMMENDED OPERATING RANGE (NOTE2)

SYMBOL	PARAMETER	VALUE
V_{IN}	Input Voltage Range	0.85V-4.2V

Notes:

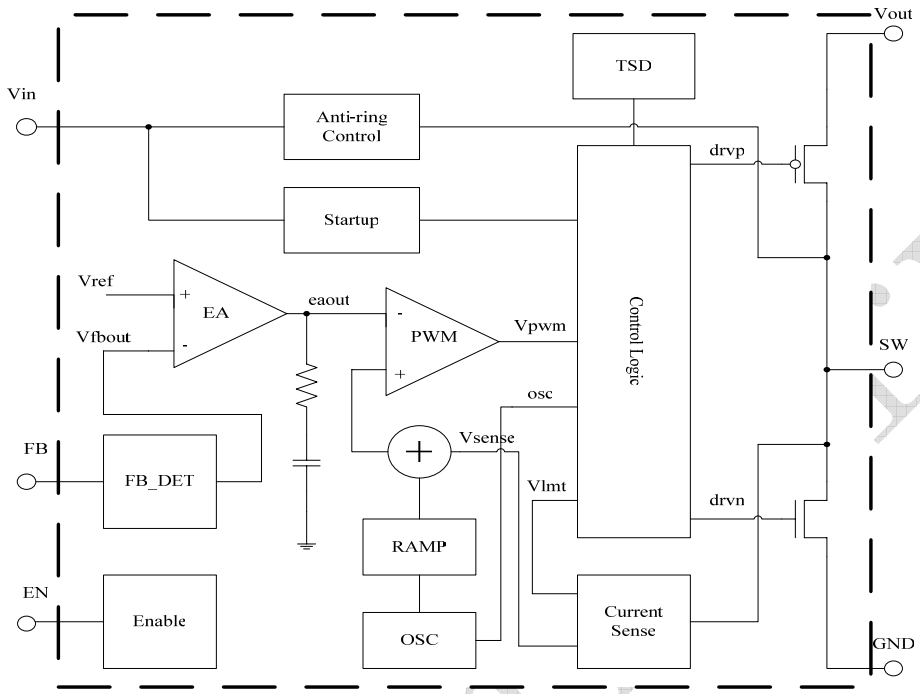
1. Exceeding these ratings may damage the device
2. The device is not guaranteed to function outside of its operating rating

ELECTRICAL CHARACTERISTICS

TA = 25°C. V_{IN} = 1.5V. V_{OUT} = 3.3V unless otherwise specified.

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{ST}	Startup voltage	IL=1mA	--	0.85	1.05	V
V_{DD}	Operation voltage		2	--	6	V
V_{FB}	Feedback voltage	3.3V fixed	3.234	3.3	3.366	V
		Adjusted output	1.225	1.25	1.275	V
$I_{SWITCH\ OFF}$	Switch off current	Iload=0mA	--	25	35	μA
$I_{SHUTDOWNF}$	Shut down current	V_{EN} =0, V_{IN}=1.5V	--	0.01	1	μA
Fs	Frequency		1	1.2	1.4	MHz
D_{MAX}	Max duty cycle		80	90		%
R_{ON_NMOS}	NMOS Resistor	VDD=3.3V	--	0.2	0.35	Ω
		VDD=5V		0.15	0.25	Ω
R_{ON_PMOS}	PMOS Resistor	VDD=3.3V	--	0.4	0.6	Ω
		VDD=5V		0.3	0.5	Ω
I_{LIMIT}	NMOS current limit		1.0	1.5	2.0	A
$\triangle V_{LINE}$	Voltage regulate	V_{IN} = 1 ~ 2.5V,	--	1.5	5	mV/V
$\triangle V_{LOAD}$	Load regulate	V_{IN} = 1.5V, IL = 1 ~ 100mA	--	0.1	--	mV/mA

SIMPLIFIED BLOCK DIAGRAM



APPLICATION INFORMATION

1) Output Voltage Setting

Referring to Typical Application Circuit 1, the output voltage of switching regulator (Vout) is set with following equation:

Vout=(1+R1/R2)*Vfb

FB short with Vout: Vout=3.3V

FB short with Gnd: Vout=5.0V

2) Feedback Loop Design

Referring to Typical Application Circuit 1 again, the selection of R1 and R2 is a trade-off between quiescent current consumption and interference immunity besides abiding by the above equation.

- Higher R reduces quiescent current (I=1.25V/R2)
- Lower R gives better interference immunity, and is less sensitive to interference, layout parasitic, FB node leakage, and improper probing to FB pin.

Hence for applications without standby or suspend modes lower R1 and R2 values are preferred, while for applications concerning the current consumption in standby or suspend modes, higher values of R1 and R2 are needed. Such high impedance feedback loop is sensitive to any interference, which requires careful PCB layout and avoid any interference, especially to FB pin.

To improve the system stability, a proper value capacitor between FB pin and Vout is suggested. An empirical suggestion is around 100pF for MΩ feedback resistors and 10nF～0.1uF for lower R values.

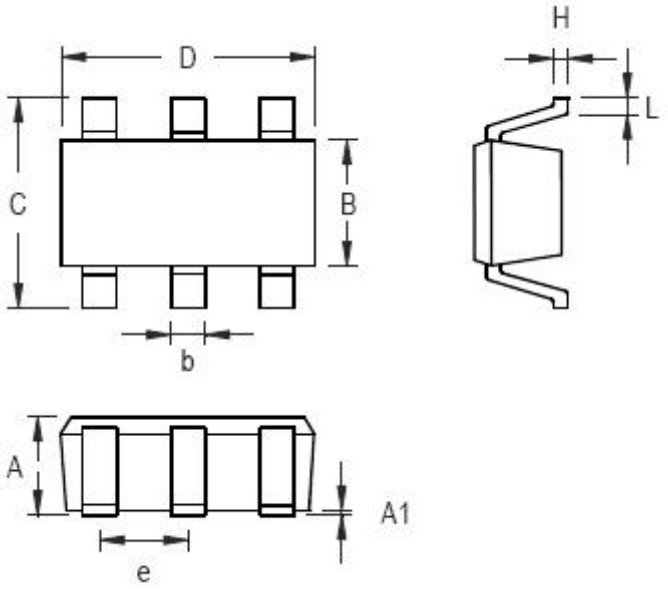
3) PCB Layout Guide

PCB Layout shall follow these guidelines for better system stability:

- A full GND plane without any gap break.
- VDD to GND bypass Cap – The 1μF MLCC noise bypass Cap between pin 5 and pin 2 shall have short and wide connections.
- Vin to GND bypass Cap – Add a Cap close to the inductor when Vin is not an idea voltage source.
- Minimize the FB node copper area and keep it far away from noise sources.

PACKAGE INFORMATION

SOT-23-6



SYMBOL	DIMENSION (in mm)		DIMENSION (in Inch)	
	MIN	MAX	MIN	MAX
A	0.787	1.450	0.031	0.057
A1		0.152		0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.559	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024