WESTERN DIGITAL
CORPORATION

PT 1482-01 (PSAT)
Programmable Synchronous & Asynchronous Transmitter

FEATURES

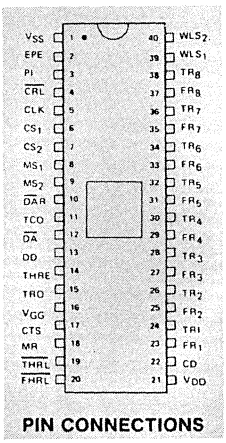
- SYNCHRONOUS, ASYNCHRONOUS OR ISOCHRONOUS OPERATION
- DC TO 640K BITS/SEC, 1X CLOCK PT1482-01
- DC TO 100K BITS/SEC, 1X CLOCK PT1482
- PROGRAMMABLE MATCH (FILL) CHARACTER
- SELECTABLE 5,6,7, OR 8 BIT PER CHARACTER
- EVEN/ODD PARITY GENERATOR. PARITY INHIBIT
- PROGRAMMABLE CLOCK RATE 1X, 16X, 32X, OR 64X.
- AUTOMATIC START & STOP BIT GENERATION IN ASYNCHRONOUS & ISOCHRONOUS MODES
- PROGRAMMABLE 1 AND 2 STOP BITS, (1½ IN 5 LEVEL MODE)
- AUTOMATIC CHARACTER STATUS AND DELIMITING SIGNAL GENERATION
- THREE STATE OUTPUTS — BUS STRUCTURE COMPATIBILITY
- DOUBLE BUFFERED
- TTL AND DTL COMPATIBLE — INTERNAL ACTIVE PULL UP
- COMPATIBLE RECEIVER, PR1472.

GENERAL DESCRIPTION

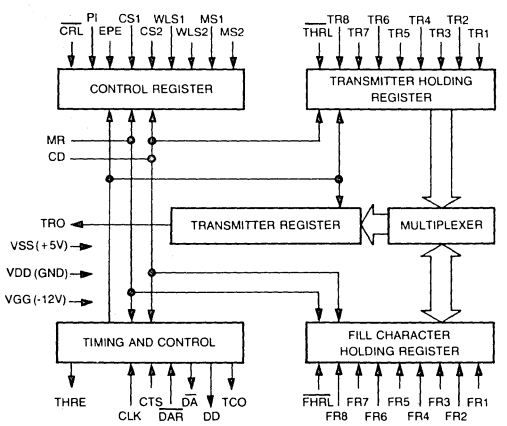
The Western Digital PT1482 (PSAT) is a programmable transmitter that interfaces variable length parallel data to a serial data channel. The transmitter converts parallel characters into a serial data stream with a format compatible with all standard Synchronous, Asynchronous or Isoschronous data communications media.

Contiguous serial characters are transmitted in the Synchronous Mode with the automatic insertion of a programmable Fill (Idle) Character during the absence of parallel input data. Programming the Asynchronous Mode selects serial transmission with automatic insertion of Start and Stop Bits. Isoschronous mode selects transmission with automatic fill character insertion during the absence of parallel input data. Four internal registers and a multiplexer, in conjunction with Three-State Output Lines, provide full system versatility.

The PSAT is a TTL compatible device. The use of internal active pull-up devices and push-pull output drivers, provides direct compatibility with all forms of current sinking logic. Western Digital also offers a compatible Receiver, PR1472.



PIN CONNECTIONS



PT1482 BLOCK DIAGRAM

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
1	V_{SS} POWER SUPPLY	V_{SS}	+5 Volt Supply
2	EVEN PARITY ENABLE	EPE	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the EPE and PI Inputs.
3	PARITY INHIBIT	PI	The Even Parity Enable Input and the Parity Inhibit Input to the Control Register, in conjunction with the Control Register Load and Chip Disable, select even, odd or no parity to be generated by the Transmitter. A high-level input voltage, V_{IH}, applied to EPE selects even parity and a low-level input voltage, V_{IL}, selects odd parity if a low-level input voltage is applied to Parity Inhibit and Chip Disable.
			PI / EPE / SELECTED PARITY / COMMENTS V_{IL} / V_{IL} / ODD / CD = V_{IL} V_{IL} / V_{IH} / EVEN / CD = V_{IL} V_{IH} / X / NONE / CD = V_{IL}
			NOTE: IF CD = V_{IH}, NO PROGRAMMING IS PERFORMED SINCE INPUTS ARE DISABLED.
			X – either V_{IL} or V_{IH} When programmed, the appropriate parity is generated following, and is contiguous with, the last data bit of a character, immediately preceding the stop element of asychronous and isochronous characters.
			A high-level input voltage, V_{IH}, applied to CD disables EPE, PI, and $\overline{CRL}$.
4	$\overline{CONTROL\ REGISTER\ LOAD}$	$\overline{CRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{CRL}$ input.
			A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Control Register and loads it with Control Bits (EPE, PI, CS_1, CS_2, MS_1, MS_2, WLS_1, WLS_2). A high-level input voltage, V_{IH}, applied to this line disables the Control Register. This line may be strobed or hard-wired to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD, disables $\overline{CRL}$.
5	TRANSMITTER REGISTER CLOCK	TRC	This is a fifty (50) percent duty cycle clock. The positive going edge of this Clock shifts data out of the Transmitter Register at a rate determined by the Control Bits CS_1 and CS_2, and provides the basic time reference for all device functions.
6-7	CLOCK RATE SELECT	CS_1-CS_2	A low-level input voltage, V_{IL}, applied to CD enables the CS_1 and CS_2 inputs. These two lines select the internal clock rate divider ratio to produce the transmitter bit rate defined by the Truth Table below:
			CS_2 / CS_1 / SELECTED CLOCK INPUT RATE V_{IL} / V_{IL} / 1X BIT RATE V_{IL} / V_{IH} / 16X BIT RATE V_{IH} / V_{IL} / 32X BIT RATE V_{IH} / V_{IH} / 64X BIT RATE

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			A high-level input voltage, V_{IH}, applied to CD disables CS_1 and CS_2.
8-9	MODE SELECT	MS_1-MS_2	These lines may be strobed or hard-wired to the appropriate input voltage. A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the MS_1 and MS_2 inputs. These lines select the transmitter operating mode. **MS_2 MS_1 MODE** V_{IL} V_{IL} ASYNCHRONOUS — ONE STOP BIT V_{IL}* V_{IH}*ASYNCHRONOUS — TWO STOP BITS V_{IH} V_{IL} SYNCHRONOUS V_{IH} V_{IH} ISOCHRONOUS *Selects 1.5 stop bits for 5-level codes. A high-level input voltage, V_{IH}, applied to CD disables MS_1 and MS_2.
10	$\overline{\text{DATA NOT AVAILABLE}}$ RESET	$\overline{\text{DAR}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DAR}}$ input. A low-level input voltage, V_{IL}, applied to this line resets the Data Not Available Flag. A high-level Input, V_{IH}, applied to CD disables $\overline{\text{DAR}}$. This input is not used during asynchronous operation.
11	TRANSMITTER CLOCK OUTPUT	TCO	This output is a clock at the transmitted bit rate. The negative going edge of this clock corresponds to the center of each transmitted data bit. The positive going edge corresponds to the start of each data bit transmission. All waveforms in this specification are referenced to TCO.
12	$\overline{\text{DATA NOT AVAILABLE}}$ FLAG	$\overline{\text{DA}}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{\text{DA}}$ input. A high-level output voltage, V_{OH}, on this line indicates that a Fill-Character has been transmitted, since a character was not loaded into the Transmitter Holding Register by the center of the last bit of a Synchronous Character or the center of the Stop Element of an Isochronous character. A high-level input voltage, V_{IH}, applied to CD disables $\overline{\text{DA}}$. This input is not used during asynchronous operation.
13	DATA DELIMIT/ END OF CHARACTER	DD/EOC	During asynchronous operation, a high-level output voltage, V_{OH}, indicates data is being transmitted. A low-level output voltage, V_{OL}, indicates that a Start or Stop Element is being transmitted. A low-level output voltage during synchronous operation indicates that the last bit of a character is being transmitted.

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
14	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A low-level input voltage applied to CD (pin 22) enables the THRE input. A high-level output voltage, V_{OH}, on this line indicates the Transmitter Holding Register is empty and has transferred its contents to the Transmitter Register and may be loaded with a new character. This line goes to a low-level output voltage, V_{OL}, when THRL goes to a low-level input voltage, V_{IL}. A high-level input voltage, V_{IH}, applied to CD disables THRE.
15	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the Transmitter Holding Register are serially shifted out as an NRZ waveform on this line provided that a character was loaded into the Transmitter Holding Register prior to $\overline{DA}$ Flag (in Synchronous or Isochronous Modes). If a character was not loaded prior to a $\overline{DA}$ Flag, the contents of the Fill-Character Register are transmitted as the next character.
16	V_{GG} POWER SUPPLY	V_{GG}	– 12 Volts Supply.
17	CLEAR-TO-SEND	CTS	The Clear-To-Send Control initiates or disables transmission as a function of the state of this line. A high-level input voltage, V_{IH}, initiates serial data transmission provided a character has been loaded into the Transmitter Holding Register. A low-level input voltage, V_{IL}, applied to this line during transmission allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.
18	MASTER RESET	MR	The rising edge of a high-level input voltage, V_{IH}, applied to this line resets timing and control logic to an idle state, sets THRE, the contents of the Fill-Character Holding Register, and TRO to a high-level output voltage, V_{OH}.
19	$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$	$\overline{THRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{THRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Transmitter Holding Register and loads it with the Transmitter Holding Register data and forces THRE to a low-level output voltage, V_{OL}. A high-level input voltage, V_{IH}, applied to this line disables the Transmitter Holding Register. A high-level input voltage, V_{IH}, applied to CD disables $\overline{THRL}$.
20	$\overline{\text{FILL-CHARACTER HOLDING REGISTER LOAD}}$	$\overline{FHRL}$	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the $\overline{FHRL}$ input. A low-level input voltage, V_{IL}, applied to this line enables DC Latches of the Fill-Character Holding Register and loads it with the Fill-Character Register data FR_1-FR_8. A high-level input voltage, V_{IH}, applied to this line disables the $\overline{FHRL}$ Register. This line may be strobed or hard-wired to a low-

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			level input voltage, V_{IL}. This input is not used during asynchronous operation. A high-level input voltage, V_{IH}, applied to CD disables $\overline{FHRL}$.
21	V_{DD} POWER SUPPLY	V_{DD}	Ground.
22	CHIP DISABLE	CD	This line controls the disconnect associated with busable inputs and Three-State outputs. A high-level input voltage, V_{IH}, applied to this line removes drive from push-pull outputs causing them to float. Drivers of disabled inputs are required to sink or source current. The I/O Lines controlled by Chip Disable are defined below: **INPUT LINES** / **TRI-STATE OUTPUT LINES** $\overline{CRL}$, $\overline{THRL}$, $\overline{DA}$ EPE, $\overline{FHRL}$, THRE PI, FR_1-FR_8 CS_1-CS_2, TR_1-TR_8 $\overline{MS_1}$-MS_2, WLS_1, WLS_2 $\overline{DAR}$
23, 25 27, 29 31, 33 35, 37	FILL-CHARACTER HOLDING REGISTER DATA INPUTS	FR_1-FR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Fill-Character Holding Register and associated Load Strobe, $\overline{FHRL}$. Parallel 8-bit characters are input into the Fill-Character Holding Register with the $\overline{FHRL}$ Strobe (pin 20). If a character of less than 8 bits has been selected (by WLS_1 and WLS_2) only the least significant bits are accepted. These lines may be strobed or hard-wired to the appropriate input voltage. These inputs are not used during asynchronous operation. During Synchronous or Isochronous transmission, the Fill-Character is transmitted if a character was not loaded into the Transmitter Holding Register prior to a $\overline{DA}$ Flag; i.e., the Transmitter Holding Register did not contain a character at the center of the last bit being transmitted from the Transmitter Register. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted, Least Significant Bit (FR_1) to Most Significant Bit (FR_n) order. A high-level input voltage, V_{IH}, applied to CD disables FR_1-FR_8.
24, 26 28, 30 32, 34 36, 38	TRANSMITTER HOLDING REGISTER DATA INPUTS	TR_1-TR_8	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs to the Transmitter Holding Register and associated Load Strobe, $\overline{THRL}$. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), only the least significant bits are accepted. A high-level input

PIN NUMBER	I/O NAME	SYMBOL	FUNCTION
			voltage, V_{IH}, will cause a high-level output voltage to be transmitted, Least Significant Bit (TR_1) to Most Significant Bit (TR_n) order. A high-level input voltage, V_{IH}, applied to CD disables TR_1-TR_8.
39-40	WORD LENGTH	WLS_1-WLS_2	A low-level input voltage, V_{IL}, applied to CD (pin 22) enables the inputs of the Control Register and Load, $\overline{CRL}$. Parallel 8-bit characters are input into the Control Register with the $\overline{CRL}$ Strobe (pin 4), WLS_1 and WLS_2 select the transmitted character length from five (5) to eight (8) bits defined by the Truth Table below:

WLS_2	WLS_1	SELECTED WORD LENGTH
V_{IL}	V_{IL}	5 BITS
V_{IL}	V_{IH}	6 BITS
V_{IH}	V_{IL}	7 BITS
V_{IH}	V_{IH}	8 BITS

A high-level input voltage, V_{IH}, applied to CD disables WLS_1 and WLS_2, forcing them to float.

ORGANIZATION

PT1482 block diagram is illustrated on page 1.

Control Register — Programming of the PSAT is accomplished by loading the 8 Bit Control Register. Mode selection, clock divisor, word length, and parity are selected when the Control Register Load signal is activated.

Transmitter Register — The Transmitter Register is used to store the outgoing data stream. The contents of this register are derived from either the Transmitter Holding Register or the Fill (Match) Character Holding Register with the Control and Timing Logic automatically adding the required start and stop bits during Asynchronous and Isoschronous Modes.

Transmitter Holding Register — The Transmitter Holding Register, a buffer register, is used to store the parallel character to be serially transmitted.

Fill Character Holding Register — The Fill Character Holding Register is used to store the Fill (Match) Character which is transmitted during the absence of characters in the Transmitter Holding Register.

Timing and Control — The Timing and Control Logic generates the required control signals to transmit Data and Fill Characters. Character transmission status signals are also derived from this logic.

SYNCHRONOUS MODE OPERATION

Synchronous transmission requires that characters (programmably variable from 5 to 8 data bits plus parity) are contiguous with no start or stop bits. Since the requirement that characters are contiuous does not imply that the system servicing the transmitter always has ample time to load the Transmitter Holding Register, it is necessary that a character be transmitted when data has not been loaded into the Transmitter Holding Register. This character is defined as the Fill or Idle Character and a separate register has been provided to load this character upon initialization. The Fill-Character Holding Register is loaded by strobing the Fill-Character Holding Register Load ($\overline{FHRL}$) line or hard-wiring it to a low-level input voltage.

Referring the Block Diagram of the Transmitter, it can be seen that the Chip Disable (CD) enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{CRL}$, $\overline{THRL}$, and $\overline{FHRL}$ are under CD control. In addition, the Transmitter Holding Register Empty (THRE) Flag, Data Not Available ($\overline{DA}$) Flag, and the Data Not Available Reset ($\overline{DAR}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. The P/SAT will enter a defined "idle" state when the Master Reset (MR) is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Flag is set to a high-level output voltage, the Data Delimit/End of Character (DD/EOC) Flag

is set to a low-level output voltage, and the contents of the Fill-Character Holding Register are forced to a high-level output voltage.

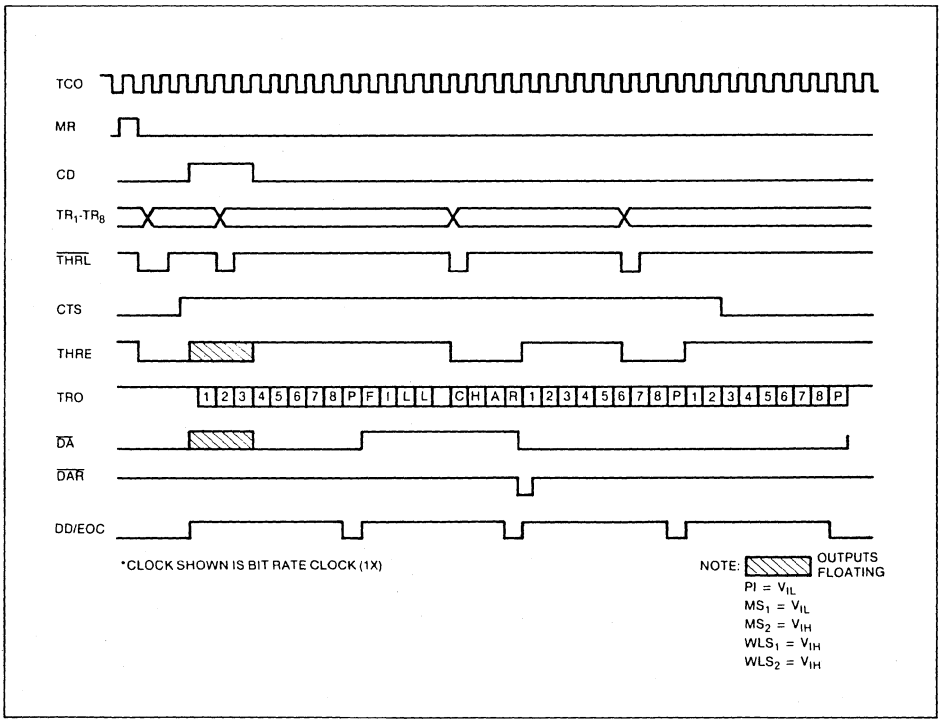
When the P/SAT is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage, defines the mode of operation, character length, selected parity if required, and the clock rate selection. Table 1 illustrates all the programmable synchronous character formats.

To initialize transmission the CTS signal must be set to a high state and the transmitter holding register must be loaded with a character to be transmitted. The transmitter will remain in an idle state until this is accomplished.

The character transferred into the Transmitter Register (from the Transmitter Holding Register or the Fill-Character Holding Register) is determined at the center of the last bit of the character being transmitted. If, at this time, no character has been loaded into the Transmitter Holding Register, the Fill-Character is loaded into the Transmitter Register at the end of the bit being transmitted

Table 1. SYNC MODE CONTROL DEFINITION

CONTROL WORD						CHARACTER FORMAT	
MSS 2	MSS 1	WLS 2	WLS 1	PI	EP	DATA BITS	ADDED PARITY BIT
1	0	0	0	0	0	5	ODD
1	0	0	0	0	1	5	EVEN
1	0	0	0	1	X	5	NONE
1	0	0	1	0	0	6	ODD
1	0	0	1	0	1	6	EVEN
1	0	0	1	1	X	6	NONE
1	0	1	0	0	0	7	ODD
1	0	1	0	0	1	7	EVEN
1	0	1	0	1	X	7	NONE
1	0	1	1	0	0	8	ODD
1	0	1	1	0	1	8	EVEN
1	0	1	1	1	X	8	NONE
↑ Sets to SYNC Mode							



SYNCHRONOUS TIMING EXAMPLE

and a Data Not Available ($\overline{DA}$) Flag is set to a high-level output voltage. This Fill-Character will be repeatedly transmitted until a character is loaded into the Transmitter Holding Register, at which time, the Data Not Available Flag is reset, the Fill-Character will be completed and the newly loaded synchronous character will follow contiguously.

A high-level output voltage, on the THRE Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load ($\overline{THRL}$) line is strobed to a low-level input voltage, forcing the THRE Flag to a low-level output voltage. This data must be stable prior to $\overline{THRL}$ going to a high-level input voltage since this register is a set of DC latches which are enabled by $\overline{THRL}$.

If the Clear-To-Send (CTS) line is at a low-level input voltage, or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or completion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register which forces the THRE Flag to be set to high-level output voltage. The selected parity is added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform. A low-level input voltage applied to CTS during transmission allows completion of that character only, after which the device enters the idle state and the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. The Data Delimit/End of Character Flag is defined as a low-level output voltage during transmission of the last bit of a synchronous character and when the P/SAT is in the "idle" state.

ASYNCHRONOUS MODE OPERATION

An asynchronous character consisting of a start bit, followed by data (programmably variable from 5 to 8 data bits), parity (if so programmed), and a stop "element" is serially transmitted, in that order, as an NRZ waveform by the P/SAT. The stop interval is referred to as an "element" since its minimum length is under program control and may be 1 or 2 bits in length. When programmed for 2 stop bits, a 5-level (bit) code will be transmitted with 1.5 stop bits.

Referring to the Block Diagram of the Transmitter, it can be seen that the Chip Disable enables or disconnects various inputs and outputs of the P/SAT. The inputs to the Control Register, Transmitter Holding Register, Fill-Character Holding Register and their respective load strobes, $\overline{CRL}$, $\overline{THRL}$ and $\overline{FHRL}$ are under CD control. In addition, the Transmitter Holding Register Empty Flag (THRE), the Data Not Available Flag ($\overline{DA}$), and the Data Not Available Reset ($\overline{DAR}$) are also controlled by CD. It is necessary that CD enable these lines to allow strobing information into these registers and to allow examination of these output flags. It should be noted that the Fill-Character Holding Register and its associated load strobe, $\overline{FHRL}$, the Data Not Available Flag and its associated reset, $\overline{DAR}$, play no role in asynchronous communications and are only mentioned here for completeness.

The P/SAT will enter a defined "idle" state when the Master Reset (MR) line is strobed to a high-level input voltage. In this state, all timing and control logic are reset, the Transmitter Register Output continues to mark, the Transmitter Holding Register Empty Flag is set to a high-level output voltage, V_{OH}, and the Data Delimit/End of Character (DD/EOC) Flag is reset to a low-level output voltage.

When the transmitter is enabled by CD, loading the Control Register by strobing the Control Register Load ($\overline{CRL}$) line to a low-level input voltage, V_{IL}, defines the mode of operation, character length, selected parity if required and the clock rate selection. Table 2 illustrates all the programmable asynchronous formats.

Continuous transmission, transmission of characters with the minimum number of stop bits programmed, is accomplished by loading the Transmitter Holding Register within a character time of when its "Empty Flag" becomes a high-level output voltage. A high-level output voltage, V_{OH}, on the Transmitter Holding Register Empty (THRE) Flag indicates that the Transmitter Holding Register is empty and may be loaded with a character. Data on the inputs of the Transmitter Holding Register is loaded when the Transmitter Holding Register Load ($\overline{THRL}$) line is strobed to a low-level input voltage, V_{IL}, for ng the THRE Flag to a low-level output voltage, V_{OL}. This data must be stable prior to $\overline{THRL}$ going to a high-level input voltage since this register is a set of DC latches which are enabled by $\overline{THRL}$. If the Clear-To-Send (CTS) line is at a low-level input voltage or if the Transmitter Register is in the process of transmitting a character, the character in the Transmitter Holding Register will not be transferred down to the Transmitter Register and the THRE Flag will remain at a low-level output voltage. Raising the CTS line to a high-level input voltage or completion of transmission of a character from the Transmitter Register causes the automatic transfer of the character in the Transmitter Holding Register to the Transmitter Register and the THRE flag will be set to a high-level output voltage.

The start bit, selected parity and stop bit(s), determined by the Control Register programming, are added to the data during the transfer to the Transmitter Register and serial transmission is initiated as an NRZ waveform.

A low-level input voltage, applied to CTS during transmission, allows completion of that character only, after which the output will continue to mark until a high-level input voltage is applied.

The Data Delimit/End of Character Flag has been provided to indicate the transmission of serial data on the Transmitter Register Output. Data Delimit is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. Neither TRO, CTS nor DD/EOC is under control of Chip Disable.

ISOCHRONOUS MODE OPERATION

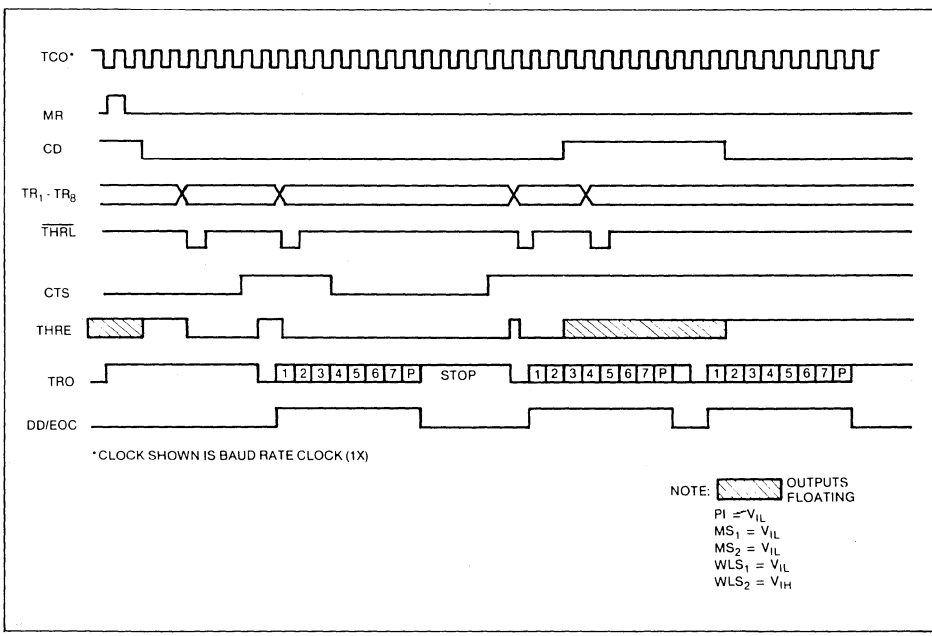
In the Isochronous Mode of operation all (Synchronous Mode) definitions apply with the exception of those for the Data Delimit/End of Character (DD/EOC) Flag and the Data Not Available Flag (DA).

This is the case since Isochronous Data Transmission requires contiguous characters with the addition of a start and a single stop bit added to each character.

Table 2. ASYNC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MS2	MS1	WLS2	WLS1	L	PI	E	START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
0	0	0	0	0	0	0	1	5	ODD	1
0	1	0	0	0	0	0	1	5	ODD	1.5
0	0	0	0	0	0	1	1	5	EVEN	1
0	1	0	0	0	0	1	1	5	EVEN	1.5
0	0	0	0	1	X		1	5	NONE	1
0	1	0	0	1	X		1	5	NONE	1.5
0	0	0	1	0	0		1	6	ODD	1
0	1	0	1	0	0		1	6	ODD	2
0	0	0	1	0	1		1	6	EVEN	1
0	1	0	1	0	1		1	6	EVEN	2
0	0	0	1	1	X		1	6	NONE	1
0	1	0	1	1	X		1	6	NONE	2
0	0	1	0	0	0		1	7	ODD	1
0	1	1	0	0	0		1	7	ODD	2
0	0	1	0	0	1		1	7	EVEN	1
0	1	1	0	0	1		1	7	EVEN	2
0	0	1	0	1	X		1	7	NONE	1
0	1	1	0	1	X		1	7	NONE	2
0	0	1	1	0	0		1	8	ODD	1
0	1	1	1	0	0		1	8	ODD	2
0	0	1	1	0	1		1	8	EVEN	1
0	1	1	1	0	1		1	8	EVEN	2
0	0	1	1	1	X		1	8	NONE	1
0	1	1	1	1	X		1	8	NONE	2

↑ Sets to ASYNC Mode



ASYNCHRONOUS TIMING EXAMPLE

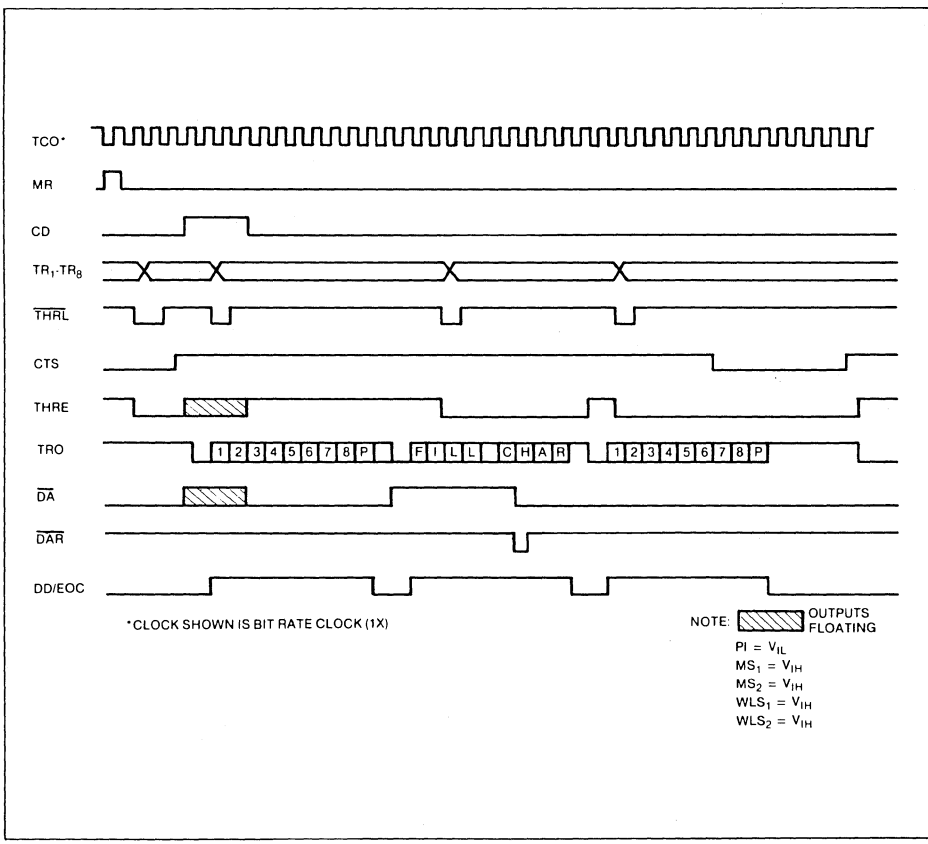
The Data Delimit/End of Character Flag is a low-level output voltage during start and stop bits and is a high-level output voltage during transmission of data and parity. The Data Not Available Flag ($\overline{DA}$) is set to a high-level output voltage at the end of the stop bit if a character has not been loaded into the Transmitter Holding Register at the center of the stop bit. The contents of the Fill-Character Holding Register will be transferred into the Transmitter Register and repeatedly transmitted until a character is loaded into the Transmitter Holding Register. At this time, the Fill-Character will be completed and the newly loaded isochronous character will follow contiguously.

Table 3 illustrates all the programmable isochronous character formats.

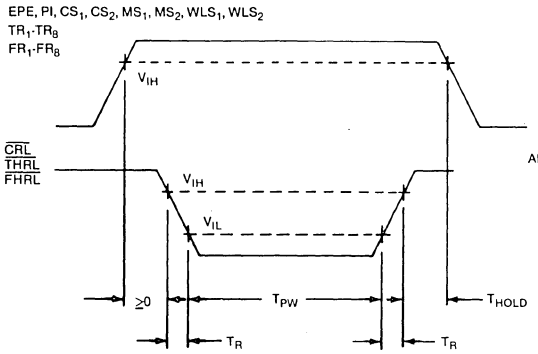
Table 3. ISOC MODE CONTROL DEFINITION

CONTROL WORD							CHARACTER FORMAT			
MSS2	MSS1	WLS2	WLS1	I	EPE	PE	START BIT	DATA BITS	ADDED PARITY BIT	STOP ELEMENTS
1	1	0	0	0	0	0	1	5	ODD	1
1	1	0	0	0	0	1	1	5	EVEN	1
1	1	0	0	1	X	X	1	5	NONE	1
1	1	0	1	0	0	0	1	6	ODD	1
1	1	0	1	0	0	1	1	6	EVEN	1
1	1	0	1	1	X	X	1	6	NONE	1
1	1	1	0	0	0	0	1	7	ODD	1
1	1	1	0	0	0	1	1	7	EVEN	1
1	1	1	0	1	X	X	1	7	NONE	1
1	1	1	1	0	0	0	1	8	ODD	1
1	1	1	1	0	0	1	1	8	EVEN	1
1	1	1	1	1	X	X	1	8	NONE	1

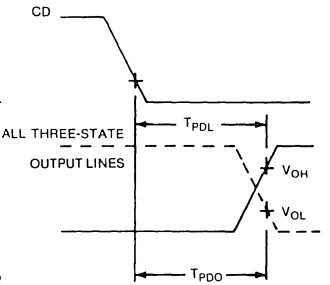
↑ Sets to ISOC Mode



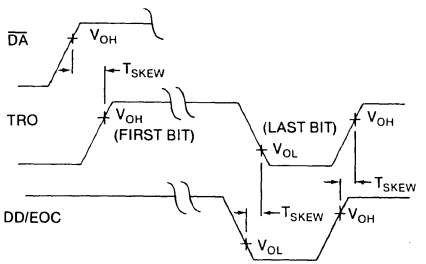
ISOCHRONOUS TIMING EXAMPLE



DATA INPUT LOAD CYCLE

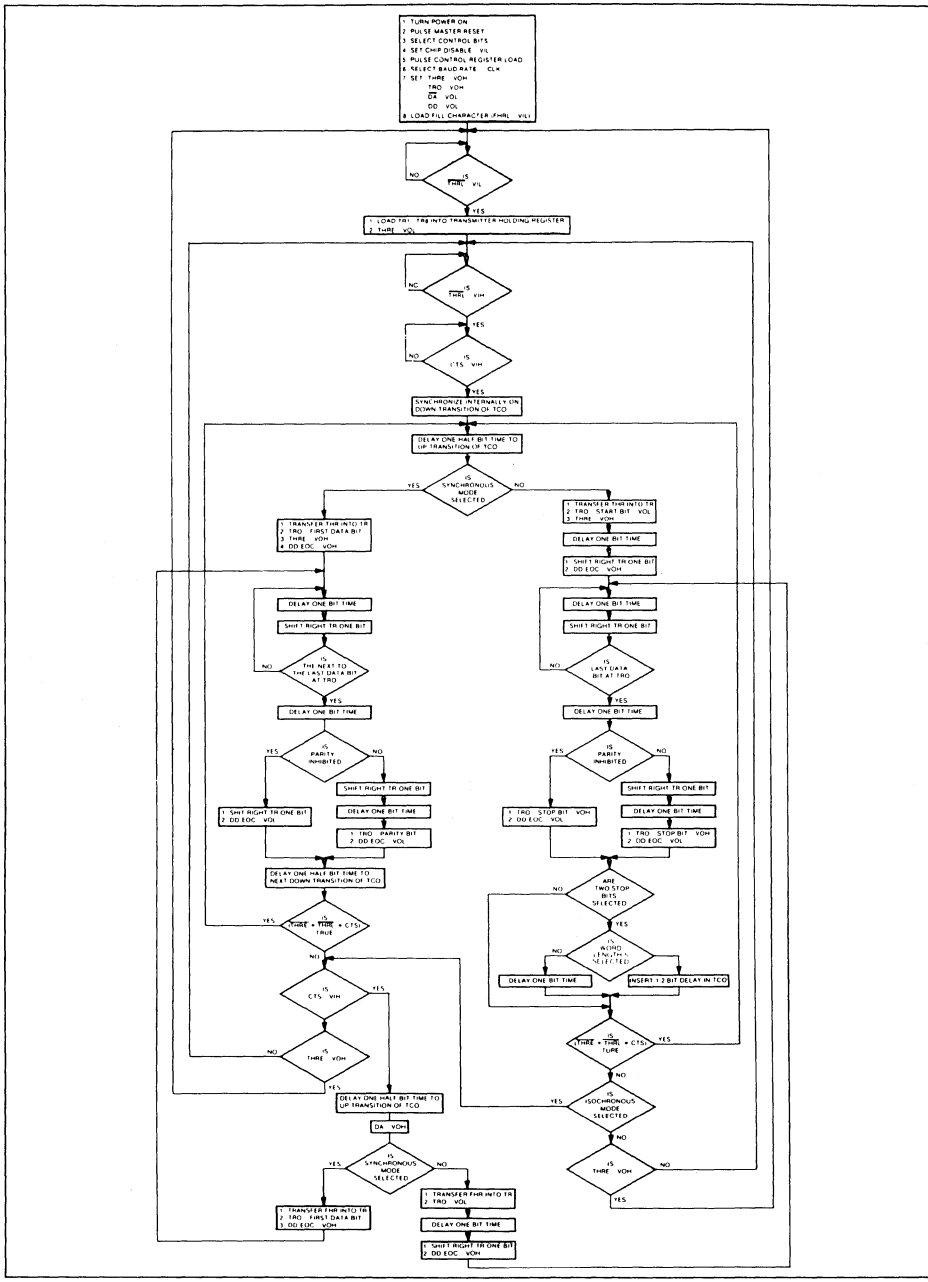


OUTPUT ENABLE DELAYS

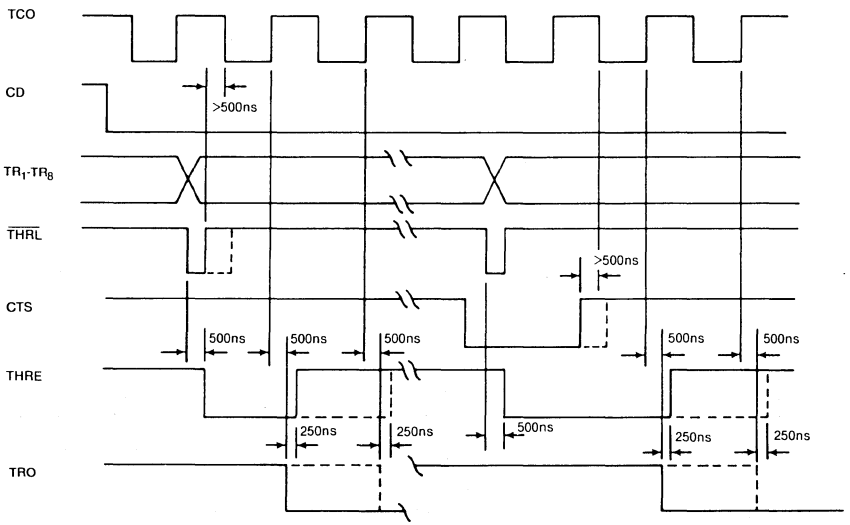


SKEW TIMES

SWITCHING WAVEFORMS



PT1482 SYNCHRONOUS ASYNCHRONOUS TRANSMITTER FLOW CHART



TIMING DETAIL

ABSOLUTE MAXIMUM RATINGS

V_{GG} Supply Voltage		+0.3V to −20V
V_{DD} Supply Voltage		+0.3V to −20V
Clock Input Voltage*		+0.3V to −20V
Logic Input Voltage*		+0.3V to −20V
Logic Output Voltage*		+0.3V to −20V
Storage Temperature	Ceramic	−65°C to +150°C
	Plastic	−55°C to +125°C
Operating Free-Air Temperature T_A Range		0°C to +70°C
Lead Temperature (Soldering, 10 sec.)		300°C

*$V_{GG} = V_{DD} = OV$

NOTE: These voltages are measured with respect to V_{SS} (Substrate)

ELECTRICAL CHARACTERISTICS

($V_{SS} = V_{CC} = 5V \pm 5\%$, $V_{DD} = OV$, $V_{GG} = -12V \pm 5\%$, $T_A = 0°C$ to $+70°C$ unless otherwise specified)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
	INPUT LOGIC LEVELS[1]			
V_{IL}	Low-level Input Voltage		0.8V	$V_{SS} = 4.75V$
V_{IH}	High-level Input Voltage	V_{SS}-1.5V		
	OUTPUT LOGIC LEVELS[2]			
V_{OL}	Low-level Output Voltage		0.5V	$V_{SS} = 5.25V$, $I_{OL} = -1.6mA$
V_{OH}	High-level Output Voltage	V_{SS}-1.0V		$V_{SS} = 4.75V$, $I_{OH} = -100\mu A$
	INPUT CURRENT –			
I_{IL}	Low-level Input Current (each input)		-1.6mA	$V_{SS} = 5.25V$, $V_{IN} = 0.4V$

**Not more than one output should be shorted at a time.

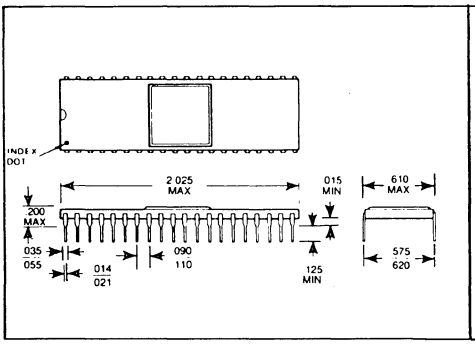
NOTE: 1) Inputs under Chip Disable control when disabled (V_{IH} applied to CD), are logically disabled and appear as a single TTL load.

2) Outputs under Chip Disable control when disabled (V_{IH} applied to CD) are logically and electrically disconnected and caused to float.
The Three-State Output has three states;
(1) Low impedance to V_{CC} (2) Low impedance to GND (3) High impedance OFF 10 Megohm.
$I_{SS} = 35mA$ $I_{GG} = 10mA$

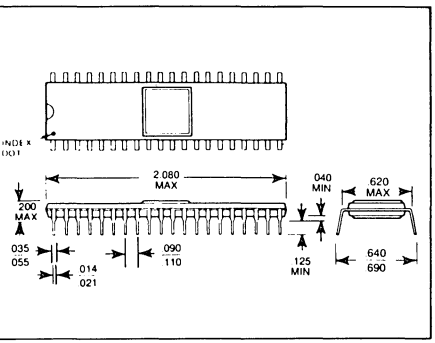
SWITCHING CHARACTERISTICS

($V_{SS} = V_{CC} = 5V$, $V_{DD} = OV$, $V_{GG} = -12V$, $T_A = 25°$, $C_L = 20pf$)

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
F_C	Clock Frequency	DC	100 KHz	1482B
		DC	640 KHz	1482B-01
	PULSE WIDTH			
T_{HOLD}	Hold Time	20 nsec		
$T_{\overline{CRL}}$	Control Register Load	250 nsec		
$T_{\overline{THRL}}$	Transmitter Holding Register Load	250 nsec		
$T_{\overline{FHRL}}$	Fill-Character Holding RegisterLoad	250 nsec		
$T_{\overline{DAR}}$	Data Not Available Reset	200 nsec		
T_{MR}	Master Reset	500 nsec		
T_{PD}	Output Enable Delay		500 nsec	
T_{SKEW}	Skew Time		250 nsec	
T_R	Rise Time		150 nsec	
T_F	Fall Time		150 nsec	



PT1482A CERAMIC PACKAGE



PT1482B PLASTIC PACKAGE

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