普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

The PT2392 is a CMOS IC that has a microphone peripheral circuit and an echo generation circuit for karaoke use, on a single chip.

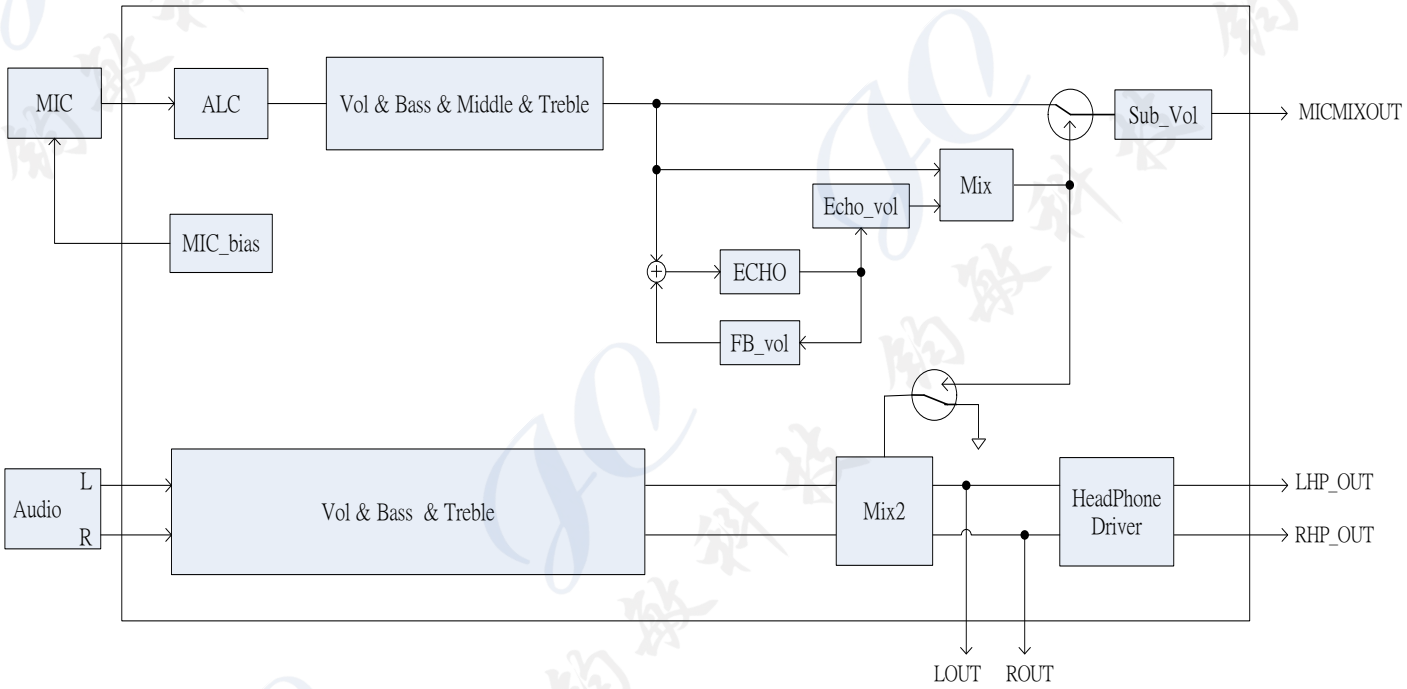
APPLICATIONS

- Wireless Microphone
- Karaoke System
- Consumer Audio Applications
- Car Entertainment System

FEATURES

- High-performance digital echo circuit using 44-Kbit RAM.
- wide delay time from 45 to 333ms in 22ms/step(typ.)
- A mic amplifier with an ALC makes it possible to handle overload input, and the ALC operating voltage are controlled by I²C Bus or externally set to the desired value.
- Built-in vol, bass,middle,treble,echo_vol, fb_volume,sub_vol and controlled by I²C Bus .
- Built-in HP Driver and DEPOP.
- Built-in MIC_bias.
- Internal micmixing amplifier.
- Master volume from +15dB to -79dB in 1dB/step.
- bass,middle,treble from +15dB to -15dB in 1dB/step.
- echo_vol ,sub_vol from 0dB to -28dB in 2dB/step.
- fb_vol from -2dB to -8dB in 1dB/step.

BLOCK DIAGRAM



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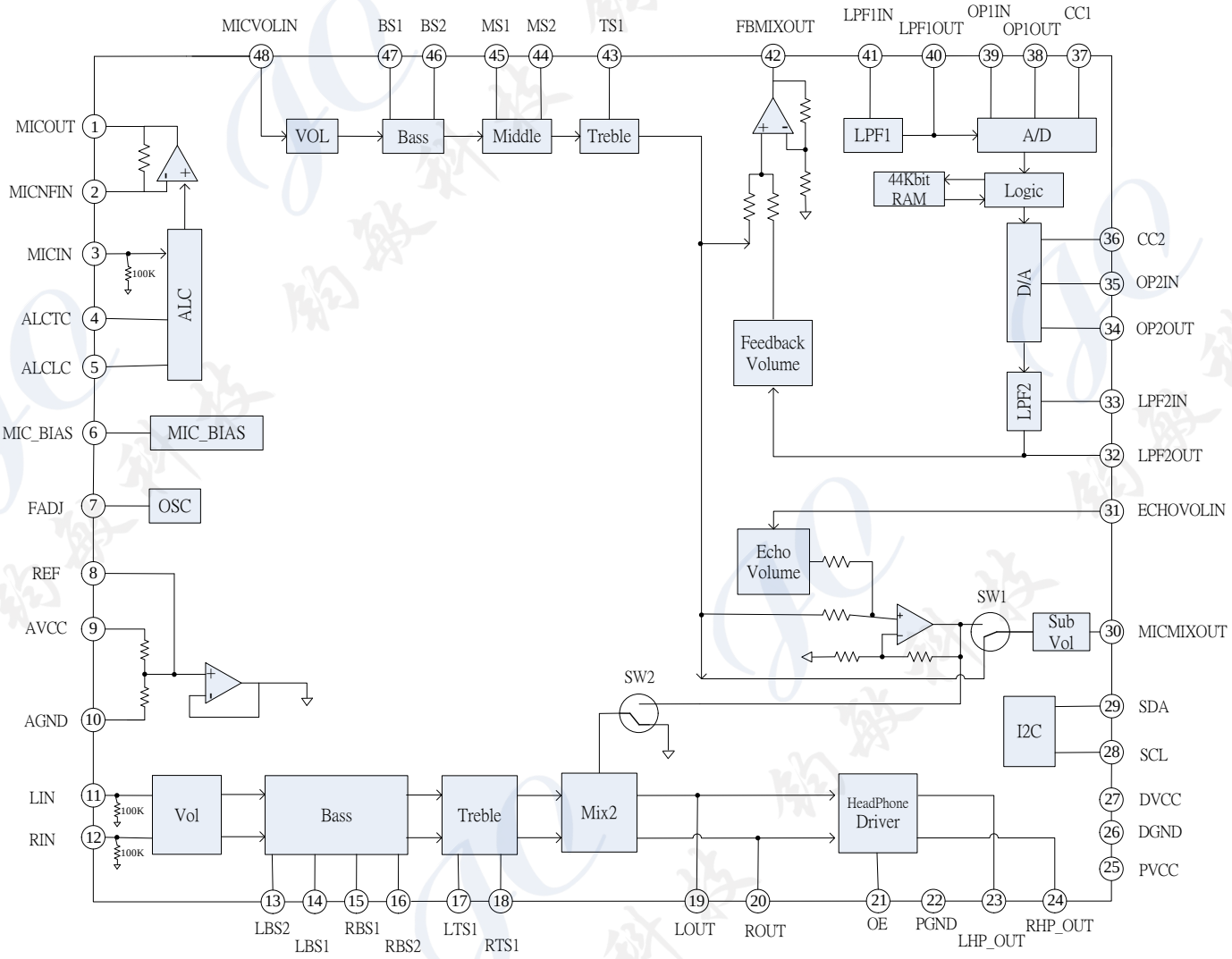
PIN CONFIGURATION

LQFP48



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PIN DESCRIPTION

LQFP48

Pin Name	I/O	Description	Pin No.
MICOUT	O	Microphone signal output	1
MICNFIN	-	External resistor for MIC gain setting	2
MICIN	I	Microphone input	3
ALCTC	-	External Capacitor for ALC function time control	4
ALCLC	-	External adjust for ALC level control	5
MICBIAS	I	Supply Voltage to MIC	6
FADJ	-	External resistor (12KΩ) connecting to VCC for system clock.	7
VREF	-	Analog reference voltage (1/2VCC)	8
AVCC	-	Analog supply voltage input	9
AGND	-	Analog power ground	10
LIN	I	Left channel input	11
RIN	I	Right channel input	12
LBS2	O	Left channel bass cap1	13
LBS1	I	Left channel bass cap2	14
RBS1	I	Right channel bass cap1	15
RBS2	O	Right channel bass cap2	16
LTS1	I	Left channel treble cap	17
RTS1	I	Right channel treble cap	18
LOUT	O	Left channel output	19
ROUT	O	Right channel output	20
OE	I	Out Enable setting,connect a cap to gnd	21
PGND	-	Headphone driver power ground	22
LHPOUT	O	Left channel headphone driver output	23
RHPOUT	O	Right channel headphone driver output	24
PVCC	-	Headphone driver supply voltage input	25
DGND	-	Digital power ground	26
DVCC	-	Digital supply voltage input	27
SCL	I	I2C clock input	28
SDA	I	I2C data input	29
MICMIXOUT	O	Output signal of main channel & ECHO mixing	30
ECHOVOLIN	I	Echo Sound signal input for mixing	31
LPF2OUT	O	Lowpass filter 2 input	32
LPF2IN	I	Lowpass filter 2 output	33
OP2OUT	O	OP Amplifier 2 input/output. These pin can be used as Modulated/	34
OP2IN	I	Demodulated Integrator by connecting Capacitor	35
CC2	-	Current control 2	36
CC1	-	Current control 1	37
OP1OUT	O	OP amplifier 1 input/output. These pin can be used as modulated/	38
OP1IN	I	Demodulated integrator by connecting capacitor	39
LPF1OUT	O	Lowpass filter 1 input	40
LPF1IN	I	Lowpass filter 1 output	41
FBMIXOUT	O	Output signal of main channel & FB mixing	42
TS1	I	Main channel treble cap	43
MS2	O	Main channel middle cap2	44
MS1	I	Main channel middle cap1	45
BS2	O	Main channel bass cap2	46
BS1	I	Main channel bass cap1	47

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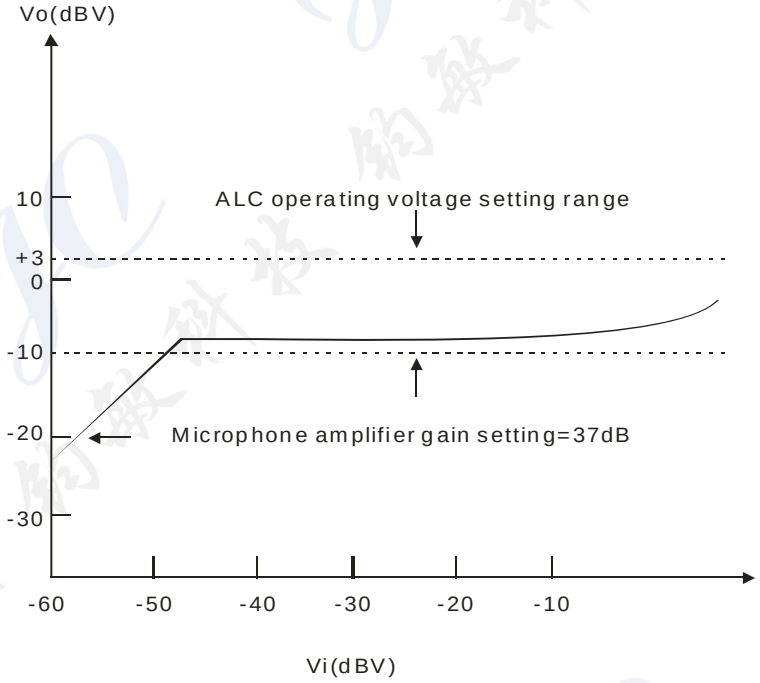
MICVOLIN	I	Main channel volume input	48

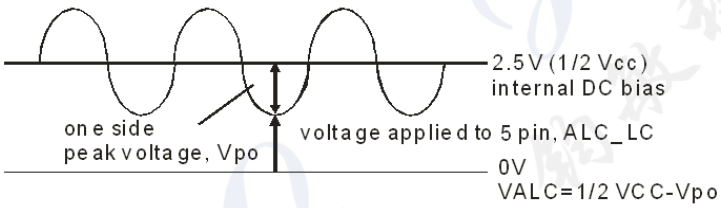
A FUNCTION DESCRIPTION

ALC LEVEL DIAGRAM



ALC OPERATING VOLTAGE SETTING

ALC operating voltage can be set at a desired value between -10 and +3dBV by control I²C Bus



To set ALC operating voltage at -5dB (Vcc=5V)

-5dBV=0.56Vrms=1.59Vp-p=0.8Vp-o
VALC=2.5-0.8=1.7V

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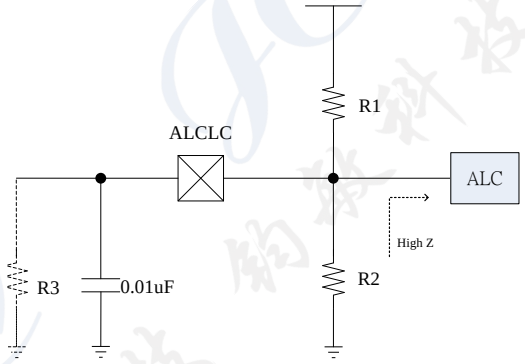
We can control I²C Bus, it is possible to provide ALC operating voltage by dividing resistance.(R1+R2=100K)



When V_{CC}=5V,ALC dBV(Sub Address: 02H):

Gain	I²C Bus Control			V_ALCLC
	D7	D6	D5	
ALC off	0	0	0	0V
+3dBV	0	0	1	0.65V
0dBV	0	1	0	1.17V
-2dBV	0	1	1	1.43V
-4dBV	1	0	0	1.64V
-6dBV	1	0	1	1.81V
-8dBV	1	1	0	1.95V
-10dBV	1	1	1	2.06V

if want other V_ALCLC ,we can parallel R3 to get the desired voltage value.

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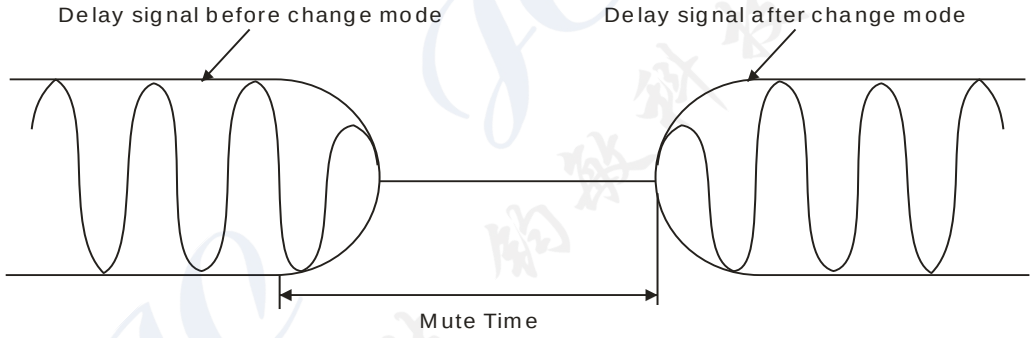
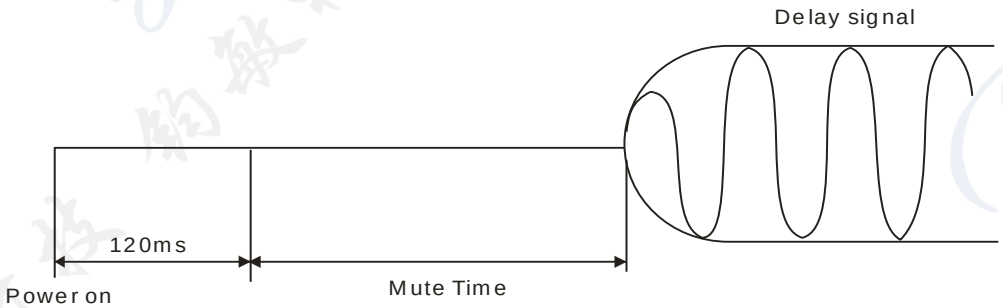
AUTOMATIC MUTE

UPON CHANGING DELAY TIME



Mute Time=524ms (Typ.)

UPON POWER ON



Mute Time=524ms (Typ.)

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DELAY TIME Td

The delay time can be calculated by the equation:
Td= N/fs (N= the number of memory bits: 44544)

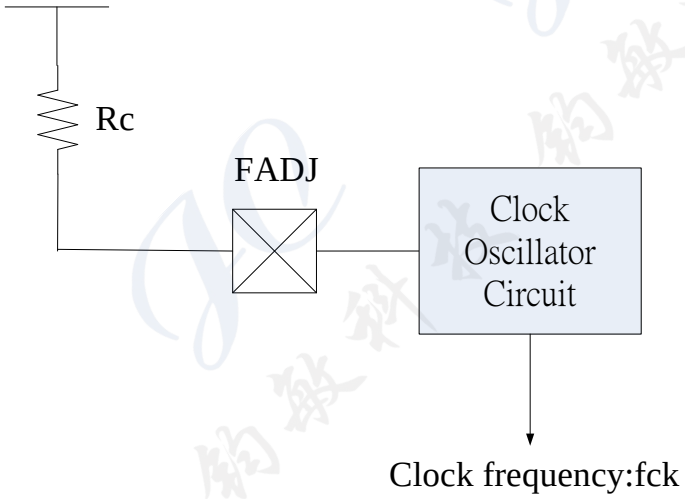
When fck=8MHz (fs=250KHz), Td can be set at 178ms. (at Td=178ms setting)

<Reference>
For clock frequency (fck)=8MHz, the sampling frequency (fs) is:

Td	fs
333ms	133KHz
311ms	143KHz
289ms	154KHz
267ms	167KHz
245ms	182KHz
223ms	200KHz
200ms	222KHz
178ms	250KHz
156ms	286KHz
134ms	333KHz
111ms	400KHz
89ms	500KHz
67ms	667KHz
45ms	1000KHz

CLOCK OSCILLATOR CIRCUIT

The PT2392 incorporates a current control type clock oscillator circuit in it, thus providing circuit configuration just by connecting a resistor for current control to pin7 (FADJ) CLOCK.
Fully internal clock supply prevents occurrence of undesired radiation without affecting any external circuit.
The oscillator frequency is fck=8MHz. (Rc=12KΩ)



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TEST MODE I²C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Sub Address	A	Data	A	P
1 bit	8 bit	1 bit	8 bit	1 bit	8 bit	1 bit	1 bit

S: Starting Term
A: Acknowledge Bit
P: Stop Term

If more than one Data Byte is transmitted, then the significant SUB ADDRESS bits are auto incremented. 00H→01H→ 00H

SLAVE ADDRESS

MSB							LSB
1	1	0	0	1	0	0	R/W_B

R/W_B=0: Write mode for register setting
R/W_B=1: Not available

SUB ADDRESS TABLE

Sub Address	Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
01H	-	<9>TEST MODE		-				1

<9>TEST MODE (Sub Address: 01H)

Mode	I²C Bus Control	
	D6	D5
Memory through and fs monitor	0	0
Mute pulse monitor	0	1
Memory only test “L”	1	0
Memory only test “H”	1	1

fs monitor : 5pin (at not necessary mute function)
Mute pulse monitor:5pin
Memory “L” output data monitor:5pin
Memory “H” output data monitor:5pin

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I²C BUS FORMAT

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Sub Address	A	Data	A	P
1 bit	8 bit	1 bit	8 bit	1 bit	8 bit	1 bit	1 bit

S: Starting Term
A: Acknowledge Bit
P: Stop Term

If more than one Data Byte is transmitted, then the significant SUB ADDRESS bits are auto incremented. 00H→01H→ 00H

SLAVE ADDRESS

MSB							LSB
1	1	0	0	1	0	0	R/W_B

R/W_B=0: Write mode for register setting
R/W_B=1: Not available

SUB ADDRESS TABLE

Sub Address	Bit							
	D7	D6	D5	D4	D3	D2	D1	D0
00H	-	<1>SW1	<2>SW2	<3>Echo Volume				-
01H	<4>Feedback Volume			<5>Delay Time				0
02H	<6>ALC_dBV			<3>Sub Volume				-
03H	<7>Main Chan Volume							
04H	<7>Right & Left Chan Volume							
05H	-			<8>Main Chan Bass				
06H	-			<8>Right & Left Chan BASS				
07H	-			<8>Main Chan Treble				
08H	-			<8>Right & Left Chan Treble				
09H	-			<8>Main Chan Middle				

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DATA TABLE

<1>SW1 (Sub Address: 00H)

Gain	I²C Bus Control
	D6
No echo	0
Mixecho	1

<2>SW2 (Sub Address: 00H)

Gain	I²C Bus Control
	D5
No echo	0
Mixecho	1

<3>Echo Volume & Sub Volume(Sub Address: 00H,02H)

Gain	I²C Bus Control			
	D4	D3	D2	D1
Mute	0	0	0	0
-28dB	0	0	0	1
-26dB	0	0	1	0
-24dB	0	0	1	1
-22dB	0	1	0	0
-20dB	0	1	0	1
-18dB	0	1	1	0
-16dB	0	1	1	1
-14dB	1	0	0	0
-12dB	1	0	0	1
-10dB	1	0	1	0
-8dB	1	0	1	1
-6dB	1	1	0	0
-4dB	1	1	0	1
-2dB	1	1	1	0
0dB	1	1	1	1

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<4>Feedback Volume(Sub Address: 01H)(D0=0)

Gain	D7	D6	D5	D0
-2dB	0	0	0	0
-3dB	0	0	1	
-4dB	0	1	0	
-5dB	0	1	1	
-6dB	1	0	0	
-7dB	1	0	1	
-8dB	1	1	0	
Mute	1	1	1	

<5>Delay Time (Sub Address: 01H) (D0=0)

Gain	I²C Bus Control				
	D4	D3	D2	D1	D0
333ms	0	0	0	0	0
311ms	0	0	0	1	
289ms	0	0	1	0	
267ms	0	0	1	1	
245ms	0	1	0	0	
223ms	0	1	0	1	
200ms	0	1	1	0	
178ms	0	1	1	1	
156ms	1	0	0	0	
134ms	1	0	0	1	
111ms	1	0	1	0	
89ms	1	0	1	1	
67ms	1	1	0	0	
45ms	1	1	0	1	

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<6>ALC dBV(Sub Address: 02H)

Gain	I²C Bus Control		
	D7	D6	D5
ALC off	0	0	0
+3dBV	0	0	1
0dBV	0	1	0
-2dBV	0	1	1
-4dBV	1	0	0
-6dBV	1	0	1
-8dBV	1	1	0
-10dBV	1	1	1

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<7>Volume (Sub Address: 03H,04H)

Gain	I²C Bus Control							
	D7	D6	D5	D4	D3	D2	D1	D0
0dB	0				0	0	0	0
-1dB					0	0	0	1
-2dB					0	0	1	0
-3dB					0	0	1	1
-4dB					0	1	0	0
-5dB					0	1	0	1
-6dB					0	1	1	0
-7dB					0	1	1	1
-8dB					1	0	0	0
-9dB					1	0	0	1
-10dB					1	0	1	0
-11dB					1	0	1	1
-12dB					1	1	0	0
-13dB					1	1	0	1
-14dB					1	1	1	0
-15dB					1	1	1	1
0dB		0	0	0				
-16dB		0	0	1				
-32dB		0	1	0				
-48dB		0	1	1				
-64dB		1	0	0				
MUTE		1			-			
0dB	1	0			0	0	0	0
+1dB					0	0	0	1
+2dB					0	0	1	0
+3dB					0	0	1	1
+4dB					0	1	0	0
+5dB					0	1	0	1
+6dB					0	1	1	0
+7dB					0	1	1	1
+8dB					1	0	0	0
+9dB					1	0	0	1
+10dB					1	0	1	0
+11dB					1	0	1	1
+12dB					1	1	0	0
+13dB					1	1	0	1
+14dB					1	1	1	0
+15dB					1	1	1	1

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<8>Bass & Treble & Middle (Sub Address: 05H,06H,07H,08H,09H)

Gain	I²C Bus Control				
	D4	D3	D2	D1	D0
Cut					
● 0dB	0	0	0	0	0
-1dB		0	0	0	1
-2dB		0	0	1	0
-3dB		0	0	1	1
-4dB		0	1	0	0
-5dB		0	1	0	1
-6dB		0	1	1	0
-7dB		0	1	1	1
-8dB		1	0	0	0
-9dB		1	0	0	1
-10dB		1	0	1	0
-11dB		1	0	1	1
-12dB		1	1	0	0
-13dB		1	1	0	1
-14dB		1	1	1	0
-15dB		1	1	1	1
Boost					
0dB	1	0	0	0	0
+1dB		0	0	0	1
+2dB		0	0	1	0
+3dB		0	0	1	1
+4dB		0	1	0	0
+5dB		0	1	0	1
+6dB		0	1	1	0
+7dB		0	1	1	1
+8dB		1	0	0	0
+9dB		1	0	0	1
+10dB		1	0	1	0
+11dB		1	0	1	1
+12dB		1	1	0	0
+13dB		1	1	0	1
+14dB		1	1	1	0
+15dB		1	1	1	1

Notes:
1. ●: IT'S INITIAL SETTING WHEN VCC TURN ON.

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ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min.	Max.	Unit
Operating supply voltage		VCC	-	6	V
Latch up current		Iin	-100	+100	mA
ESD grade	Human body model	HBM	-4	+4	KV
	Machine model	MM	-0.4	+0.4	KV
Input voltage		Vin	-0.3	VDD+0.3	V
Operating temperature		Topr	-40	+85	℃
Storage temperature		Tstg	-65	+150	℃

RECOMMENDED OPERATING CONDITION

(Unless otherwise specified, Ta=25℃)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	VCC		3.0	5	5.5	V
Clock Frequency	fck	V_{CC}=5V	6.8	8	9.2	MHz
Low level input voltage	V_{IL}	V_{CC}=5V	0	-	0.9	V
High level input voltage	V_{IH}	V_{CC}=5V	2.25	-	5	V
Maximum clock frequency	f_{SCL}		-	-	100	KHz

QUICK REFERENCE DATA

Parameter	Symbol	Condition	Min	Typ.	Max.	Unit
Supply voltage	VCC		3.0	5	5.5	V
Clock Frequency	fck	V_{CC}=5V	6.8	8	9.2	MHz
Low level input voltage	V_{IL}	V_{CC}=5V	0	-	0.9	V
High level input voltage	V_{IH}	V_{CC}=5V	2.25	-	5	V
Maximum clock frequency	f_{SCL}		-	-	100	KHz
Main chan Total harmonic distortion (0.1Vrms,1KHz)	THD_MAIN	V_{CC}=5V,MICVOLIN->MICMIXOUT ,NO ECHO	-	0.01	0.03	%
RL chan Total harmonic distortion (0.1Vrms,1KHz)	THD_RL	V_{CC}=5V, LIN->LOUT or RIN->ROUT ,NO ECHO	-	0.01	0.03	%
Main chan Signal to noise ratio	SNR_MAIN	V_{CC}=5V,MICVOLIN->MICMIXOUT ,NO ECHO	-	100	-	dBV
RL chan Signal to noise ratio	SNR_RL	V_{CC}=5V, LIN->LOUT or RIN->ROUT ,NO ECHO	-	100	-	dBV
Channel separation (f=1KHz)	Sc	R to L or L to R channel	-	100	-	dB
Volume control 1dB step	-	-	-79	-	+15	dB
Bass & middle & treble control 1dB step	-	-	-15	-	+15	dB
Echo_vol & Sub_vol control 2dB step	-	-	-28	-	0	dB
Fb_vol control 1dB step	-	-	-8	-	-2	dB
Delay_time control 22ms step			45	-	333	ms

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Vcc=5V, f=1KHz ,Vi=0.1Vrms, VOLUME=0dB, ECHOVOL=0dB, FEEDBACKVOL=∞, BASS=0dB, MIDDLE=0dB, TREBLE=0dB, SUB_VOL=0dB,NO ECHO,fck=8MHz (fs=250KHz), Ta=25℃,Rg=0)

Parameter	Symbol	Test Condition	Min	Typ.	Max.	Unit
Total						
Supply voltage	VDD		3.0	5	5.5	V
Circuit current	ICC	No signal input	35	65	80	mA
Sampling frequency	fs	fs=133KHz	106.4	133	159.6	KHz
Microphone amplifier						
Total harmonic distortion	THD1	Vo=-17dBV, with ALC not operated	-	0.1	0.5	%
Total harmonic distortion	THD2	Vi=-27dBV, with ALC operated	-	3.65	6.0	%
ALC operating voltage measurement error	VoALC	Measurement: -10 to +3dBV	-3	0	+3	dB
ALC attack time	TALCAT	C=4.7μF	5	10	20	msec
ALC recovery time	TALCRE	C=4.7μF	0.9	1.2	1.6	sec
Maximum output voltage	VoMAX	THD=10%	5	5.7	-	dBV
Output noise voltage	No	Gv=37dB, BW=100 to 5KHz	-	-78	-67	dBV
Input impedance	Zi		50	100	200	KΩ
Digital echo						
Voltage gain	Gv	LPF1IN→LPF2OUT	-3.0	0	+3.0	dB
Total harmonic distortion	THD	LPF1IN→LPF2OUT, (TD=178mS)	-	0.5	1.2	%
Maximum output voltage	VoMAX	LPF1IN→LPF2OUT, THD=10%	0	2.5	3.5	dBV
Output noise voltage	No	DIN AUDIO	-	-90	-80	dBV
Mix out						
Voltage gain	Gv	MICVOLIN→MIXOUT, MIXECHO	-3	0	+3	dB
Total harmonic distortion	THD	MICVOLIN→MIXOUT, MIXECHO	-	0.02	0.1	%
Maximum output voltage	VoMAX	MICVOLIN→MIXOUT, THD=10%, MIXECHO	1	4	-	dBV
Output noise voltage	No	MICVOLIN→MIXOUT, MIXECHO	-	-97	-88	dBV
Volume						
Input resistance	Rin	-	70	100	130	KΩ
Max. gain	Gvmax	-	+14	+15	+16	dB
Max. attenuation	Avmax	-	-77	-79	-80	dB
Step resolution	Sstep	-	0.5	1	1.5	dB
Attenuation set error	Ea	step=+15~-50dB	-1	0	1	dB
		step=-51~-79dB	-1.5	0	1.5	dB
Mute attenuation	Amute	-	-85	-100	-	dB
Bass						
Control range	Crange	F=100HZ	±14	±15	±16	dB
Step resolution	Sstep	-	0.9	1	1.1	dB
Feedback resistance	Rb	-	37.7	53.9	70	KΩ
Middle						
Control range	Crange	F=1KHZ	±14	±15	±16	dB
Step resolution	Sstep	-	0.9	1	1.1	dB
Feedback resistance	Rb	-	37.7	53.9	70	KΩ
Treble						
Control range	Crange	F=20KHZ	±14	±15	±16	dB
Step resolution	Sstep	-	0.9	1	1.1	dB

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Parameter	Symbol	Test Condition	Min	Typ.	Max.	Unit
Sub_Volume						
Min. attenuation	Avmin	-	-1	0	1	dB
Max. attenuation	Avmax	-	-27	-28	-29	dB
Step resolution	Sstep	-	1.8	2	2.2	dB
Attenuation set error	Ea		-0.5	0	0.5	dB
Mute attenuation	Amute	-	-85	-100	-	dB
HeadPhone Driver						
Total harmonic distortion	THD	Po=100mW,RL=16Ω	-	0.02	0.05	%
Output Power	Hpo	THD=10%,F=1KHz,RL=16Ω	140	160	-	mW
Noise	Vno	Series RL chan	-	20	30	uV
Channel separation	Sc	R to L or L to R chan.	85	90		dB
Input low level	OE_{IL}		0	-	1	V
Input high level	OE_{IH}		2.6	-	5	V
Under voltage lock out	UVLO		2.55	2.75	2.95	V
General						
Main chan Total harmonic distortion	THD_MAIN	MICVOLIN->MICMIXOUT	-	0.01	0.03	%
RL chan Total harmonic distortion	THD_RL	LIN->LOUT or RIN->ROUT	-	0.01	0.03	%
Main chan Signal to noise ratio	SNR_MAIN	MICVOLIN->MICMIXOUT	-	100	-	dBV
RL chan Signal to noise ratio	SNR_RL	LIN->LOUT or RIN->ROUT	-	100	-	dBV
Main chan Max input level	Vimax_MAIN	THD=1%	1.1	1.25		Vrms
Main chan Max input level	Vimax_RL	THD=1%	1.1	1.25		Vrms
Main chan DC offset	Vos_MAIN	Vol from +15 to -79db	-	8	12	mV
RL chan DC offset	Vos_RL	Vol from +15 to -79db	-	8	12	mV
Channel separation	Sc	R to L or L to R chan.	-	100	-	dB
I^2C Bus						
Input low voltage	V_{IL}		0	-	0.9	V
Input high voltage	V_{IH}		2.25	-	5	V
Input current	I_{IN}	-	-5	-	+5	μA

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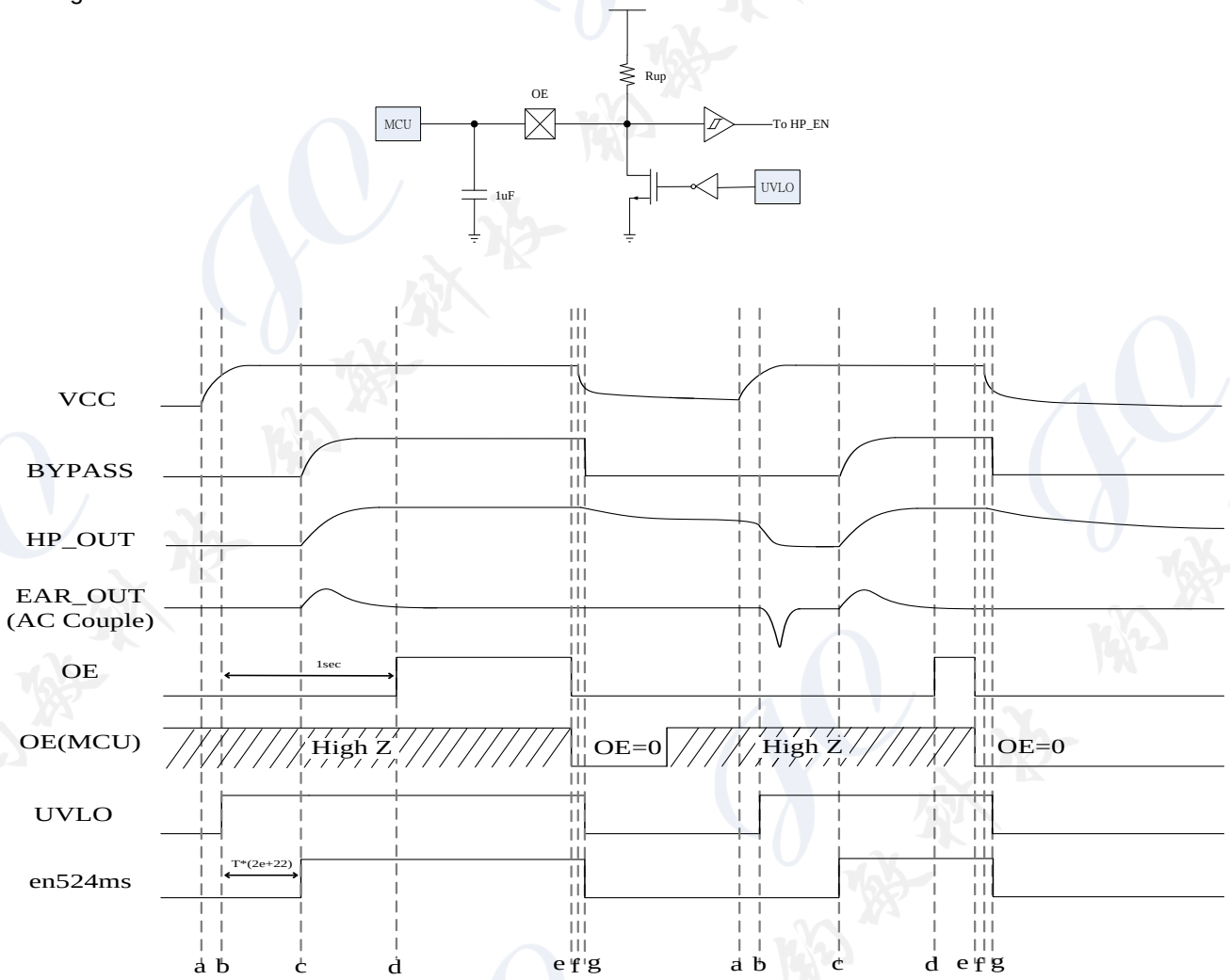
DEPOP

When power supply was applied,the chip default setting is muted,add a cap to the OE could extend mute time to avoid any pop noises happen,when power off,the UVLO will disable the HeadPhone driver to reduce pop noises,For better depop result to avoid pop noises after power off before UVLO,the OE can control by MCU,when power down,OE=0 else OE=high Z.



POWER ON and OFF timing Sequence

a:power on
b:UVLO pull high(start calculate 524ms)
c: after UVLO 524ms(for HP_OUT pull low)
d:OE pull high(enable HP)
e:MCU control OE pull low(disable HP)
f:power off
g:UVLO pull low(disable HP)

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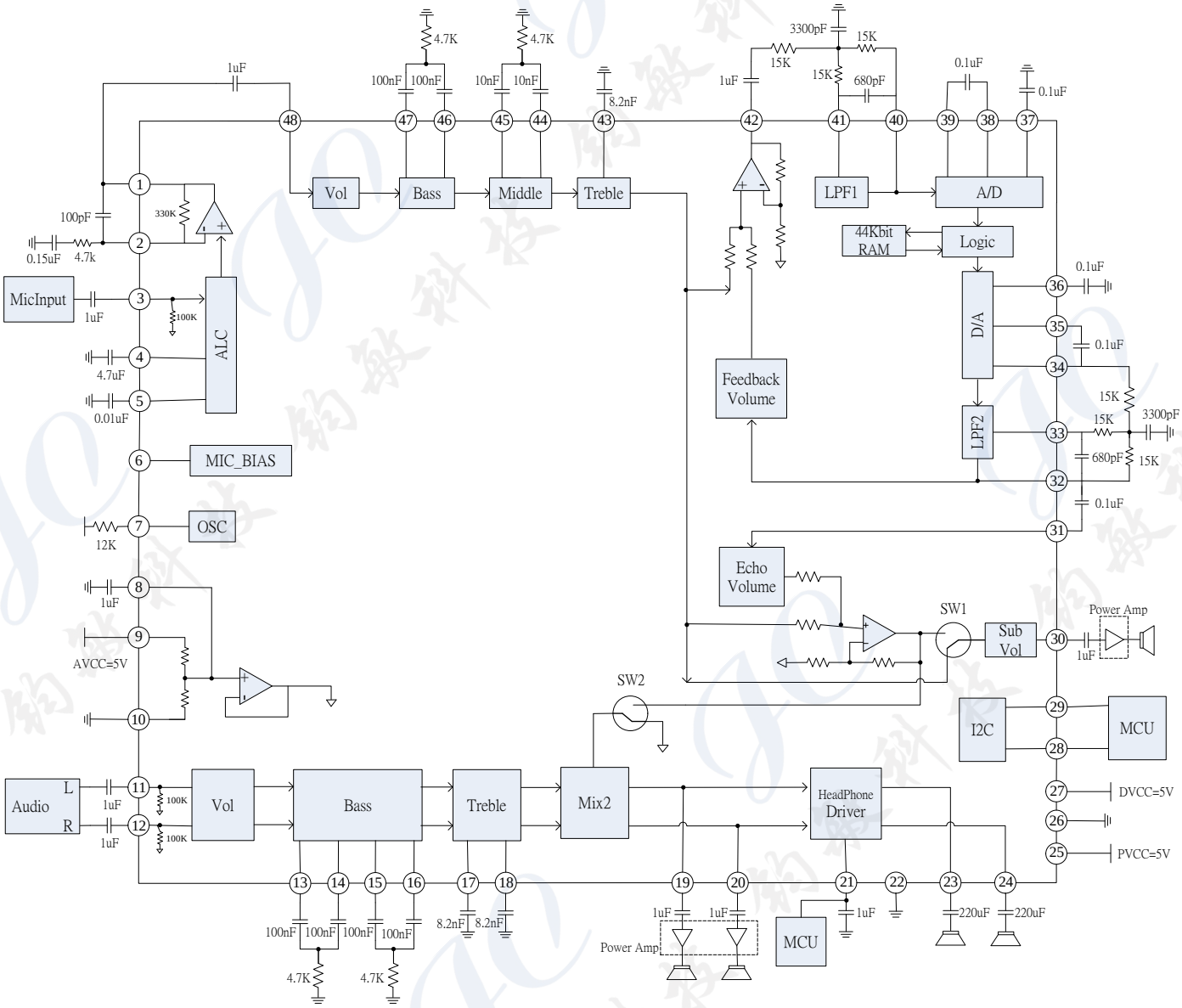
APPLICATION EXAMPLE

LQFP48



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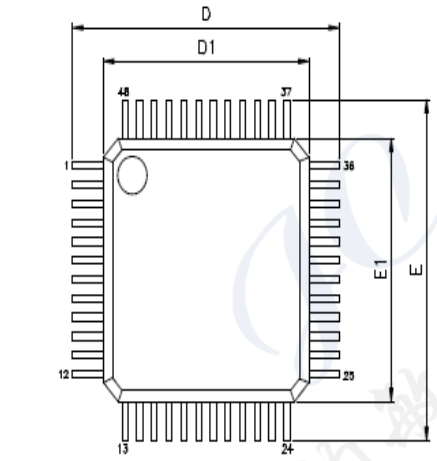
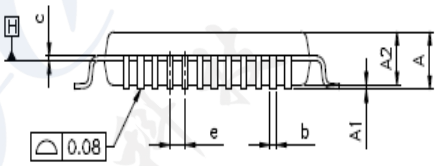
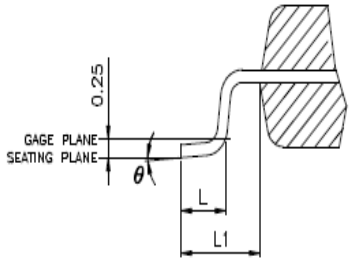
PACKAGE INFORMATION

48 PINS, LQFP, 300MIL

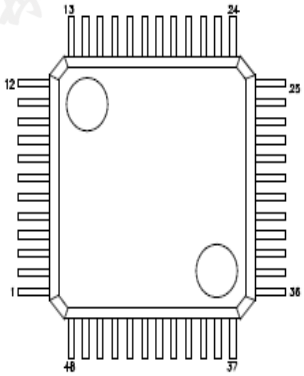


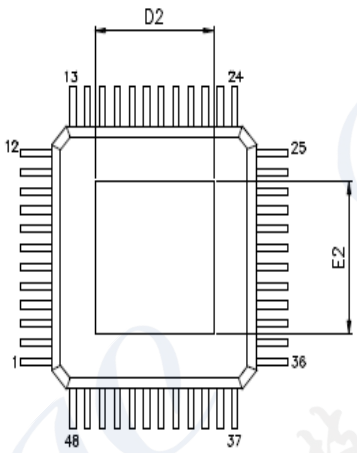




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°





THERMALLY ENHANCED VARIATIONS ONLY

2 THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
205X20E	4.31	5.21	4.31	5.21

NOTES:
1.JEDEC OUTLINE :
MS-026 BBC
MS-026 BBC-HD(THERMALLY ENHANCED VARIATIONS ONLY)
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.