DESCRIPTION

The PT2469 is a monolith integrated motor driver designed for printers, scanners, and home and office automated equipment. The two H-bridge drivers can drive a bipolar stepper motor or two DC motors. The output H-bridge driver is consists by all of N-channel MOSFET. The PT2469 is allows driving up to 1.6A maximum output current (VM=24 V, Ta=25°C).

An EN-PH type parallel logic control interface can be configuring the output switches ON-OFF of H-bridge, and motor current decay mode is also programming by the parallel input port.

The PT2469 is available in a 28-pin HTSSOP package with thermal pad and in a 28-pin QFN package thermal pad.

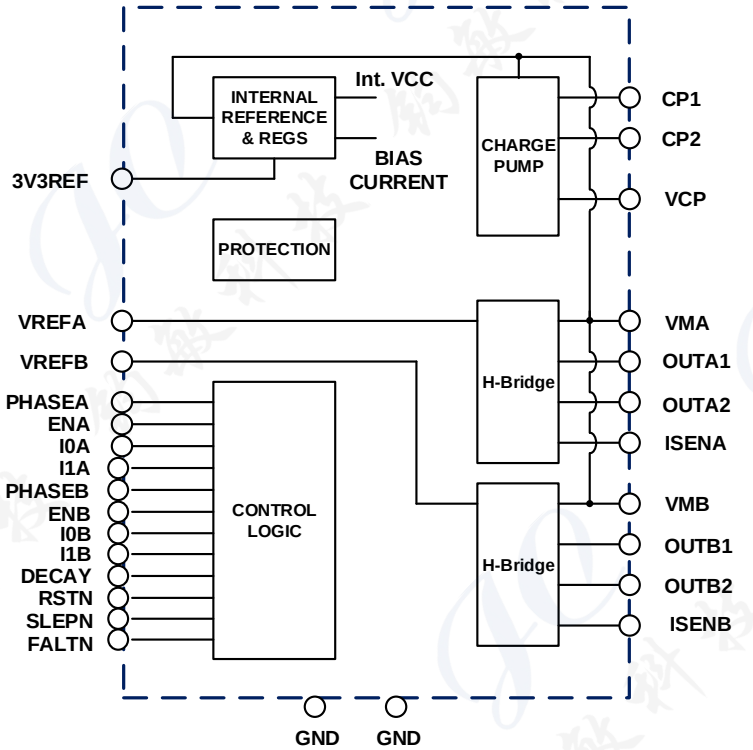
FEATURES

- 8.2-V to 40-V Supply Voltage Range
- 1.6-A Maximum Driving Current at VM=24V (with additional heatsink)
- EN-PH Control Logic Interface
- Dual H-Bridge Driver with 4 Level PWM Current Control.
- Winding Current Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Drives Single Bipolar Stepping Motor or Dual DC Motors
- Built In a 3.3V Reference Voltage Output
- Low-Power Sleep Mode
- Protection Features
  - Over Current Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Under Voltage Lock Out (UVLO)
  - Fault Indication Pin (FAULTN)

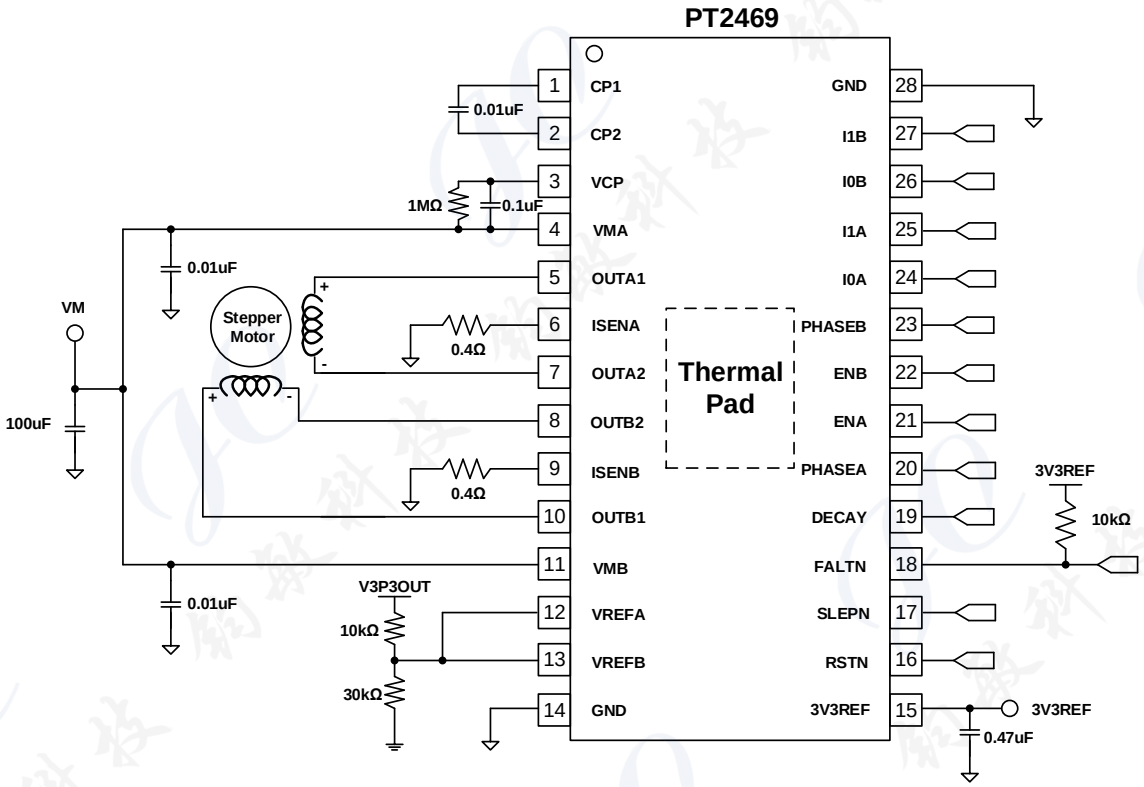
APPLICATIONS

- Automatic Teller Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Amusement Machines
- Factory Automation
- Robotics

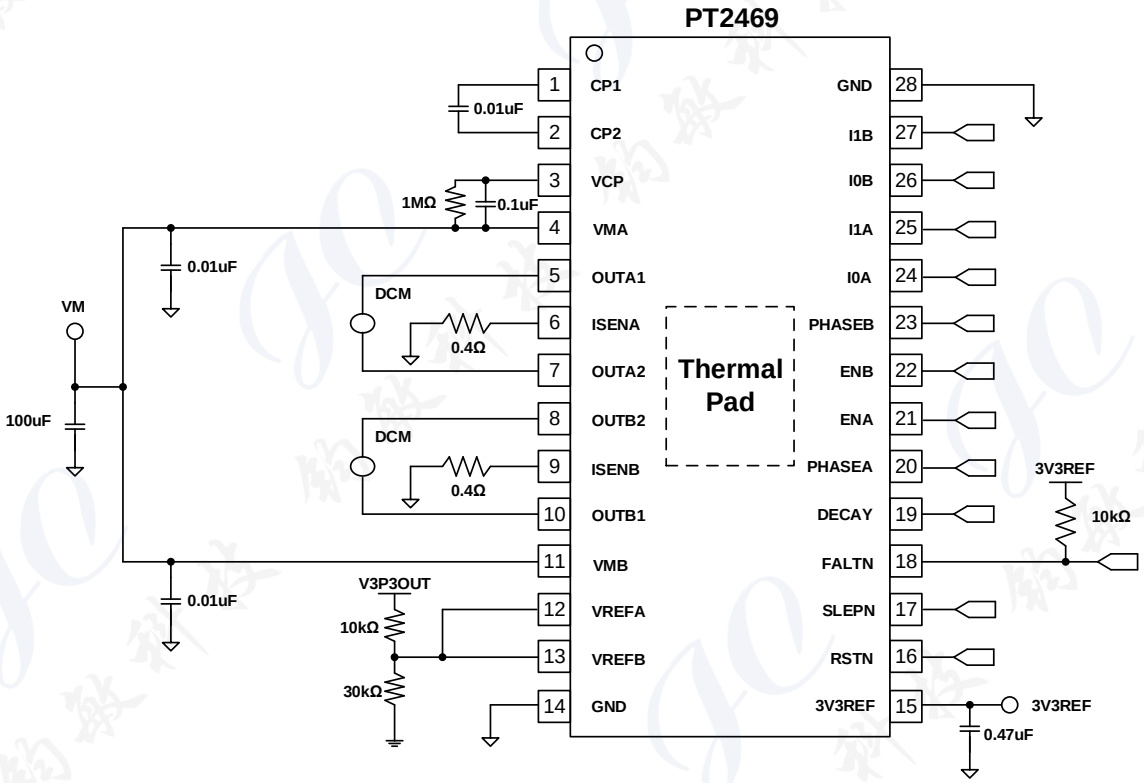
BLOCK DIAGRAM



APPLICATION CIRCUIT



Drives a bipolar stepping motor



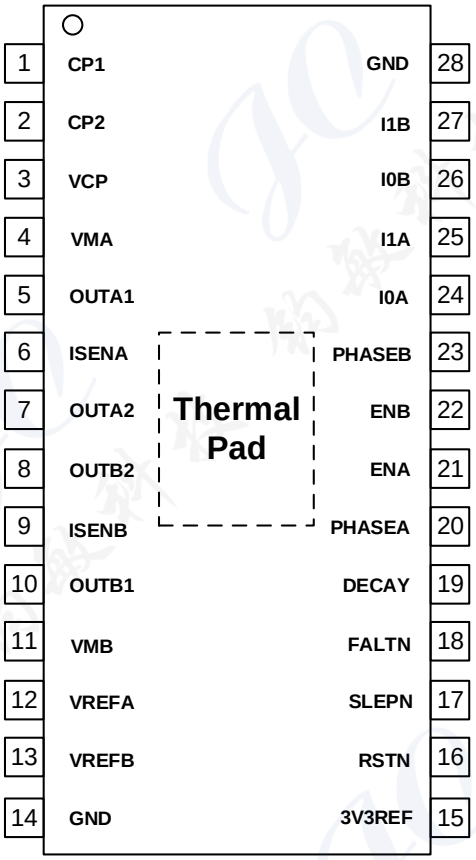
Drives two DC brushed motor

ORDER INFORMATION

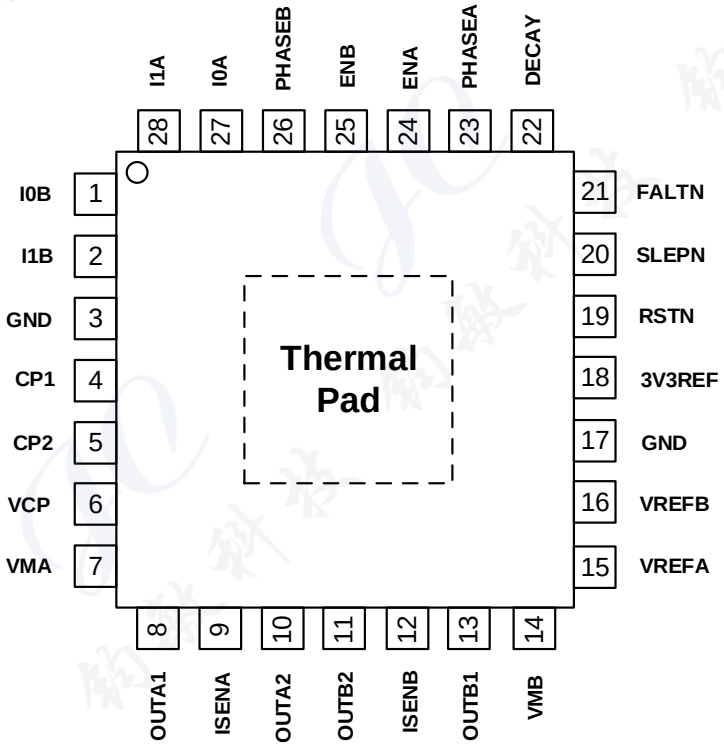
Valid Part Number	Package Type	Top Code
PT2469-HT	28 Pins, HTSSOP	PT2469-HT
PT2469	28 Pins, QFN	PT2469

PIN CONFIGURATION

HTSSOP



QFN



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			HTTSSOP	QFN
CP1	I	External flying capacitor for charge pump, Connect a 0.01μF/50V low-ESR ceramic capacitor between CP1 and CP2.	1	4
CP2	I		2	5
VCP	O	High-side gate drive supply voltage (Connect a 0.1μF/50V ceramic capacitor and a 1MΩ resistor to VM.)	3	6
VMA	-	H-Bridge A power supply	4	7
OUTA1	O	H-Bridge A output 1	5	8
ISENA	I	H-Bridge A current sense / GND	6	9
OUTA2	O	H-Bridge A output 2	7	10
OUTB2	O	H-Bridge B output 2	8	11
ISENB	I	H-Bridge B current sense / GND	9	12
OUTB1	O	H-Bridge B output 1	10	13
VMB	-	H-Bridge B power supply	11	14
VREFA	I	H-Bridge A current set reference input	12	15
VREFB	I	H-Bridge B current set reference input	13	16
GND	-	Device ground	14	17
3V3REF	O	3.3V reference voltage output	15	18
RSTN	I	Reset input (L=Initialize all of internal logic registers and disables H-bridge outputs)	16	19
SLEPN	I	Sleep mode input (H=device enable, L=low-power sleep mode)	17	20
FALTN	O	Fault, Logic low when fault condition appear (OCP, OTP)	18	21
DECAY	I	Decay mode (Low = slow decay, open = mixed decay, high = fast decay)	19	22
PHASEA	I	H-Bridge A phase (H=AOUT1 high, AOUT2 low)	20	23
ENA	I	H-Bridge A enable (H=H-bridge A output active)	21	24
ENB	I	H-Bridge B enable (H=H-bridge B output active)	22	25
PHASEB	I	H-Bridge B phase (H=BOUT1 high, BOUT2 low)	23	26
I0A	I	H-Bridge A current set (Sets H-bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0%)	24	27
I1A	I		25	28
I0B	I	H-Bridge B current set (Sets H-bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0%)	26	1
I1B	I		27	2
GND	-	Device ground	28	3

FUNCTION DESCRIPTION

PWM MOTOR DRIVERS

The PT2469 includes two H-bridge drivers with PWM current regulation circuitry. A block diagram of the system control circuitry is shown in Figure 1, it's connects a bipolar stepper motor for example, but drives two separate DC motors is also possible.

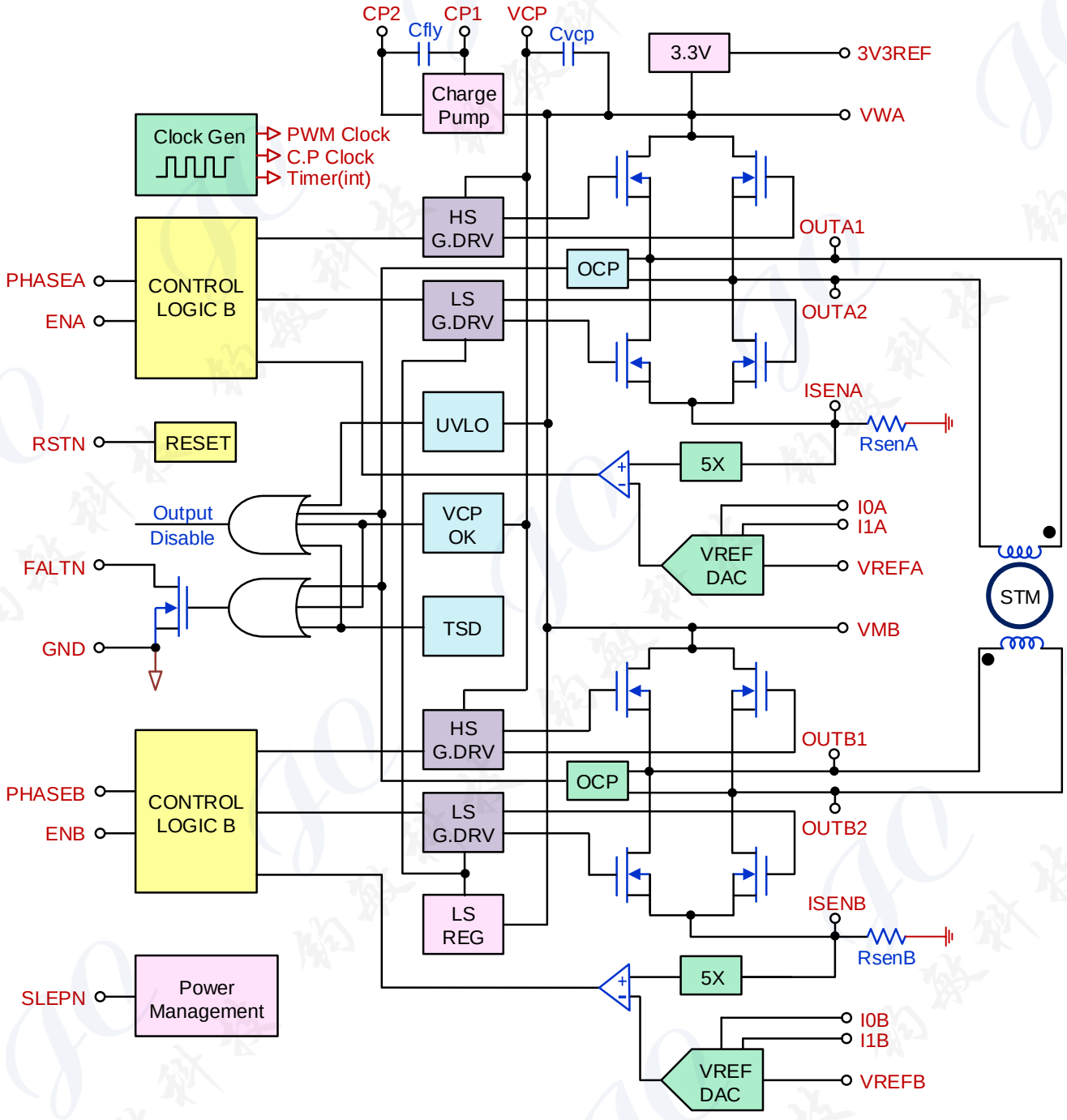


Figure 1. Motor Control Circuitry

The multiple motor power supply pins (VMA and VMB) must be tight together to single supply voltage node on PCB.

H-BRIDGE OUTPUT CONFIGURATION

The output current direction of the H-bridge driver is controlled by PHASEx pins, and ENx pin is controls the H-bridge driver enable or not. Refer to the Table 1 for the I/O logic corresponds.

ENx	PHASEx	OUTx1	OUTx2
0	X	HiZ	HiZ
1	1	H	L
1	0	L	H

Table 1. H-Bridge Output Configuration

PWM CHOPPING CURRENT REGULATION

The motor windings current is regulated by a fixed-frequency PWM chopping, when the H-bridge is enabled, the winding current flows through the switches FET of H-bridge and direction determinate by PHASEx setting. The slew rate of winding current is depends on the VM voltage and inductance of the winding. Once the current reaches the current chopping threshold, the H-bridge FET will be disabled and decay mode setting will handles current decay behavior.

For a stepping motor, PWM current regulation is often used to maintain the winging current level and helps motor torque steady, and chopping current divider can be used on micro-stepping motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

A comparator is used to sets the chopping current level, first the voltage across an external current sense resistor connected to the ISENx pins will multiples by 5, and compare with VREFx voltage input. The VREFx input voltage is scaled by a 2-bit DAC that allows current settings from 100%, 71%, 38% of full-scale, and down to zero.

Each H-bridge has own VREFx DAC setting inputs (I0x and I1x). The voltage applied to the PWM current comparator is derives from VREFx DAC output, and VREFx DAC output is scaling from VREFx input and divide ratio determinates by logic states of the I0x and I1x, in Table 2 shows bit definition. The H-bridge will be disabled flows when both I0x and I1x bits in logic Hi state.

I1x	I0x	VREFx DAC Current Ratio (% Full-Scale Chopping Current)
1	1	0% (H-bridge disabled)
1	0	38%
0	1	71%
0	0	100%

Table 2. PWM Chopping Current VS VREFx DAC Bit Definition

The PWM chopping current is calculated in Equation 1.

$$\mathbf{I_{CHOP}} = \frac{\mathbf{V_{REFX}} \times \mathbf{DAC\ ratio}}{\mathbf{5} \times \mathbf{R_{ISENSE}}} \qquad \text{Eq.(1)}$$

Example 1:

If a 0.5Ω sense resistor is used and the VREFx pin is 2.5 V, and VREFx ratio is sets to 100% of full scale chopping current level (I0x=H, I1x=H) , the output current will be :

(2.5 V x 100%) / (5 x 0.5 Ω) = 1.0A.

Example 2:

If a 0.2Ω sense resistor is used and the VREFx pin is 1.5V, and VREFx ratio is sets to 38% of full scale chopping current level (I0x=L, I1x=H) , the output current will be :

(2.5 V x 38%) / (5 x 0.2 Ω) = 0.95A.

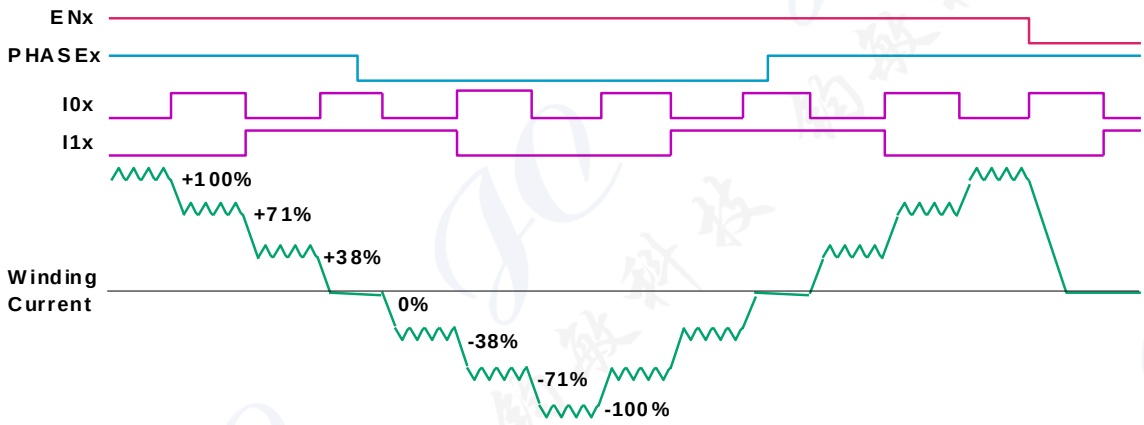


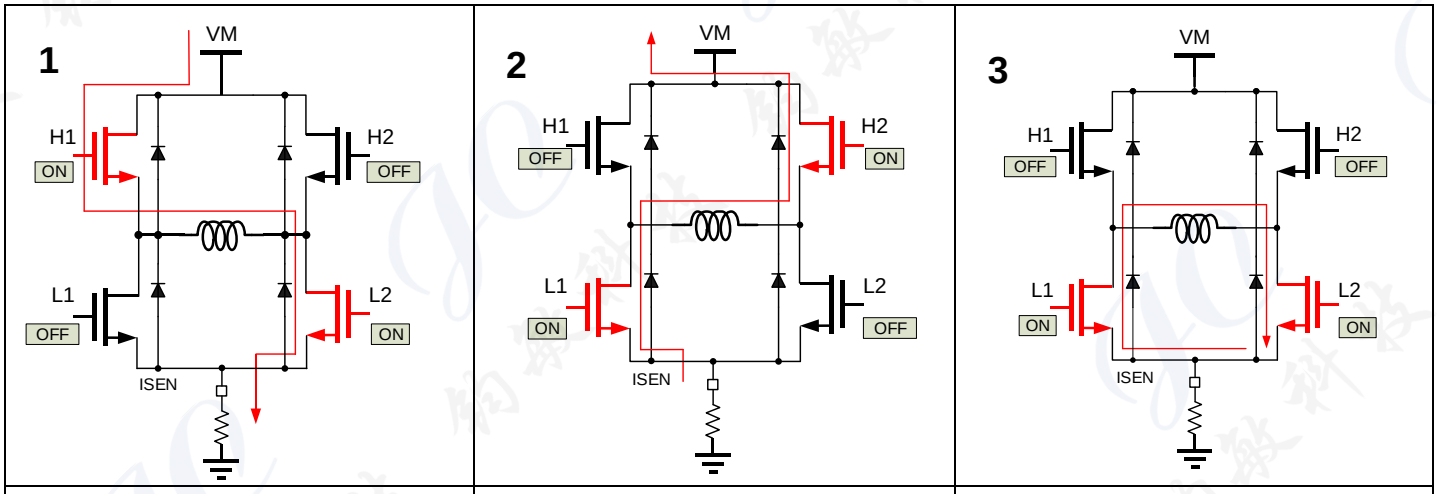
Figure 2. PWM Chopping Current with VREFx DAC Bit Setting

DECAY MODE

The motor winding current in PWM chopping cycle is determinates by the voltage on the DECAY pin. In charge phase the winding is excitation by H-bridge output current, the winding current through the current sense resistor on the ISENx pin presents a voltage drops and H-bridge will leaves charge mode if reaches desire comparator threshold, and next step of H-bridge will goes to one of three mode, fast, slow or mixed decay, depends on DECAY pin logic status, please refer to the Table 3. The DECAY sets will apply to both H-bridges simultaneously, and Figure.3 shows the current direction in different decay mode and Figure 4 shows mixed decay sequence waveform.

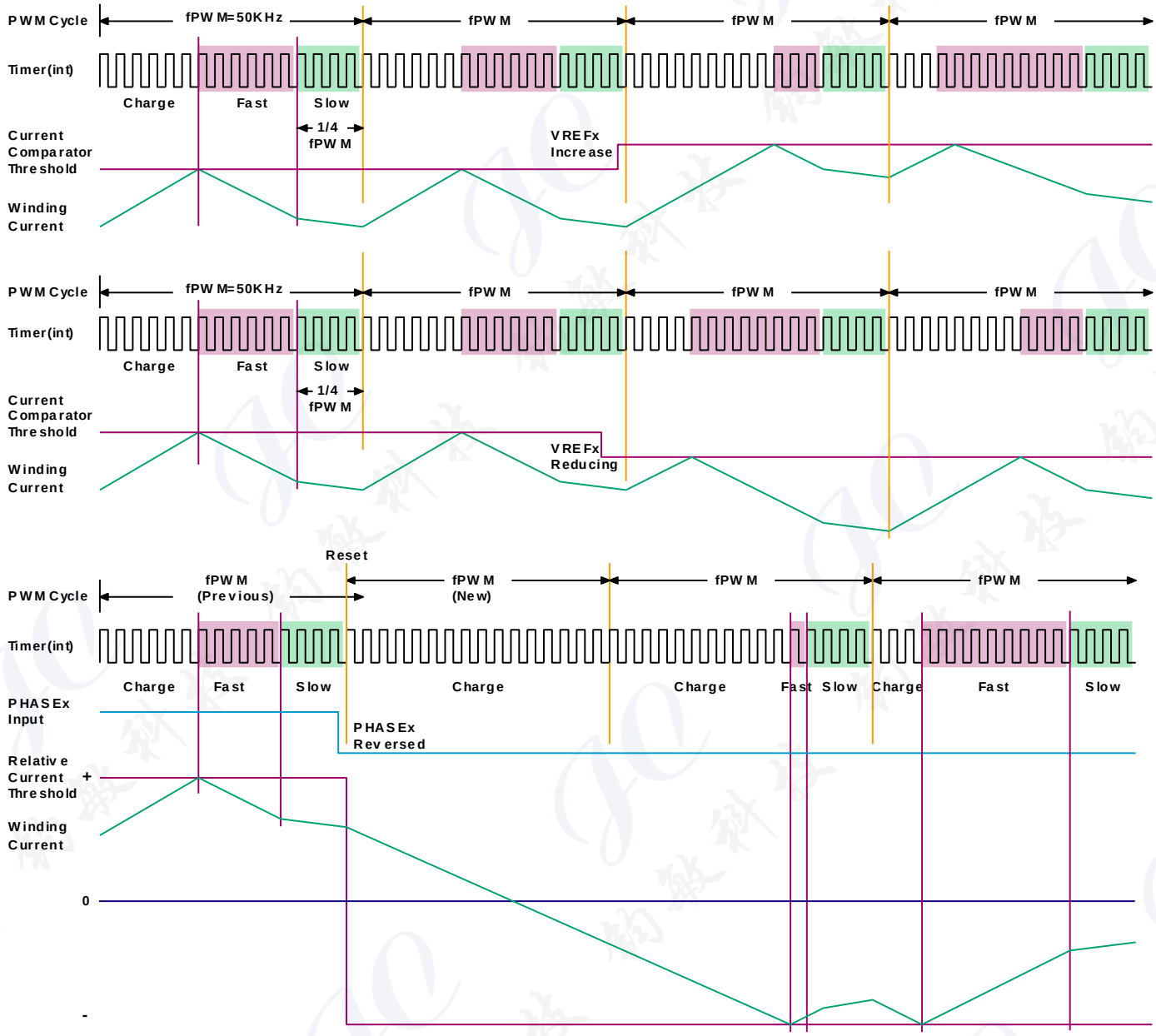
Decay Pin Level	DECAY Pin Logic	Decay Mode
<0.6V	L	Slow
OPEN	FLOAT	Mixed
>2V	H	Fast

Table 3. DECAY Mode Setting



Charge	Fast Decay	Slow Decay
Turn on H1 and L2, the winding current through the H-bridge from VM to GND. When comparator threshold, is reached, the charge mode will be goes to next step.	Turn on L1 and H2, The reversed polarity of H-bridge will force winding current reduced quickly. The current sense circuits will turns-off fast decay mode if current reaches to zero.	Turn on L1 and L2 both, the circulate winding current is flows in the low side loop.(synchronous rectifier)

Figure 3. Mixed Decay Mode Switching Sequence (Forward mode only)



(Timer(int) is an internal clock management block uses to drives charge pump and PWM switching cycles, timing clock is only for realize mixed decay operation, not an exactly clock)

Figure 4. Mixed Decay Sequence Waveform

RESET and LOW POWER SLEEP MODE

Pull the RSTN pin to logic low state, the status of all control pins (except SLEPN) will be ignore and internal control circuit will be reset to initial state, the H-bridge output also disabled during RESTN in low state, in the meantime the 3.3V voltage reference and charge pump still works.

Pull the SLEPN pin to logic low will force the chip into a low power sleep mode. During sleep mode is active the H-bridges outputs are disabled, and analog circuit such like charge pump for HS gate driver, 3.3V voltage reference (3V3REF) and internal clocks blocks are all stopped. In this mode all inputs are ignored until SLEPN returns to logic high state. When chip is wakes up from the low power sleep mode, a short waiting time (less than 1mS) before H-bridge becomes to normal operation is required because of charge pump starting time.

BLANKING TIME

During PWM chopping current is flows after the H-bridge enable, the current signal can be picked-up in the sense resistor connected in ISENx pins, the signal will delivers to comparator after a fixed delay time to avoid noises or current spike causes fault-triggered. The blanking time is fixed at 3.2μS and it also sets a limit to the duty cycle of PWM in charge period, the minimum on-duty will not less than around 16% in a 50KHz PWM frequency.

PROTECTION CIRCUITS

The PT2469 have fully protection function to against miss-operation events.

◆ OVERCURRENT PROTECTION (OCP)

Overcurrent detection circuit will always monitor all of output pins current during H-bridge is enabled, this operation is independent from PWM chopping. If any output pin is connected to VM, GND or across load shorted, the inrush high current will be detected by OCP circuit and immediately turn off both H-bridge outputs after blanking time. The chip will remain disabled until either RSTN pin is toggle once or power down the VM supply and apply again.

If an output pin connects to the VM, the short circuit current will be passing through the low side MOSFET and current sense resistor to GND, to avoid sense resistance interference OCP detection, it should not be higher than a certain range, for example, 0.5Ω or less is recommended.

◆ THERMAL SHUTDOWN (TSD)

If the chip temperature exceeds preset 160℃, all of MOSFET of H-bridge will be turn off and the FALTN pin will be pull down, an external pull up resistor may needed to detects FALTN logic state by MCU I/O pin. Once the chip temperature is cooling down to below hysteresis window, H-bridge outputs will be enabled again.

◆ UNDERVOLTAGE LOCKOUT (UVLO)

In Any time the VM pin voltage drops below the under voltage lockout threshold voltage, all circuitry in the chip will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

◆ FAULT INDICATION (FALTN)

Whatever which condition is happens, the OCP, TSD or charge pump voltage failed, the open-drain FALTN pin will pull down immediately and remains until RSTN pin re-toggled or VM voltage re-applied. FALTN could connects to MCU I/O port for error reporting with a pull high resistor to the 3V3REF or 5V logic supply.

POWER SUPPLY CAPACITOR RECOMMENDATIONS

Consider a real world application scenario; the motor driver is designed to drives high inductance load such like motor winding or solenoid coil. If a H-bridge turns-off all of outputs during inductor current still flowing, because the inductor current would not be reset immediately, the rest of free-wheel current would re-directs and passing through the body diode of the output FET and runs into VM supply and final decay to zero after de-magnetization time. This reverse current depends on load inductance, inductor current and re-generates current from the motor due to inertia of rotor.

In another case, the parasitic reactance (inductance + resistance) of power wire between the power supply and motor driver board with parasitic capacitance of PCB consists a LC resonates tank, during power supply sourcing current to the motor driver board, the VM voltage may drops quickly and parasitic LC will be trigged and shows oscillation spike if the local bypass capacitor is not sufficient.

To prevent unstable bounce or spike appears on VM bus, a high capacitance bounce absorber capacitor (>100μF) should be placed on VM bus line, it could absorb re-generates free-wheels current during DC motor brake and stabilize VM voltage during high forward/reverse motor current sources. A small MLCC 0.1μF bypass capacitor should be placed near the motor driver IC power pin, VM and 3V3REF both, to reduce the spike causes by power line LC resonates.

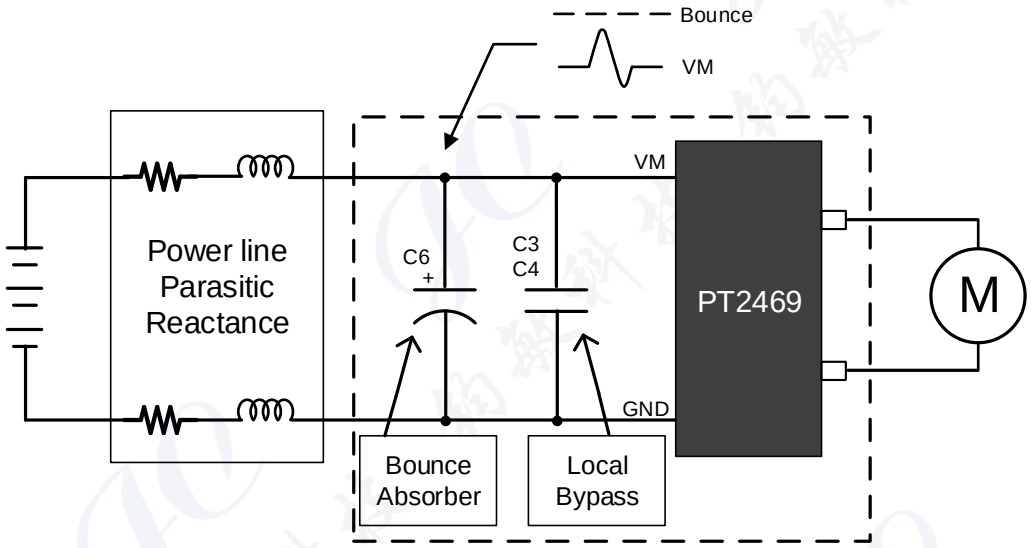
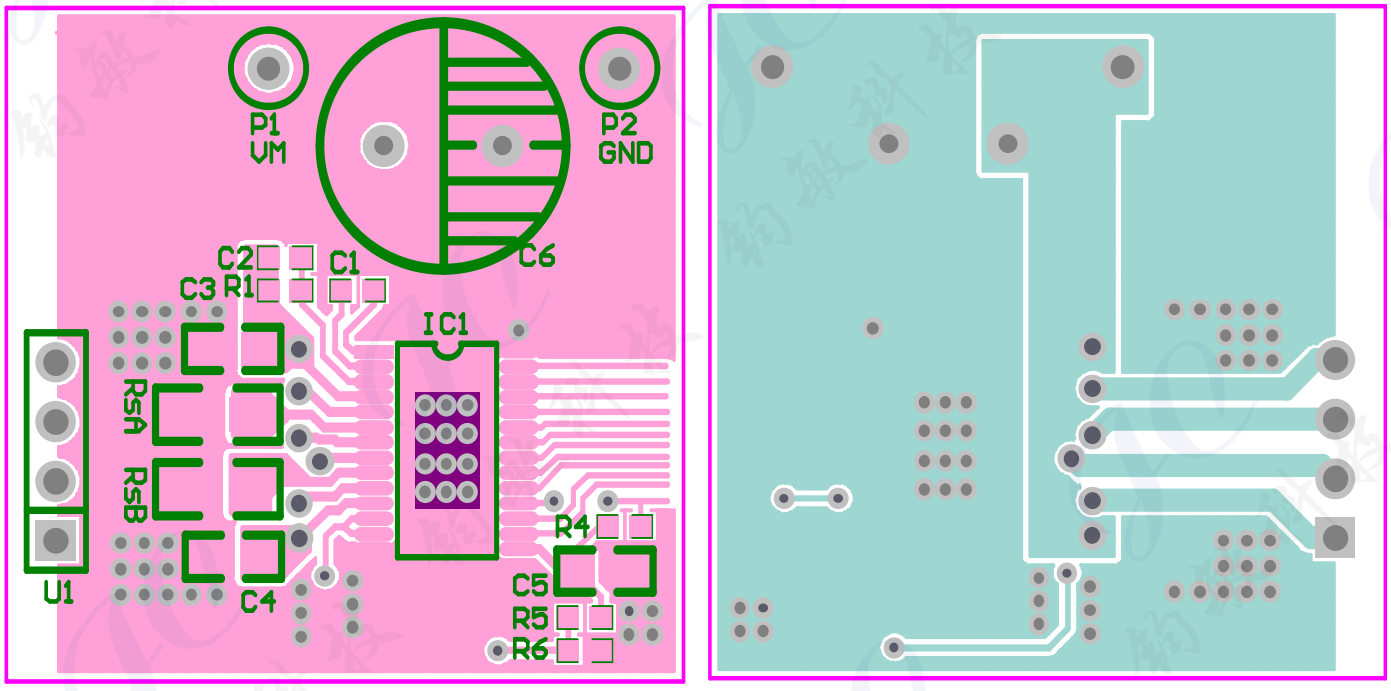


Figure 3. Motor Driver System with External Power Supply

PCB LAYOUT RECOMMENATION

The local bypass capacitor C3 and C4 should be placed near the IC power pins, and bounce absorber capacitor C6 should be placed on VM bus line. The GND plane should be placed on the component side under the chip as a low impedance power trace, and larger area of GND plane and wider cooper trace reduce the thermal resistance (θ_{JA}). The thermal pad under TSSOP and QFN package should be soldered to the PCB component side and connects to the bottom side through via holes, this arrangement can further enhance the heat dissipation.



Top Side Bottom Side

Figure 5. Simplified Layout Example (for HTSSOP package)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VMx	0	42	V
Digital Pin Voltage	xPHASE/xENBL	0	5	V
VREF Input Voltage	xVREF	0	4	V
Output Current	Iout	0	1.6	A
Operating Temperature	Topr	-40	85	°C
Storage Temperature	Tstg	-40	150	°C
ESD, Human Body Model	HBM	-2000	+2000	V
ESD, Machine Model	MM	-200	+200	V

PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	HTSSOP (28 PINS)	VQFN (28 PINS)	Unit
From chip conjunction dissipation to external environment	Rja	Ta=25°C	38.9	35.8	°C/W
From chip conjunction dissipation to package surface	Rjc		23.3	25.1	

RECOMMENED OPERATING CONDICTION

Parameter	Symbol	Min	Typ	Max	Unit
Motor Power Supply Voltage Range	V_M	8.2	24	40	V
VREFx Input Voltage	V_{REF}	1	-	3.5	V
3V3REF Load Current	I_{3V3}	-	-	1	mA

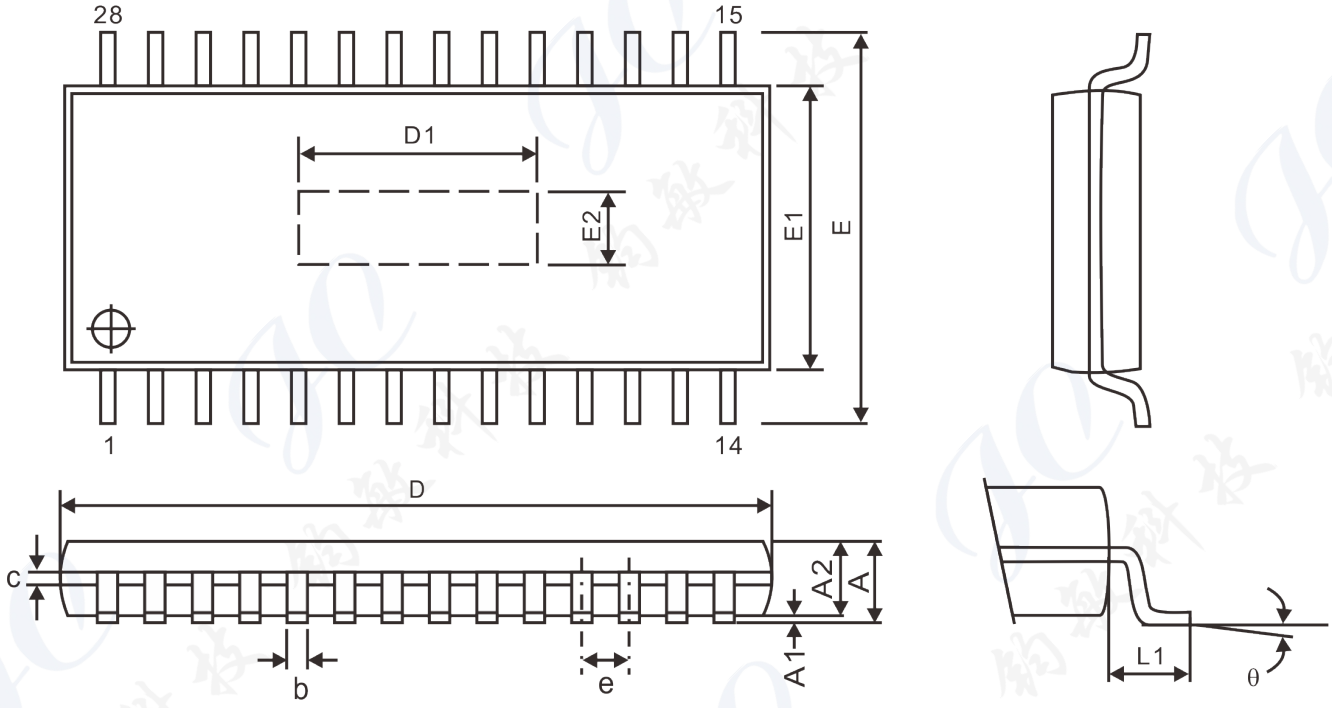
ELECTRICAL CHARACTERISTIC

TA=25°C , VM=24V ,over operating free-air temperature range (unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Current	I_M	V_M=24V, f_{PWM}<50Hz		7	10	mA
		V_M=24V, Sleep mode		20	30	μA
Under Voltage Lock Out	UVLO	V_M rising		7.8	8.2	V
V3P3OUT REGULATOR						
V3P3OUT Voltage	V3P3	IOUT = 0 to 1mA,VM=24V	3.18	3.30	3.42	V
LOGIC LEVEL INPUTS						
Digital Input High Level	V_{IH}		2		5.25	V
Digital Input Low Level	V_{IL}			0.6	0.7	V
Input Hysteresis	V_{HYS}			0.5		V
Input High Current	I_{IH}	VIN = 3.3 V			100	uA
Input Low Current	I_{IL}	VIN = 0	-20		20	uA
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
Output Low Voltage	V_{OL}	IO = 5mA			0.5	V
Output High Threshold	I_{OH}	VO = 3.3 V			1	uA
DECAY INPUT						
Input High Threshold Voltage	V_{IH}	For fast decay mode	2			V
Input Low Threshold Voltage	V_{IL}	For slow decay mode	0		0.6	V
Input Current	I_{IN}	-			±40	uA
H-BRIDGE FETS						
HS FET on Resistance	$R_{DS(ON)}$	V_M = 24V, I_O = 1A , T_J = 25°C		0.63		Ω
		V_M = 24V, I_O = 1A , T_J = 85°C		0.76		Ω
LS FET on Resistance	$R_{DS(ON)}$	V_M = 24V, I_O = 1A , T_J = 25°C		0.65		Ω
		V_M = 24V, I_O = 1A , T_J = 85°C		0.78		Ω
Off-State Leakage Current	I_{OFF}		-20		20	uA
MOTOR DRIVER						
Internal PWM Frequency	f_{PWM}			50		kHz
Current Sense Blanking Time	t_{BLANK}			3.2		us
Rise Time	t_R	V_M =24V	100		360	ns
Fall Time	t_F	V_M =24V	50		250	ns
Dead Time	t_{DEAD}			70		ns
Input Deglitch Time	t_{DEG}		1.3		2.9	us
PROTECTION CIRCUITS						
Overcurrent Protection Trip Level	I_{OCP}		1.8		5	A
Thermal Shutdown Temperature	t_{TSD}	Die temperature	150	160	180	°C
CURRENT CONTROL						
xVREF Input Current	I_{REF}	xVREF = 3.3V	-3		3	uA
xISENSE Trip Voltage	V_{TRIP}	xVREF = 3.3V, 100% current setting	635	660	685	mV
		xVREF = 3.3V, 71% current setting	445	469	492	mV
		xVREF = 3.3V, 38% current setting	225	251	276	mV
Current Sense Amplifier Gain	A_{ISENSE}	Reference only		5		V/V

PACKAGE INFORMATION

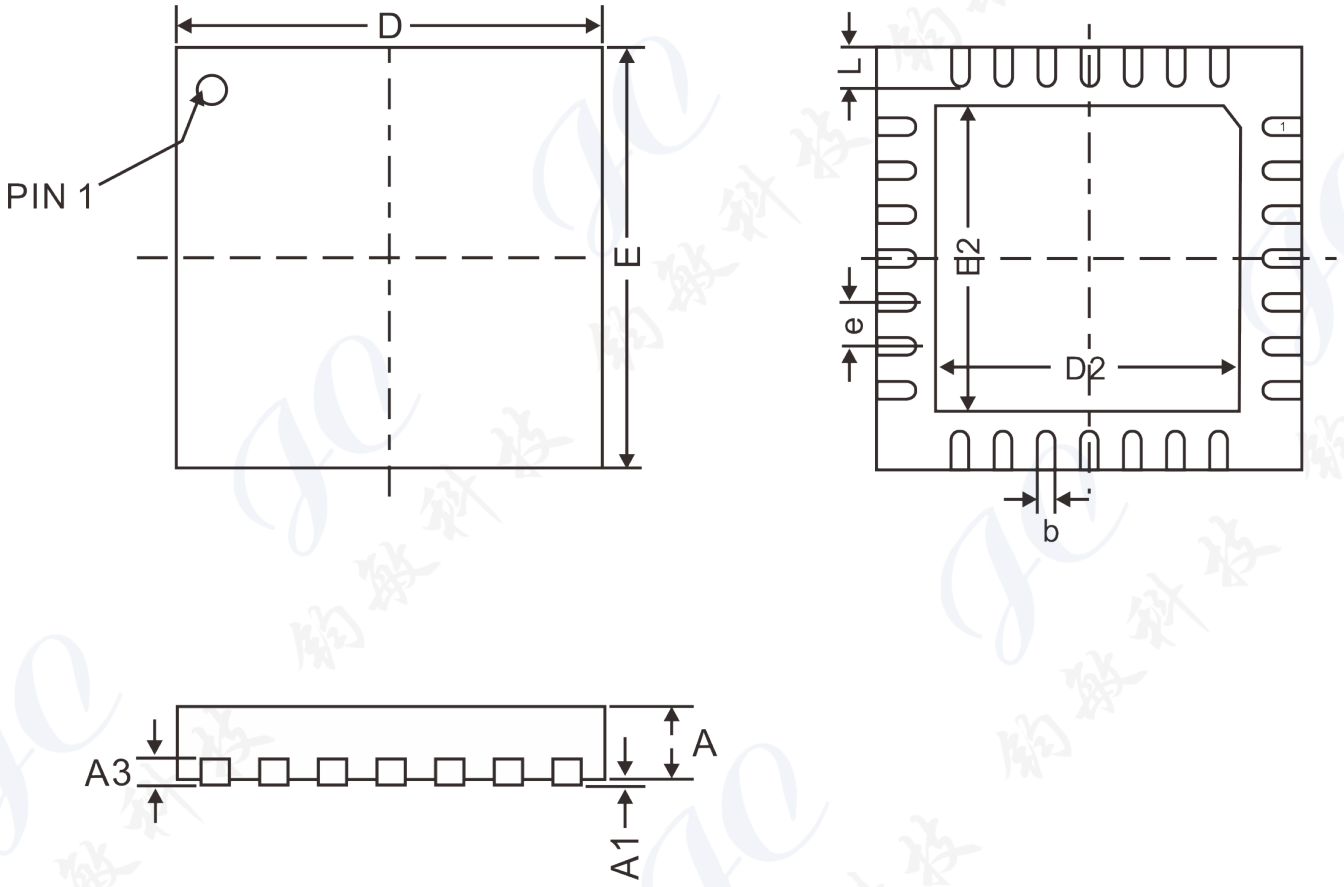
28-PIN, HTSSOP, 173MIL



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
b	0.19	-	0.30
c	0.09	-	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E		6.4 BSC.	
e		0.65 BSC.	
D1	4.41	-	5.51
E2	2.40	-	3.00
L1		1.00 REF	
θ	0°	-	8°

Notes:
1. All dimensions refer to JEDEC MO-153 AET

28-PIN, QFN, 5X5



Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	-	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC.		
D2	3.20	3.25	3.30
E	5.00 BSC.		
E2	3.20	3.25	3.30
e	0.50 BSC.		
L	0.50	0.55	0.60

Notes:
1. All dimensions refer to JEDEC MO-220 WHHD-1

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