DESCRIPTION

The PT2485 is a monolith integrated motor driver designed for printers, scanners, and home and office automated equipment. The single H-bridge drivers can drives a DC brushed motor or single winding of a bipolar stepping motor. The output H-bridge driver is consists by all of N-channel MOSFET, and allows driving up to 5A maximum peak output current (VM=24 V, Ta=25°C).

The phase and enable, industrial standard control logic interface is very versatile to configuring the H-bridge output switches with 32 levels PWM current regulation, it is useful to limiting the starting current of the DC brushed motor; or determinate the winding current of a stepping motor. The motor current decay mode also programmable by a tristate input pin.

The PT2485 is available in a 28-pin HTSSOP package with thermal pad.

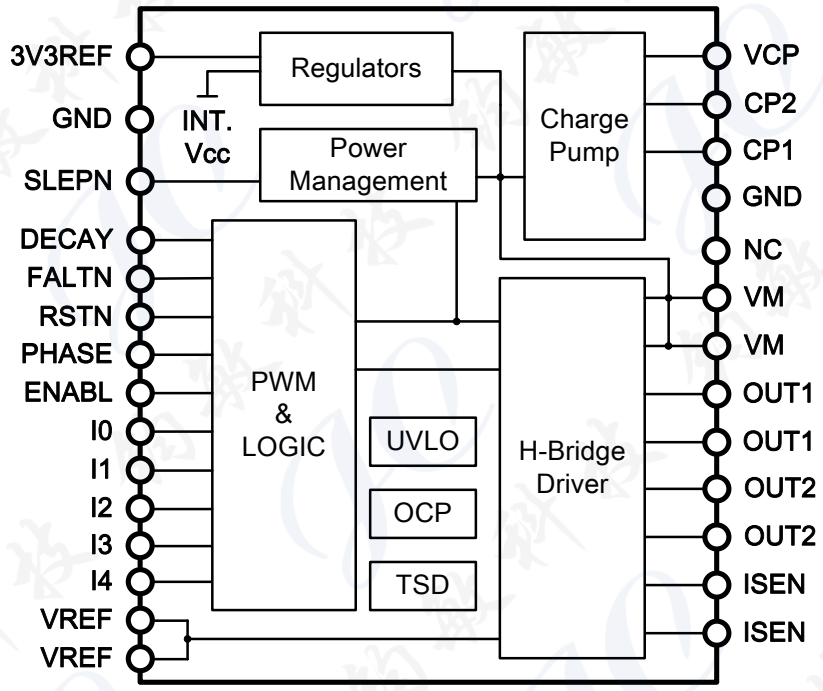
APPLICATIONS

- Automatic Teller Machines
- Printers
- Scanners
- Office Automation Machines
- Amusement Machines
- Factory Automation
- Robotics

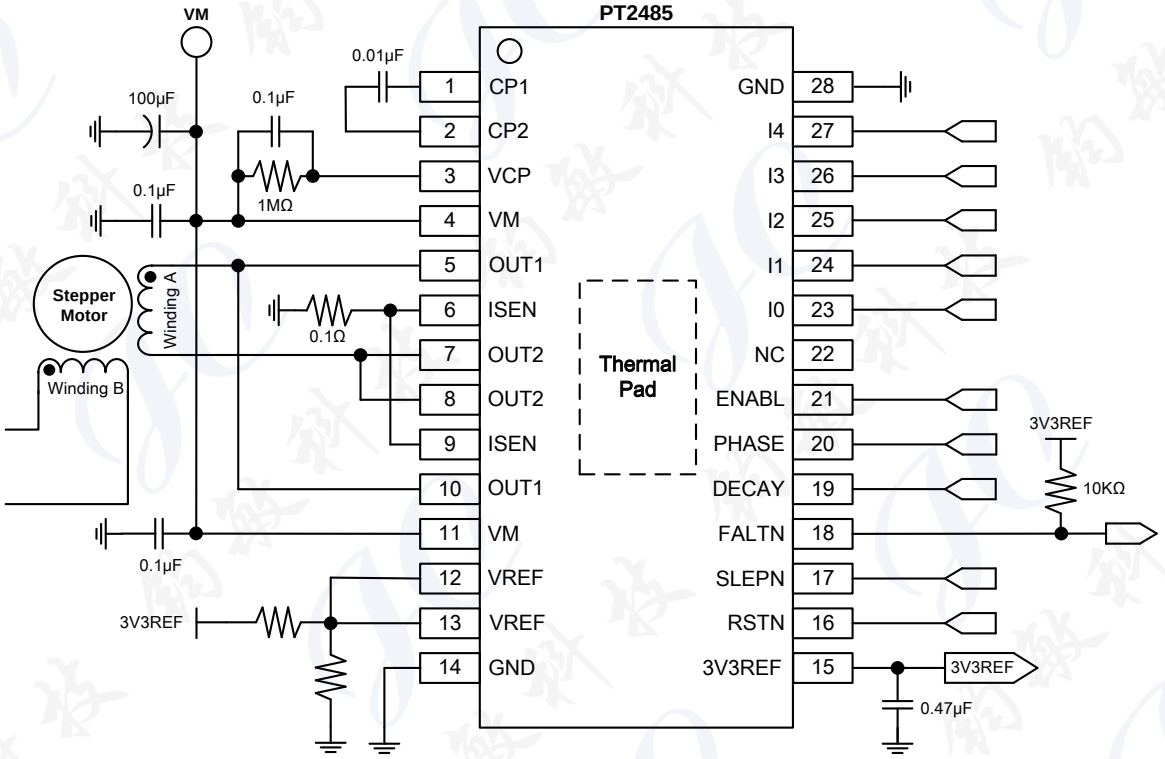
FEATURES

- 8V to 45V Supply Voltage Range
- 5A Maximum Peak Output Current at VM=24V, 3.5A Continue Output Current with additional heatsink.
- Low Conduction Resistance Switches: 0.2Ω(typ) for high side + low side in Tj=25℃.
- Phase and Enable Control Logic Interface
- H-Bridge Output Current is determinate by 5 Bits, 32 Levels PWM Current Regulation Inputs.
- Winding Current Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Drives a Single DC brushed Motor or Single Winding of a Bipolar Stepping Motor.
- Built In a 3.3V Reference Voltage Output
- Low-Power Sleep Mode
- Protection Features
  - Over Current Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Under Voltage Lock Out (UVLO)
  - Fault Indication Pin (FALTN)

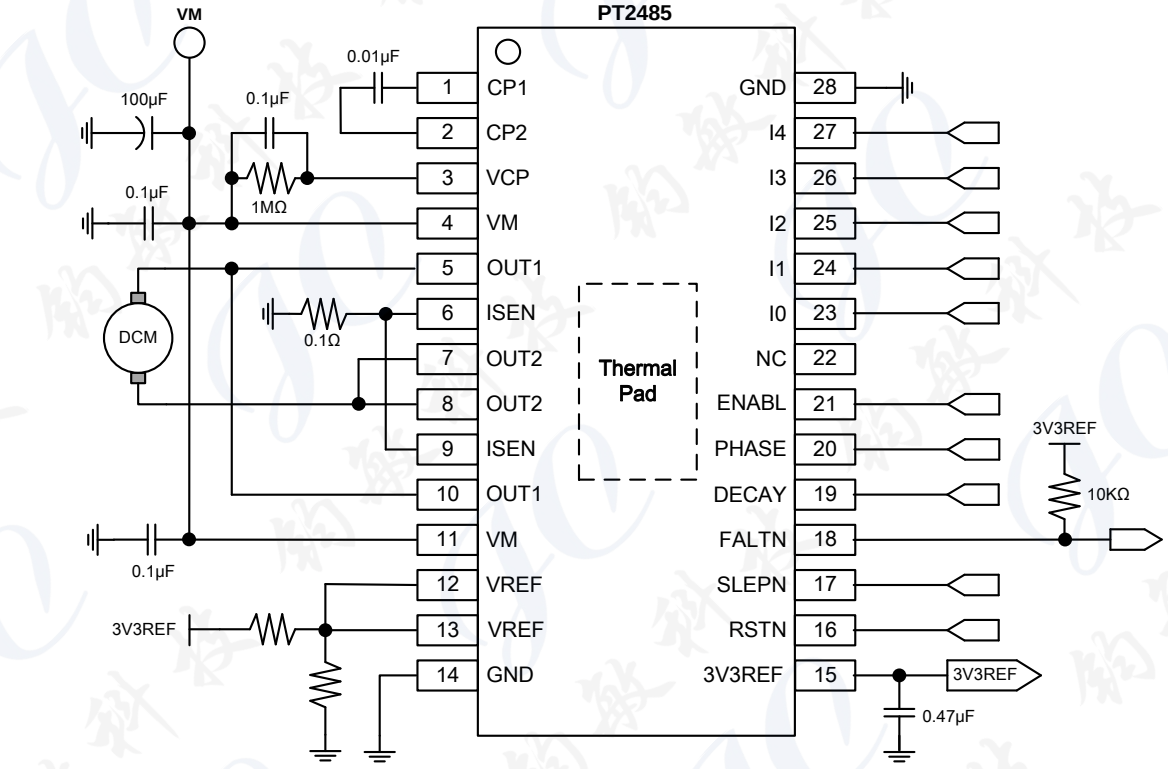
BLOCK DIAGRAM



APPLICATION CIRCUIT



Drives a single winding of bipolar stepping motor



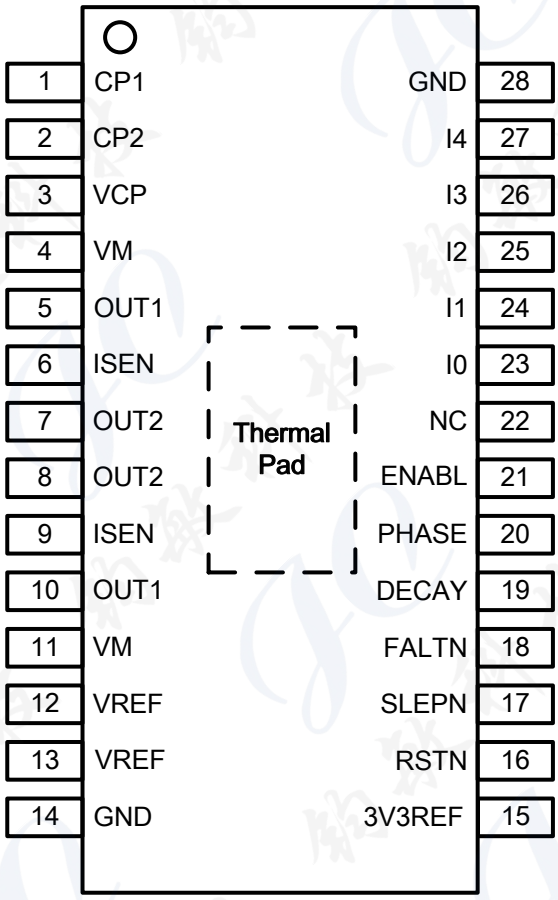
Drives a DC brushed motor

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2485-HT	28 Pins, HTSSOP	PT2485-HT

PIN CONFIGURATION

Top View



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
CP1	I	External flying capacitor for charge pump, Connect a 0.01μF/50V low-ESR ceramic capacitor between CP1 and CP2.	1
CP2	I		2
VCP	O	High-side gate drive supply voltage (Connect a 0.1μF/50V ceramic capacitor and a 1MΩ resistor to VM.)	3
VM	-	H-Bridge power supply	4
OUT1	O	H-Bridge output 1	5
ISEN	I	H-Bridge current sense / GND	6
OUT2	O	H-Bridge output 2	7
OUT2	O	H-Bridge output 2	8
ISEN	I	H-Bridge current sense / GND	9
OUT1	O	H-Bridge output 1	10
VM	-	H-Bridge power supply	11
VREF	I	H-Bridge current set reference input	12
VREF	I	H-Bridge current set reference input	13
GND	-	Device ground	14
3V3REF	O	3.3V reference voltage output	15
RSTN	I	Reset input (L=Initialize all of internal logic registers and disables H-bridge outputs)	16
SLEPN	I	Sleep mode input (H=device enable, L=low-power sleep mode)	17
FALTN	O	Fault, Logic low when fault condition appear (OCP, TSD)	18
DECAY	I	Decay mode (Low = slow decay, open = mixed decay, high = fast decay)	19
PHASE	I	H-Bridge output current phase (H: OUT1=high, OUT2=low)	20
ENABL	I	H-Bridge enable (H: H-bridge output active)	21
NC	-	No connect.	22
I0	I	H-Bridge PWM current regulation reference generator input, the 5 bit DAC derives the VREF input and generates 32 steps dc level to the PWM comparator.	23
I1	I		24
I2	I		25
I3	I		26
I4	I		27
GND	-	Device ground	28

FUNCTION DESCRIPTION

PWM MOTOR DRIVERS

The PT2485 is a single H-bridge driver with PWM current regulation circuitry. A block diagram of the system control circuitry is shown in Figure 1, the H-bridge driver is able to drives a DC-brushed motor or single winding of a bipolar stepping motor.

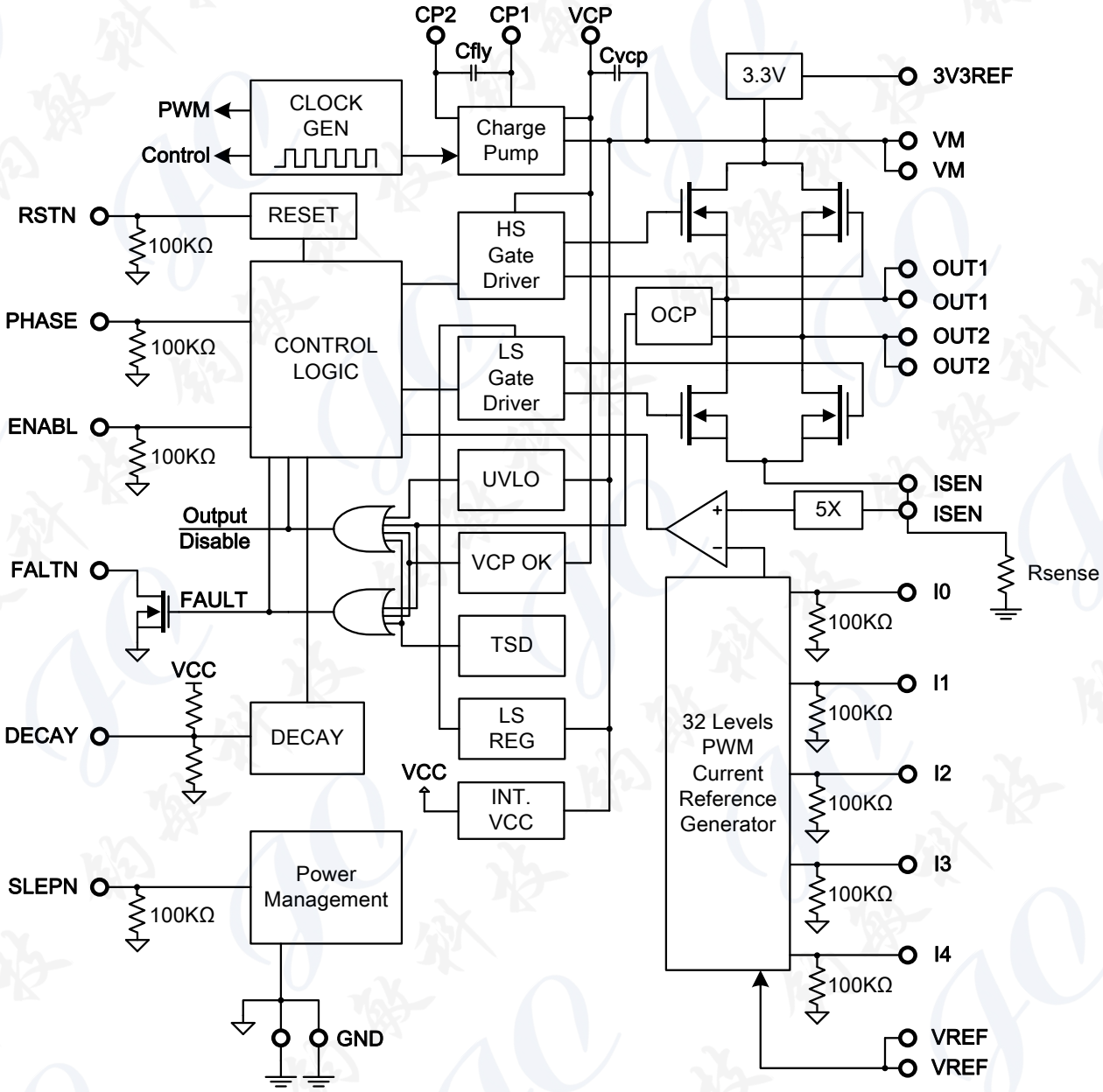


Figure 1, Motor Control Circuitry

The pins with same naming (VM, OUT1, OU2, ISEN, VREF) should be tight together in PCB with cupper trace.

H-BRIDGE OUTPUT CONFIGURATION

The output switches conducts controlled by the PHASE and ENABL logic state and the Table 1 shows the I/O logic corresponds.

ENABL	PHASE	OUT1	OUT2
0	X	HiZ	HiZ
1	1	H	L
1	0	L	H

Table 1, H-Bridge Output Configuration

PWM CHOPPING CURRENT REGULATION

The motor windings current is regulates by a fixed-frequency PWM chopping, the ENABL pin pull-up to logic high level will enable the H-bridge outputs, the winding current flows through the switches of H-bridge and current phase determinate by PHASE logic setting. The slew rate of winding current is depends on the VM voltage and inductance of the winding. Once the winding charge current reaches PWM comparator threshold, the H-bridge will transit to current decay mode and it is determinate by the DECAY pin setting. For a stepping motor, PWM current regulation is often to maintain the winging current level and helps motor torque steady, and current reference generator can be uses for micro-stepping purpose. For a DC motors, PWM current regulation can limiting starting and stall current.

A comparator is uses to control the PWM chopping current level. The winding current signal is retrieve from the I*R drops of the current sense resistor on the ISEN pin and multiples by 5; and the current setting voltage is applied to the VREF pin and scale by a 5-Bits DAC, divides the VREF input to 32 levels. In the Table 2 shows the bits definition. The H-bridge output current will be sets to zero when I0 to I4 pins are all in logic LO state (0x00h).

The PWM chopping current is calculate in Equation 1.

$$\mathbf{I_{CHOP}} = \frac{\mathbf{V_{REF}} \times \mathbf{DAC\ ratio}}{\mathbf{5} \times \mathbf{R_{ISENSE}}} \qquad \text{Eq.(1)}$$

Example 1:

With a 0.1Ω sense resistor and the VREF pin is 2.0 V, the VREF 5-Bits DAC ratio is 100% of full-scale level (0x1Fh), the output current can calculates by Eq.(1):

(2.0 V x 100%) / (5 x 0.1 Ω) = 4.0A.

Example 2:

With a 0.2Ω sense resistor and the VREF pin is 2.5V, the VREF 5-Bits DAC ratio is 38% of full-scale level (0x08h), the output current will calculates by Eq.(1):

(2.5 V x 38%) / (5 x 0.2 Ω) = 0.95A.

I4	I3	I2	I1	I0	Hex Value	VREF DAC Ratio (% Full-Scale Chopping Current)
1	1	1	1	1	0x1Fh	100%
1	1	1	1	0	0x1Eh	100%
1	1	1	0	1	0x1Dh	99%
1	1	1	0	0	0x1Ch	98%
1	1	0	1	1	0x1Bh	97%
1	1	0	1	0	0x1Ah	96%
1	1	0	0	1	0x19h	94%
1	1	0	0	0	0x18h	92%
1	0	1	1	1	0x17h	90%

1	0	1	1	0	0x16h	88%
1	0	1	0	1	0x15h	86%
1	0	1	0	0	0x14h	83%
1	0	0	1	1	0x13h	80%
1	0	0	1	0	0x12h	77%
1	0	0	0	1	0x11h	74%
1	0	0	0	0	0x10h	71%
0	1	1	1	1	0x0Fh	67%
0	1	1	1	0	0x0Eh	63%
0	1	1	0	1	0x0Dh	60%
0	1	1	0	0	0x0Ch	56%
0	1	0	1	1	0x0Bh	51%
0	1	0	1	0	0x0Ah	47%
0	1	0	0	1	0x09h	43%
0	1	0	0	0	0x08h	38%
0	0	1	1	1	0x07h	34%
0	0	1	1	0	0x06h	29%
0	0	1	0	1	0x05h	24%
0	0	1	0	0	0x04h	20%
0	0	0	1	1	0x03h	15%
0	0	0	1	0	0x02h	10%
0	0	0	0	1	0x01h	5%
0	0	0	0	0	0x00h	0% (H-bridge disabled)

Table 2, PWM Chopping Current VS VREF DAC Bit Definition

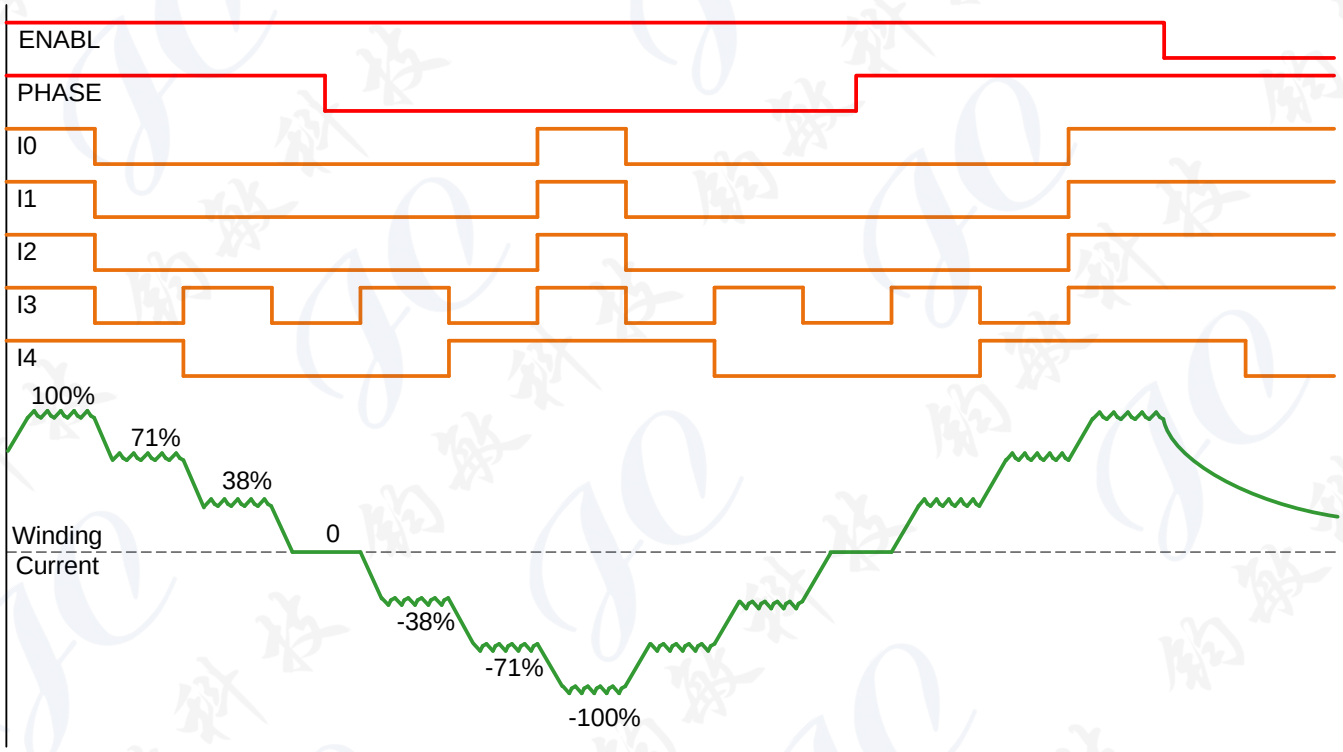


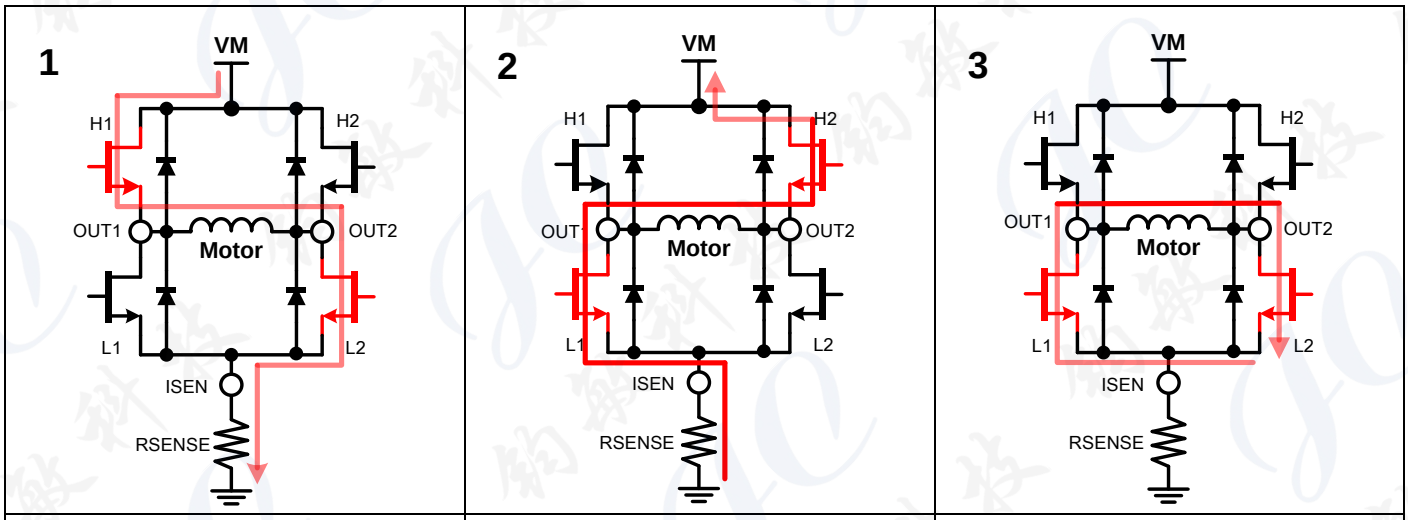
Figure 2, PWM Chopping Current with VREF DAC Bit Status

DECAY MODE

The DECAY pin logic states will determinate the winding current flows in current decay time. In charge period, the motor winding excitation by H-bridge output current and ISEN resistor measures I*R drops then send to PWM comparator. When charge current reaches target level, the H-bridge will switches to decay mode, it depends on DECAY pin logic status and could choose from fast, slow or mixed decay. Please refer to the Table 3 and Figure.3 shows the current direction in different decay mode and Figure 4 shows mixed decay sequence waveform.

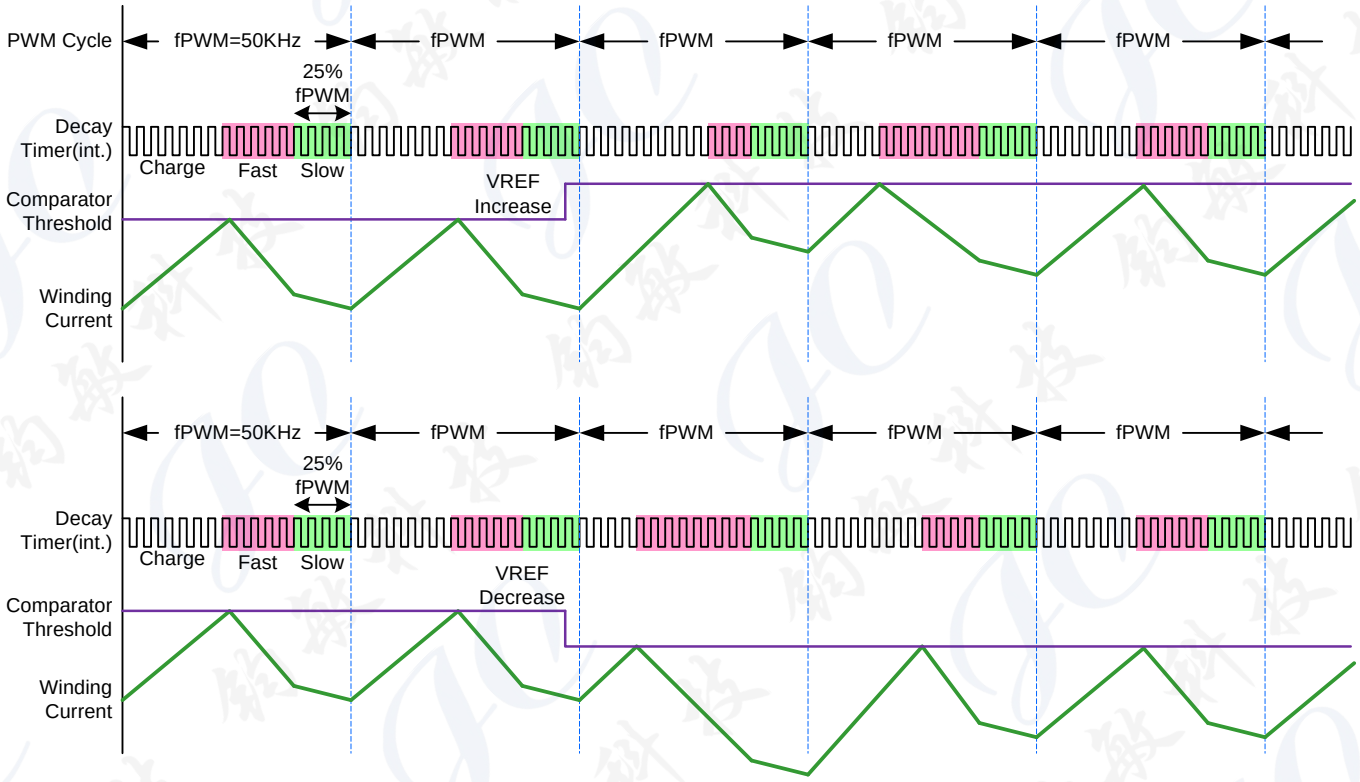
DECAY Pin Level	DECAY Pin Logic	Decay Mode
<0.6V	L	Slow
OPEN	FLOAT	Mixed
>2V	H	Fast

Table 3. DECAY Mode Setting



Charge	Fast Decay	Slow Decay
Motor winding connects to the VM and GND and the current flows through the switches H1 and L2, when ISEN I*R drops reaches target level, the charge mode will transit to decay mode.	Turn on the switches L1 and H2, The reversed voltage polarity applied to the winding inductor will quickly reduce the current. The H-bridge will be turns-off in fast decay mode if the winding current decays to zero.	Turn on the switches L1 and L2, the winding inductor current will flows in low side loop and reduced very slowly (synchronous rectifier).

Figure 3. Mixed Decay Mode Switching Sequence (PHASE=H)



(Decay timer(int.) is an internal clock timing for realize mixed decay operation ,it is not scaling to the fPWM.)

Figure 4. Mixed Decay Sequence Waveform

RESET and LOW POWER SLEEP MODE

Pull the RSTN pin to logic low state, the status of all control pins (except SLEPN) will be ignore and internal control circuit will be reset to initial state, the H-bridge output also disabled during RESTN in low state, in the meantime the 3.3V voltage reference and charge pump still works.

Pull the SLEPN pin to logic low will force the chip into a low power sleep mode. During sleep mode is active the H-bridges outputs are disable, and analog circuit such like charge pump for HS gate driver, 3.3V voltage reference (3V3REF) and internal clock generator will stopped. In the sleep mode, all of input logic states will be ignore until SLEPN returns to logic high state. When chip is wakes up from the low power sleep mode, a short waiting time (less than 1mS) before H-bridge becomes to normal operation is required because of charge pump starting time.

BLANKING TIME

During PWM chopping current flows through the H-bridge switches, the current level can be measures from the I*R drops of sense resistor on the ISEN pin, at the each edge of H-bridge switching , the current signal will waiting a blanking time then send to PWM comparator to avoid noises or spike causes fault-triggered. The blanking time fixed at 4μS and sets the minimum on-duty cycle in charge period, it will not less than around 20% in the 50 KHz PWM frequency.

PROTECTION CIRCUITS

The PT2485 have fully protection function to against miss-operation events.

OVERCURRENT PROTECTION (OCP)

Overcurrent detection circuit will always monitor all of output pins current during H-bridge is enable, this operation is independent from PWM chopping. If any output pin connects to VM, GND or across load shorted, the inrush current will detects by OCP circuit and immediately turn off H-bridge output after OCP deglitch time(T_{OCP} ,3μS). The chip will remain disabled until either RSTN pin is toggle once or power down the VM supply and apply again.

If an output pin touching the VM, the short circuit current will flows through the low side MOSFET and current sense resistor to GND, to avoid sense resistance interference the OCP detection, user must keeping the sense resistance under certain range, for example, 0.3Ω or less is recommend.

THERMAL SHUTDOWN (TSD)

If the chip temperature exceeds preset 160℃, the H-bridge will be turn off and the FALTN pin will pull down, an external pull up resistor may detects FALTN logic state by MCU I/O pin. Once the junction temperature cooling down to below hysteresis window, the H-bridge outputs will be enables again.

UNDERVOLTAGE LOCKOUT (UVLO)

In Any time the VM pin voltage drops below the under voltage lockout threshold voltage, all circuitry in the chip will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

FAULT INDICATION (FALTN)

Whatever which condition is happens, the OCP, TSD or charge pump voltage failed, the open-drain FALTN pin will pull down immediately and remains until RSTN pin re-toggled or VM voltage re-applied. FALTN could connect to MCU I/O port for error reporting with a pull high resistor to the 3V3REF or 5V logic supply.

POWER SUPPLY CAPACITOR RECOMMENDATIONS

Consider a real world application scenario; the motor driver is design to drives high inductance load such like motor winding or solenoid coil. If a H-bridge turns-off all of outputs during inductor current still flowing, because the inductor current would not be reset immediately, the rest of free-wheel current would re-directs and passing through the body diode of the output FET and runs into VM supply and final decay to zero after de-magnetization time. This reverse current depends on load inductance, inductor current and re-generates current from the motor due to inertia of rotor.

In another case, the parasitic reactance (inductance + resistance) of power wire with the parasitic capacitance of PCB consists a LC resonates tank. During power supply sourcing current to the motor driver board, the VM voltage may drops quickly and parasitic LC resonate will trigged and starts oscillation if the local bypass capacitor is not sufficient.

For prevent unstable bounce or spike appears on VM bus, a large bounce absorber capacitor (>100μF) should be placed on VM bus line, it could absorb re-generates free-wheels current during DC motor brake and stabilize VM voltage during high forward/reverse motor current sources. A small MLCC 0.1μF bypass capacitor should be place near the motor driver IC power pin, VM and 3V3REF both, to reduce the spike causes by power line LC resonates.

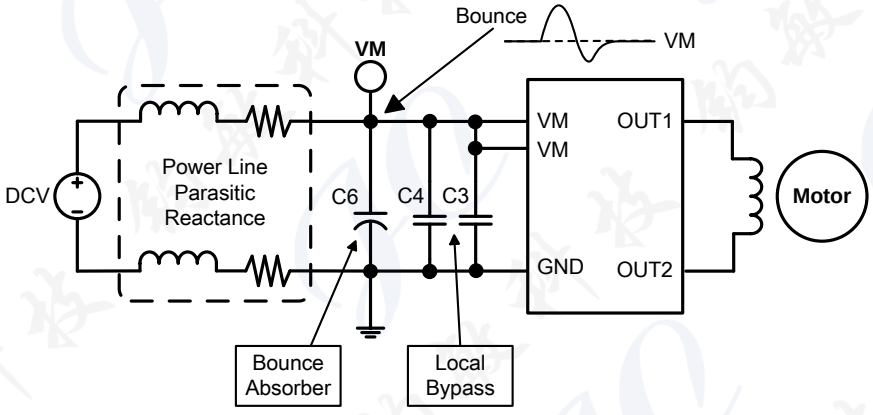
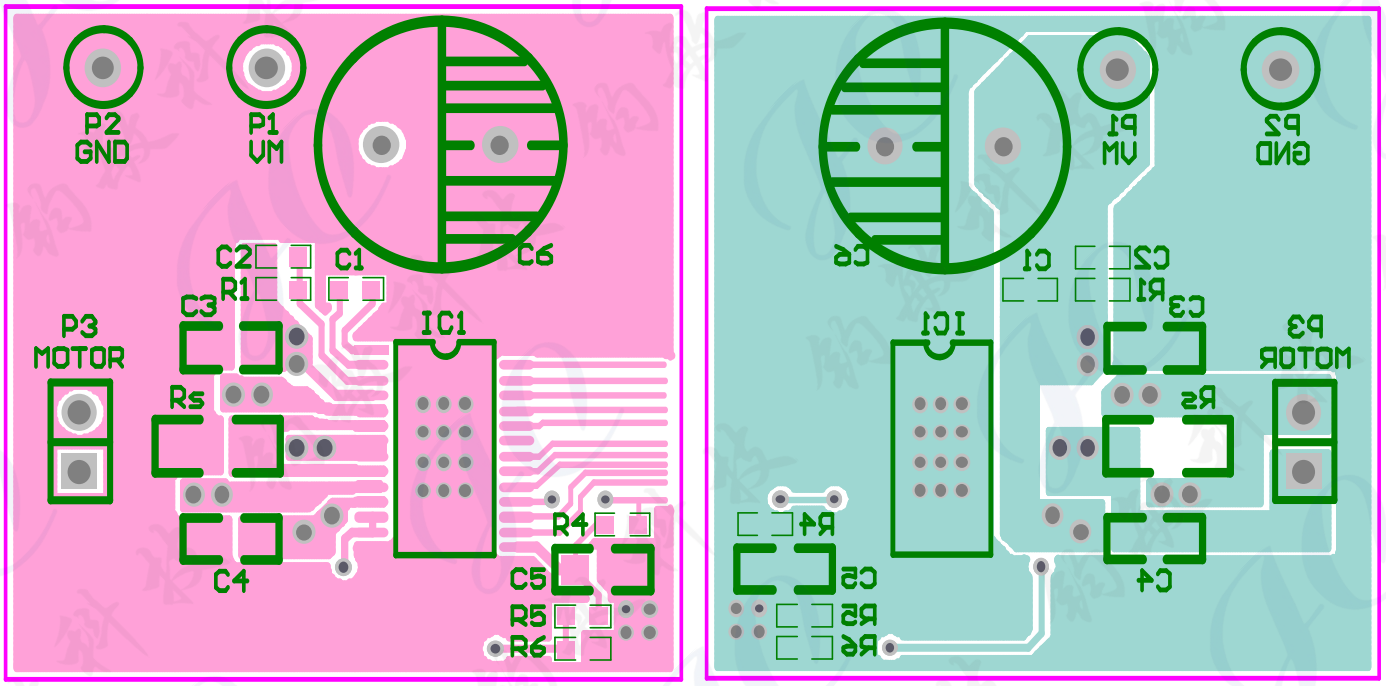


Figure 3. Motor Driver System with External Power Supply

PCB LAYOUT RECOMMENATION

The local bypass capacitor C3 and C4 should be place near the IC power pins, and bounce absorber capacitor C6 should be place on VM bus line. The GND plane should be place on the component side under the chip as a low impedance power trace, and larger area of GND plane and wider cooper trace reduce the thermal resistance (θ_{JA}). The thermal pad under HTSSOP package must soldering to the PCB component side and connects to the bottom side through via holes, this arrangement can further enhance the heat dissipation.



Top Side Bottom Side

Figure 5. Simplified Layout Example (HTSSOP package)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VM	-0.2	47	V
Control Pins Voltage	PHASE,ENABL, I0,I1,I2,I3,I4, DECAY RESTN,SLEPN,FALTN	-0.3	6	V
VREF Input Voltage	VREF	0	4	V
ISEN Input Voltage	V_{ISENx}	-0.6	+0.6	V
Peak Motor Output Current, T<1μS	Ipk	Limited by Internal Circuit		A
Continue Motor Output Current(note1)	Iout	0	5	A
Operating Temperature	Topr	-40	85	°C
Storage Temperature	Tstg	-40	150	°C
ESD, Human Body Model	HBM	-2000	+2000	V
ESD, Machine Model	MM	-200	+200	V

PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	HTSSOP (28 PINS)	VQFN (28 PINS)	Unit
From chip conjunction dissipation to external environment	Rja	Ta=25°C	38.9	35.8	°C/W
From chip conjunction dissipation to package surface	Rjc		23.3	25.1	

RECOMMENED OPERATING CONDICTION

Parameter	Symbol	Min	Typ	Max	Unit
Motor Power Supply Voltage Range	V_M	8	24	45	V
VREF Input Voltage(note2)	V_{REF}	1	-	3.5	V
3V3REF Load Current	I_{3V3}	-	-	1	mA
External PWM clock frequency	F_{EXT}	0		100	KHz

note1 : Maximum Iout is depends on thermal resistance of PC board.
note2 : VREF less than 1V may degrades the Itrip tolerance.

ELECTRICAL CHARACTERISTIC

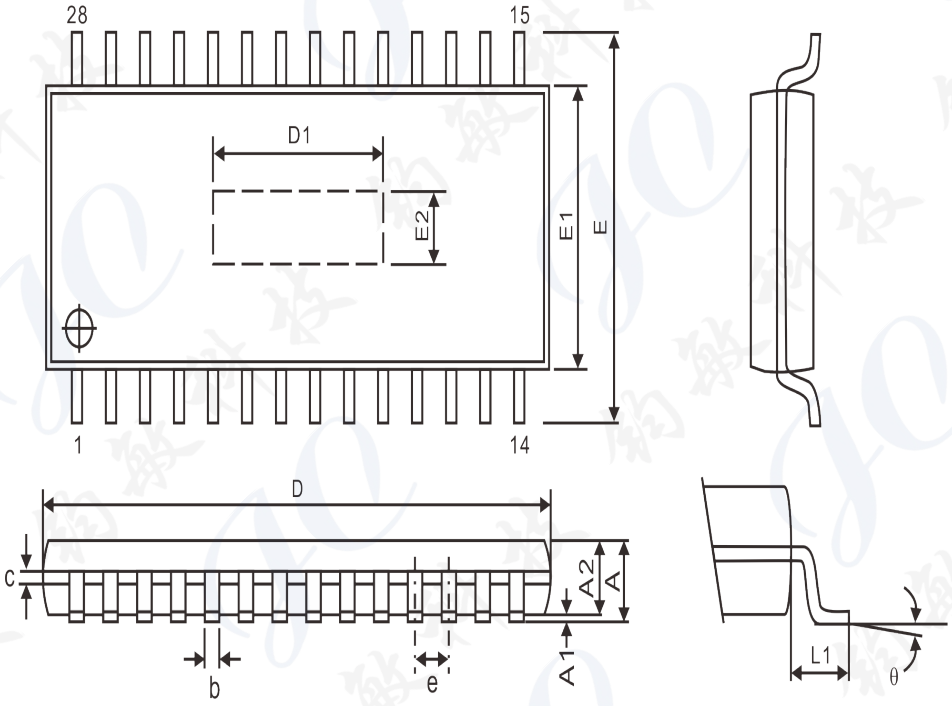
TA=25°C , VM=24V ,over operating free-air temperature range (unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Current	I_M	V_M=24V, f_{PWM}<50KHz		7	10	mA
		V_M=24V, Sleep mode		20	30	μA
Under Voltage Lock Out	UVLO	V_M rising		6.8	7.4	V
3V3REF REGULATOR						
3V3REF Output Voltage	V3P3	IOUT = 0 to 1mA,VM=24V	3.2	3.3	3.4	V
Charge Pump						
Charge Pump Output Voltage	VCP	Between VCP and VM	4.5	5	5.5	V

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC LEVEL INPUTS						
Digital Input High Level	V_{IH}		2		5.25	V
Digital Input Low Level	V_{IL}			0.6	0.7	V
Input Hysteresis	V_{HYS}			0.5		V
Input High Current	I_{IH}	VIN = 3.3 V		33	100	μA
Input Low Current	I_{IL}	VIN = 0	-20		20	μA
Internal Pulldown Resistance	R_{PD}			100		KΩ
FALTN OUTPUT (OPEN-DRAIN OUTPUT)						
Output Low Voltage	V_{OL}	IO = 5mA			0.5	V
Output High Leakage Current	I_{OH}	VO = 3.3 V			1	μA
DECAY INPUT						
Input High Threshold Voltage	V_{IH}	For fast decay mode	2			V
Input low Threshold Voltage	V_{IL}	For slow decay mode	0		0.6	V
Input Current	I_{IN}	Vin=3.3V			±20	μA
Internal Pullup Resistance	R_{UP}			250		KΩ
Internal Pulldown Resistance	R_{DN}			250		KΩ
H-BRIDGE DRIVER						
HS FET on Resistance	$R_{DS(ON)}$	V_M = 24V, I_O = 1A , T_J = 25°C		0.1		Ω
		V_M = 24V, I_O = 1A , T_J = 85°C		0.13	0.16	Ω
LS FET on Resistance	$R_{DS(ON)}$	V_M = 24V, I_O = 1A , T_J = 25°C		0.1		Ω
		V_M = 24V, I_O = 1A , T_J = 85°C		0.13	0.16	Ω
Off-State Leakage Current	I_{OFF}		-40		40	μA
MOTOR DRIVER						
Internal Current Regulation PWM Frequency	f_{PWM}			50		KHz
Current Sense Blanking Time	t_{BLANK}			4		μS
Rise Time	t_R	V_M =24V	70		220	nS
Fall Time	t_F	V_M =24V	70		220	nS
PROTECTION CIRCUITS						
Overcurrent Protection Trip Level	I_{OCP}		6			A
Overcurrent Protection Deglitch time	T_{OCP}			3		μS
Thermal Shutdown Temperature	t_{TSD}	Junction Temperature	150	160	180	°C
Recovery Window	t_{RW}			50		°C
PWM CURRENT REGULATION CONTROL						
VREF Input Current	I_{REF}	VREF = 3.3V	-3		3	μA
ISEN Trip Voltage	V_{TRIP}	VREF = 3.3V, 100% current setting	635	660	685	mV
Current Regulation Tolerance	ΔI_{CR}	VREF = 3.3V, 71% current setting	-5		5	%
		VREF = 3.3V, 38% current setting	-10		10	
		VREF = 3.3V, 10% current setting	-15		15	
		VREF = 3.3V, 5% current setting	-25		25	
Current Sense Amplifier Gain	A_{ISENSE}	Design Guarantee		5		V/V

PACKAGE INFORMATION

28-PIN, HTSSOP, 173MIL



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
b	0.19	-	0.30
c	0.09	-	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.4 BSC.		
e	0.65 BSC.		
D1	4.41	-	5.51
E2	2.40	-	3.00
L1	1.00 REF		
θ	0°	-	8°

Notes:
1. All dimensions refer to JEDEC MO-153 AET

IMPORTANT NOTICE

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REVISION HISTORY

Date	Revision No.	Reference No.	Modification
08/11/2020	PT2485 PRE1.0		Initial version