1

DESCRIPTION

The PT2511 is a three-phase, hall sensor sinusoidal brushless DC motor driver with integrated power MOSFETs, which can provide continuous drive current up to 1.5A. The three-phase control is based on sine wave driving scheme and it is designed to reduce electrical audible noise in motor phase commutation. The integrated charge pump of the device boosts VDD internally and fully enhances the high-side MOSFETs. On-chip +5V LDO provide voltage for logic and analog circuits operation. The PT2511 has internal TSD function protection. The package of PT2511 is HTSSOP28.

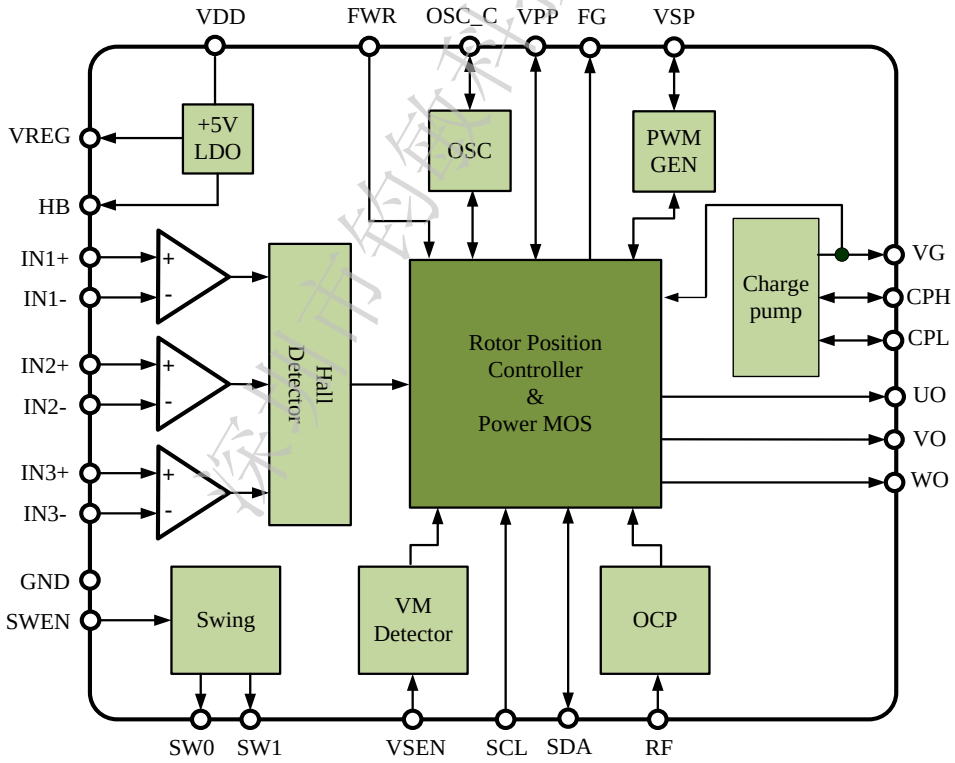
FEATURES

- Hall sensor sinusoidal control for 3-phase BLDC
- Current limit function
- Drive current: 1.5 A continuous
- Thermal shutdown(TSD) protection
- Motor lock protection
- Forward/Reverse control with FWR pin
- PWM or DC input for speed control
- FG output for rotation speed
- Support Hall element and Hall sensor
- I2C interface for parameter setting and write to internal OTP.

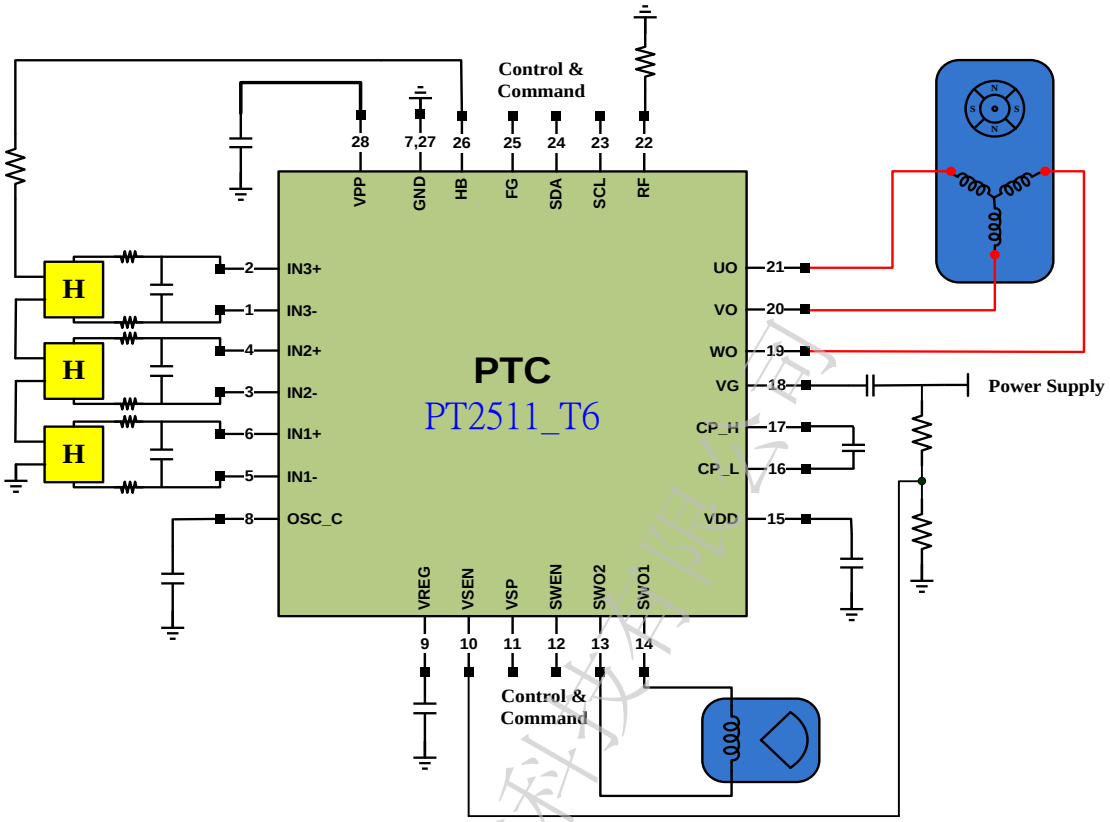
APPLICATIONS

- Three-phase BLDC motor
- Fan application

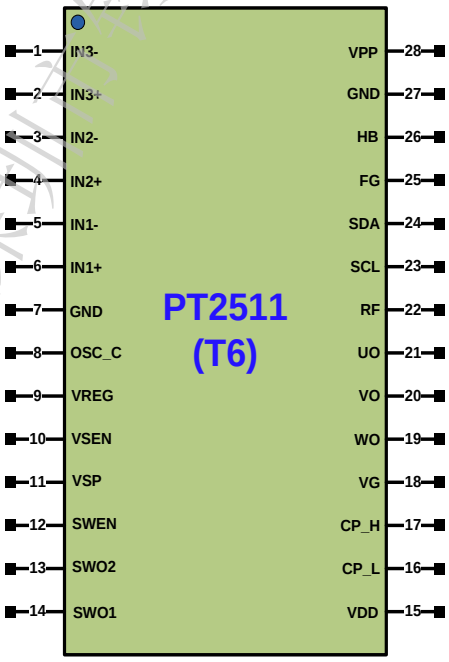
BLOCK DIAGRAM



APPLICATION BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESCRIPTION

Pin Name	I/O/P	Description	Pin No.
IN3-	I	Hall element 3 input-	1
IN3+	I	Hall element 3 input+	2
IN2-	I	Hall element 2 input-	3
IN2+	I	Hall element 2 input+	4
IN1-	I	Hall element 1 input-	5
IN1+	I	Hall element 1 input+	6
GND	P	Signal ground	7,27
OSC_C	I	Connect to external capacitor for startup step setting	8
VREG	O	+5V LDO output	9
VSEN	I	Connect to voltage divider of VDD for voltage sensing.	10
VSP	I	DC or PWM input for speed control	11
SWEN	I	Swing head enable control; "1" = start motor	12
SWO2	I/O	Swing motor control – full-bridge output 2	13
SWO1	I/O	Swing motor control – full-bridge output 1	14
VDD	P	VDD supply input	15
CP_L	I/O	Charge pump pin, use a ceramic capacitor between CP_H and CP_L	16
CP_H	I/O	Charge pump pin, use a ceramic capacitor between CP_H and CP_L	17
VG	P	Charge pump output	18
WO	O	W phase signal output	19
VO	O	V phase signal output	20
UO	O	U phase signal output	21
RF	I	Current limit voltage sensing	22
SCL	I	Serial clock input - I2C control interface	23
SDA	I/O	Serial data input/output – I2C control interface	24
FG	O	Motor rotation speed indicator, logic level output	25
HB	O	Controlled +5V output for Hall sensor bias	26
VPP	P	High voltage power supply (7.5V) for programming OTP	28

FUNCTION DESCRIPTION

POWER SUPPLY

PT2511 consumes very low current (<5mA) and build-in a 5V LDO for logic and analog circuits. The supply voltage for VDD range from +7V to +28V. For lower operation voltage in VDD, the VDD and VREG can be connected together.

PT2511 will detect VREG to reach 3V internally for avoiding instability on external power. A power good signal will send to logic circuit to start operation within 10ms.

Adding proper bypass capacitor(s) close to the sensible IC pins will reduce interference from motor systems or wires connection to improve chip performance.

PT2511 has an integrated charge pump to boost VDD for internal N-N type MOSFET driver.

PWM OR DC INPUT FOR SPEED CONTROL

The PT2511 has an external DC or PWM control input to change the motor speed. For PWM input, the HIGH voltage level needs to be greater than 3.3V(recommended to 3.5V) and the LOW voltage level need to be less than 0.5V(recommended to 0.3V). The PWM carrier frequency is recommended between 15 KHz to 25 KHz. For DC input, the DC control voltage should range from 0.5V to 3.3V.

Besides the traditional “duty control voltage” scheme, PT2511 also provide close loop speed control through the setting SpdEN in bit 3 of sub-address 0x39, as depicted in Figure 1. Four slope selections, SpdSel[1:0], are also provide for different motor application. With the help of RiseStep,FallStep1 and FallStep2 parameters, PT2511 provide stable speed regulation output.

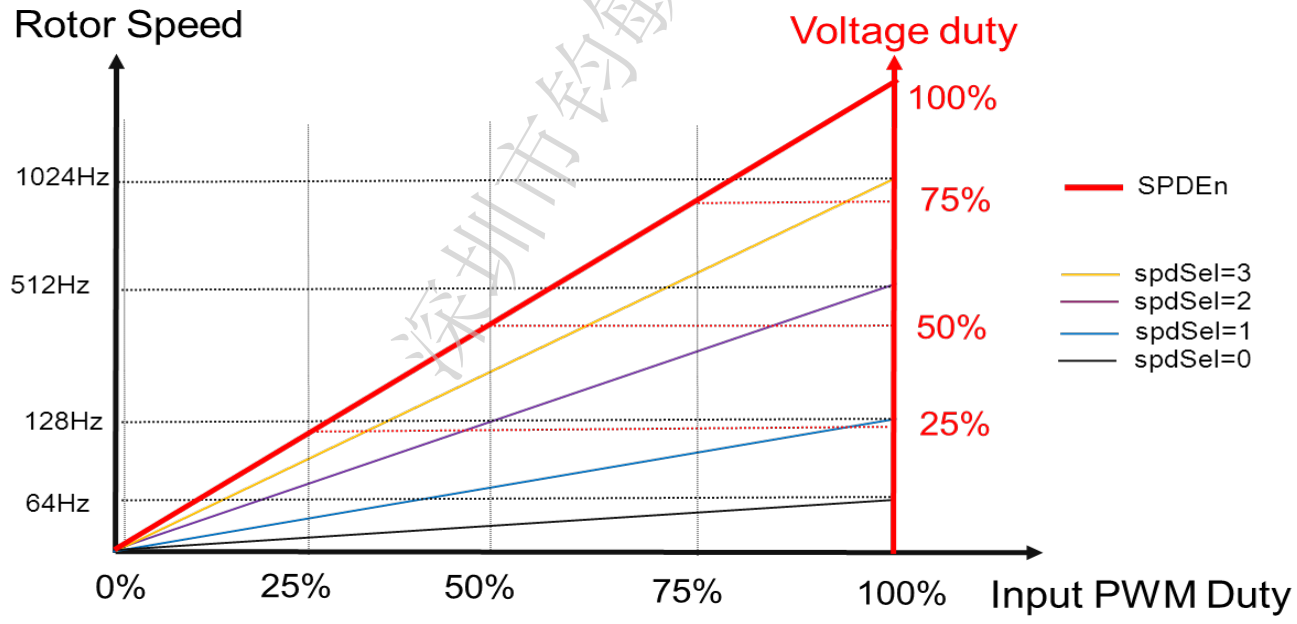


Figure 1. PT2511 provide different speed control scheme

HALL SENSOR CONTROL SCHEME

The PT2511 control scheme is based on hall sensor information and produce sinusoidal excitation waveform. It benefits to provide accurate and silent (without electrical noise) driving control. Unlike the sensorless control scheme, hall sensor control provides smooth start-up without reverse rotation.

As shown in **Figure 2** and **Figure 3**, three hall sensors can be configured as 60° or 120° spacing through internal parameter, PhCode, 0: 60 degree spacing, 1: 120 degree spacing.

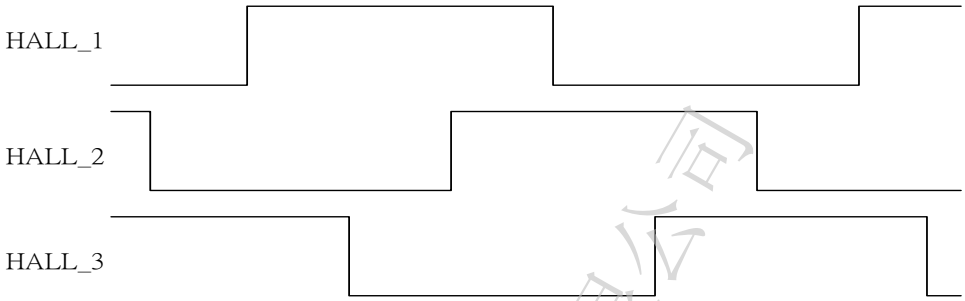


Figure 2. 120 degree spacing of the hall signals

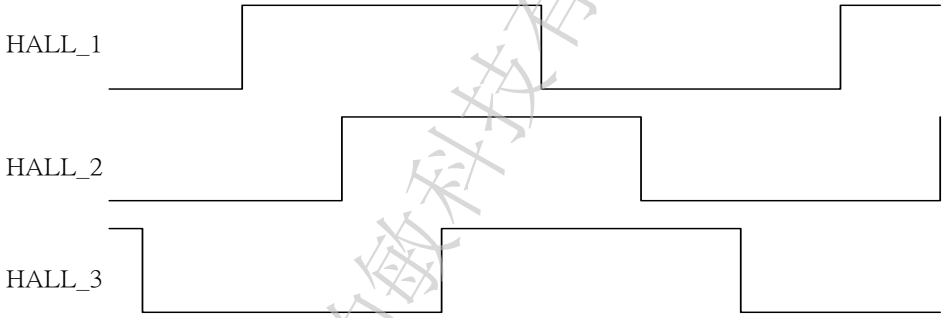


Figure 3. 60 degree spacing of the hall signals

The hall sensor has different sensitivity and layout distance from the rotor to cause phase offset. As shown in **Figure 4**, PT2511 can synchronize the phase offset related to HALL_U, range from -60 degree to 60 degree through internal parameters, SyncAng and RSyncAng. The phase offset is set individually for the forward or reverse rotation.
PT2511 also support different type or sensitivity hall device, for examples, hall IC or hall element

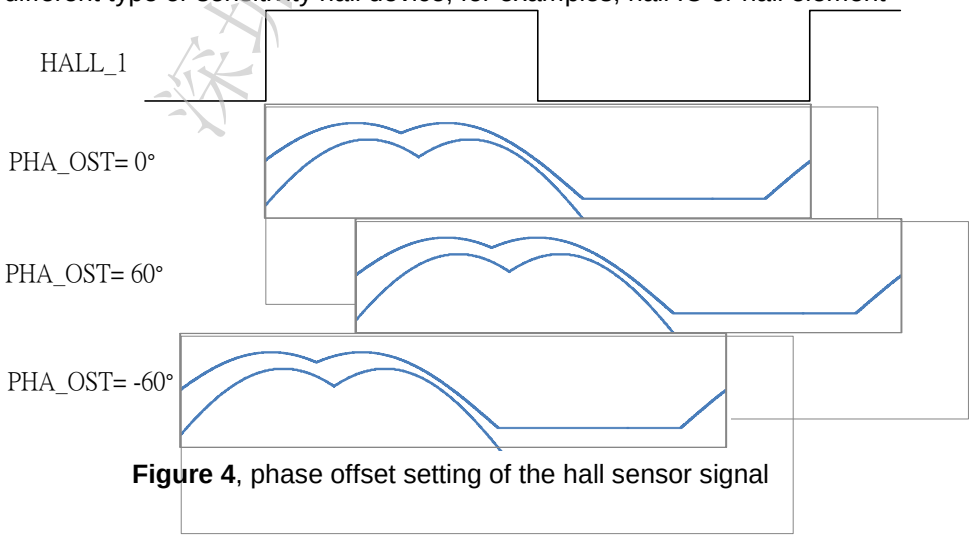


Figure 4, phase offset setting of the hall sensor signal

PHASE ADVANCE SETTING

Due to the characteristics of inductance loading of stator winding, the phase of the shunt current may drift away as the rotor speed increase. The PT2511 provide automatic or manual adjustment through the setting PAAuto in address 0x30. It's easy for customer to achieve best efficiency in any circumstance. In the automatic setting, it provides sixteen curves PASlope and one maximum phase leading limitation MaxPA to choose.

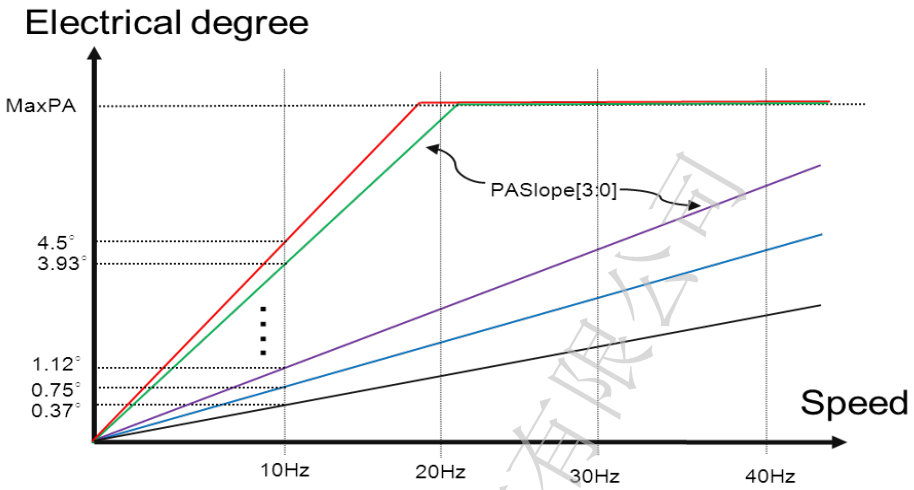


Figure 5. Automatic phase advance slope selection

Moreover, the best efficiency point may vary with the intensity of back EMF, shunt current, rotor speed and shunt inductance, etc. With the non-linear characteristic, the parameters of PAM10HZ~PAM150HZ help to adjust phase advance in individual rotation speed manually. The maximum manual adjustment speed is up to 150Hz. And the maximum phase leading limitation MaxPA is also applied in manual mode.

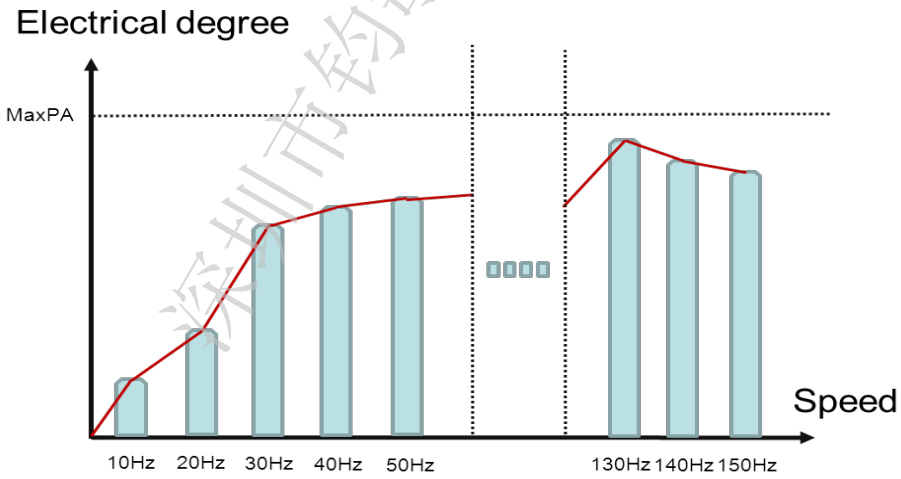


Figure 6. Manual phase advance setting according to speed

INPUT COMMAND PROFILE

PT2511 provide smooth speed up/down profile with different load as depicted in Figure 7. With the StopDuty setting, user can decide when to release excitation without audible noise.

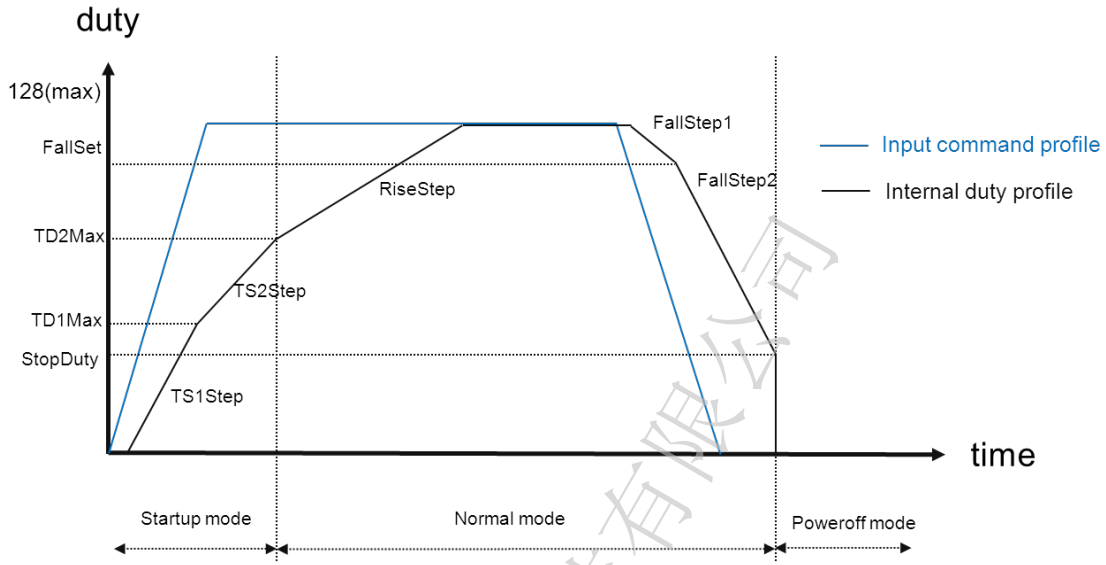


Figure 7. Smooth parameter for speed up/down.

CURRENT PROTECTION

The PT2511 has a two-level current protection function by using a sense resistor over RF pin and the sensed signal (V_{RF}) are related to motor current(Imotor) after low pass filter. When the V_{RF} exceeds V_{OCPL}, OCPL signal is triggered, PWM duty will reduce to keep V_{RF} under V_{OCPL} threshold. And if the V_{RF} exceed V_{OCPH}, OCPH signal is triggered, PWM turnoff and system go into the lock mode.

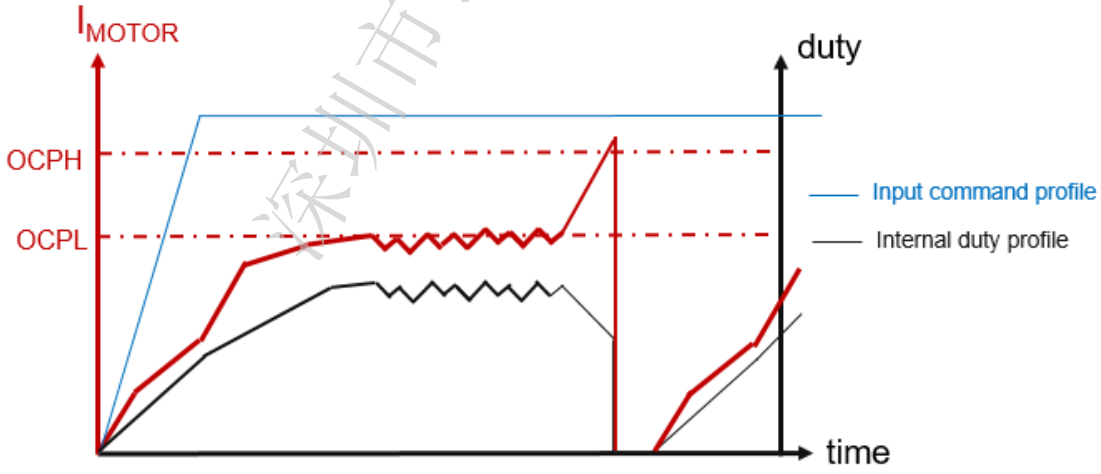


Figure 8. Two-stage over current protection

The OCPHFilter and OCPLFilter provide deglitch time period ranging from 0.4us to 0.4ms to make sure stable motor operation. Due to the different applications, PT2511 provide multi-level V_{OCPL}/ V_{OCPH} setting through PRT_LVL register.

START UP & LOCK PROTECTION

The initial position information is provided by hall sensor. According to hall signal, PT2511 commutates motor and startup. The startup mode maximum duty is set by TD2Max, in other words, the maximum startup force for different motor application. Increasing / decreasing PWM duty, the motor speed can be accelerated/ decelerated. And the profile can be set from parameters.

If the controller did not detect the expected hall sensor signal, the state machine would go to the lock protection mode. PT2511 will wait a period and re-start again (the period and re-start times are set by internal parameter CTRise and CTFall) and the ExptNum exception number counter will plus 1. If the motor remained to be locked, and the counter number exceed the MaxExptNum setting, it would cause system fall into the dead lock status. System no longer start at this state, and the only way to restart the system is turning off then turning on the supply voltage.

OVER TEMPERATURE PROTECTION

PT2511 has an internal thermal shutdown (TSD) protection. It shuts down the chip for junction temperature larger than 155 ˚C and recovers operating conditions for junction temperature falls back to 115 ˚C.

UNDER VOLTAGE AND OVER VOLTAGE PORTECTION

When the voltage level of VSEN pin is greater than (VREG/2) or less than (VREG/2)-△V, the output power MOSFETs are shut down .
The voltage level of △V is set by OTP(One Time Programming) memory.

FG OUTPUT FOR SPEED INFORMATION

PT2511 has FG output to observe motor speed. When the rotor is running an electric cycle, the FG output toggles High to Low. So when calculating the rotation speed, it needs to take into account the pole numbers of the rotor. For example, if rotor is 8 poles (four pairs of NS), the motor run a lap will have 4 FG output. Motor speed is usually present in RPM (Revolutions per Minute), so the rotation speed of the simple formula is calculated as

RPM = FG x 120 / POLE, FG is frequency in Hz, “POLE” is numbers of rotor.

FG pin is a 5V logic output.

PT2511 provide different FG configuration for external device to access, as the **Figure 11** depicted. XOREn setting enable three times factor and FGDiv provide divided by 1,2,4,8 setting.

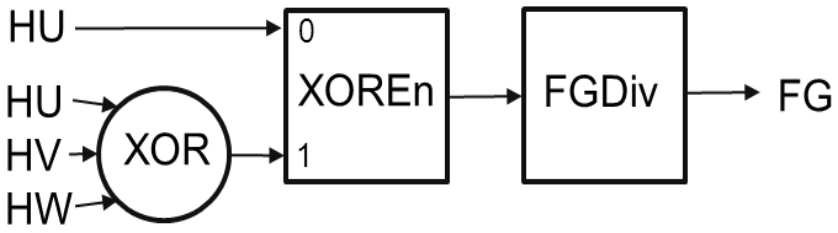


Figure 11. FG output configuration

FORWARD AND REVERSE SETTING

PT2511 can be set to forward or reverse rotation with internal parameter. If the rotation is switched, the motor will stop automatically and rotate with opposite direction. It is also suggested to control the motor speed by monitoring FG signal to optimize the reverse behavior, such as slow down profile or reverse waiting time.

UPWIND OR DOWNWIND STARTUP SETTING

PT2511 can detect automatically if the motor operate in the upwind or downwind condition. To make sure the motor operate properly the PT2511 brake the motor in the upwind condition until the rotor speed is down to acceptable range. In the downwind condition, PT2511 provide a scheme to adjust the startup duty to make sure the back EMF won't damage the HV device. The startup duty is set according to the rotor speed with scale and an offset value.

StartDudy=(RotorSpeed>>DNWScale) + DNWInit, where ">>" means right shift

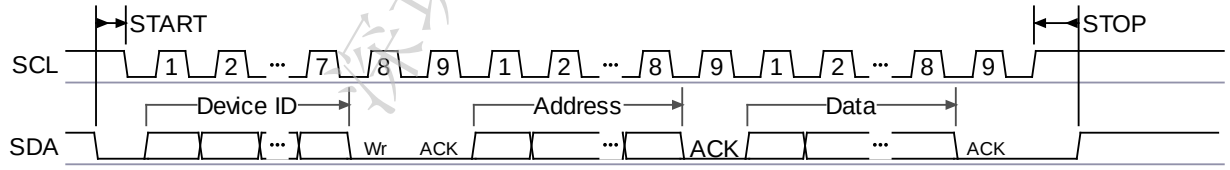
PARAMETERS SETTING

The other parameters are adjustable and wrote to internal OTP(One Time Programming) memory. PT2511 can be programmed two times through the I2C interface. VPP pin need apply +7.5V during the OTP programming.

I²C *MICROPROCESSOR INTERFACE*

To communicate with PT2511, the following control and status registers are accessible via I²C interface. I²C communicates with multiple devices by only two lines, **START** bit means a start condition; any transmission must start with it. **Device ID** is 7-bit device address identifier, each device owns only one address, and PT2511 is fixed to 0110100b. $\overline{\text{Wr}}$ $\overline{\text{Rd}}$ issuing a read or write operation, **ACK** is acknowledge bit, perform in the receiver, to inform the transmitter the data is properly received or stop data transmitting. **Address** is PT2511's register number to be described in next section. **STOP** is stop bit; any sequence must end with it. The I²C write operation is byte write mode, and read operation is byte read mode as described in **Figure 12**. The current I²C protocol speed support up to 50 KHz.

I2C Byte Write



I2C Byte Read

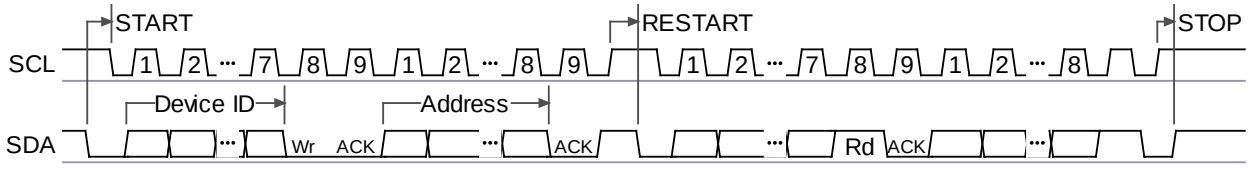


Figure 12. I²C byte write and byte read timing.

REGISTER TABLE

Register table mapping for address 0x0~0x8

Bit								Address
7	6	5	4	3	2	1	0	Hex
Reserved					PWMS	FWRS1	FWRS0	0
PWM_I2C								1
FG_CNT[7:0]								2
M_Status[2:0]			RDL	TSD	FG_CNT[10:8]			3
Reserved			SUMERR	BLANKERR		OCPL	OCPH	4
Reserved								5
HVID								6
EXPNUM[7:0]								7
Reserved							EXPNUM[8]	8

Register table mapping for address 0x21~0x53

Bit								Address
7	6	5	4	3	2	1	0	Hex
TS1Step[7:0]								21
TD2Max								22
TS1Step[8]	DNWScale[1:0]		TD1Max					23
TS2Step[7:0]								24
RiseStep[7:0]								25
DNWInit[5:0]						TS2Step[8]	RiseStep[8]	26
FallStep1[7:0]								27
FallStep2[7:0]								28
Reserved			DeadTime			FallStep1[8]	FallStep2[8]	29
FallSet								2A
StopDuty								2B
Reserved				ZCTarget				2C
Reserved								2D
FilterMax[9:8]		Reserved						2E
FilterMax[7:0]								2F
HallPwrEn	OCPLSlope		PAAuto	PASlope				30
HallSel	RSyncAng							31
Reserved	SyncAng							32
CTRise				CTFall				33
MaxExptNum[7:0]								34

Reserved						35
Reserved	MaxExptNum [8]	Reserved				36
Reserved						37
Reserved						38
HSMOS	HallCode	Reserved	SPDEN	Reserved	SPDSEL	39
Reserved						3A
MaxPA						3B
PAM10Hz						3C
PAM20Hz						3D
PAM30Hz						3E
PAM40Hz						3F
PAM50Hz						40
PAM60Hz						41
PAM70Hz						42
PAM80Hz						43
PAM90Hz						44
PAM100Hz						45
PAM110Hz						46
PAM120Hz						47
PAM130Hz						48
PAM140Hz						49
PAM150Hz						4A
Reserved	CLKTrim					4B
PRT_LVL						4C
OCPHFLTR[7:0]						4D
OCPLFLTR[5:0]					OCPHFLTR[9:8]	4E
UPWSel	Reserved					4F
UPWNUM[7:0]						50
Reserved	MinDuty					51
FWRSW	Reserved		OVOTSEL	Reserved		52
Reserved				FGDIV	XOREN	53

REGISTER DESCRIPTION

Address 0x0~0x8 is system control registers, providing information such as system status, even direct control the PWM duty, forward or reverse, etc.

Address	Register Name	Description		Default	Unit	R/W
0x00	SYS_CTL1	Bit [7:3]	Reserved			R/W
		Bit[2]	PWMS : 1 : select internal PWM duty control 0 : external VSP control	0		
		Bit[1:0]	FWRS : FWR is controlled by 1x : external FWR pin 00_b : FWR is 0 01_b : FWR is 1	2		
0x01	PWM_I2C	When PWMS set 1, PWM duty is controlled by this register		0	duty	R/W
0x02	FG_CNT[7:0]	Combine FG_CNT[10:8] to get a 11 bit frequency counter value every one second		0	counter	R
0x03	SYS_CTL2	Bit[7:5]	M_Status, Motor status 000_b : Startup 001_b : Normal 010_b : PWMOff 100_b : LockOn 101_b : DeadLock			R
		Bit[4]	RDL, normal operation status 0 : motor is in the normal state 1 : motor is not in the normal state			
		Bit[3]	TSD signal from the VSEN pin 0 : Comparator result is correct 1 : Comparator result is not correct			
		Bit[2:0]	FG_CNT[10:8]			
0x04	SYS_CTL3	Bit[7:5]	Reserved			R
		Bit[4]	SUMERR, OTP checksum error indicator. If the first byte is 0x5A, the checksum is generated automatically. 1 : OTP checksum is error 0 : OTP checksum is correct.			
		Bit[3:2]	BLANKERR, OTP blanking check. 00 : Bank 0 and 1 is blank. 01 : Bank 0 is blank, bank 1 is not blank. 10 : Bank 0 is not blank, bank 1 is blank. 11 : Bank 0 and 1 is not blank.			
		Bit[1]	OCPL, 1 : RF pin voltage exceed low level threshold. 0 : RF pin voltage is under low level threshold.			

Address	Register Name	Description		Default	Unit	R/W
		Bit[0]	OCPH 1 : RF pin voltage exceed high level threshold. 0 : RF pin voltage is under high level threshold.			
0x06	HVID	Hardware version control ID		2		R
0x07	EXPTNUM [7:0]	Combine with EXPTNUM[8] to get a EXPTNUM[8:0] register. The EXPTNUM will add one automatically when exception happen, for example, OCPH or LockOn state happens.		0		R
0x08		Bit[7:1]	Reserved			
		Bit[0]	EXPTNUM[8]	0		R

Address 0x21~0x5F is OTP parameters mapping registers, provide motor control related parameters.

Address	Register Name	Description		Default	Unit	R/W
0x21	TS1Step	Combine with bit 7 of sub-address 0x23 to form 9-bit of TS1Step[8:0] TS1Step is the first stage slope before reaching TD1MAX in the startup mode. Please refer to Figure 7. Unit is ms		10	ms	R/W
0x22	TD2Max	TD2Max is the maximum duty of the second stage startup. Please refer to Figure 7		50	duty	R/W
0x23	TD1Max	bit [7]	TS1Step[8]			R/W
		bit[6:5]	DNWScale[1:0], a scale of current speed in Hz, for example, the current speed is 48Hz, DNWScale set to 0, then the initial duty is startup from 48>>(0+2)	0	scale	
		bit[4:0]	TD1Max is the maximum duty of the first stage startup. Please refer to Figure 7.	3	duty	
0x24	TS2Step	Combine with bit 1 of sub-address 0x26 to form 9-bit of TS2Step[8:0] TS2Step is the second stage slope before reaching TD2MAX in the startup mode. Please refer to Figure 7.		47	ms	R/W
0x25	RiseStep	Combine with bit 0 of sub-address 0x26 to form 9-bit of RiseStep[8:0] RiseStep is the update slope before reaching the OCPL or desire speed setting. Please refer to Figure 7.		47	ms	R/W
0x26	Downwind startup	bit [7:2]	DNWInit[5:0], Combine with DNWScale[1:0], a suitable initial force to startup the motor when motor in a forward running situation.	0	duty	R/W
		bit [1]	TS2Step[8]			
		bit [0]	RiseStep[8]			
0x27	FallStep1	The first stage slope of slow down before the actual duty down to Fallset.		47	ms	R/W
0x28	FallStep2	The second stage slope of slow down before the actual duty down to StopDuty		47	ms	R/W
0x29	DeadTime Setting	Bit[7:5]	Reserved	0	clock	R/W
		Bit[4:2]	Dead time setting, range from 0.4us to 2.4us, suit for wide voltage operation. 0: 0.4us, 1: 0.8us, 2: 1.2us, 3: 1.6us, 4: 2.0us, 5~7: 2.4us			
		bit [1]	FallStep1[8]			
		bit [0]	FallStep2[8]			
0x2A	FallSet	The first stage duty for the actual duty decrease to.		40	duty	R/W
0x2B	StopDuty	The second stage duty for the actual duty decrease to.		64	duty	R/W

Address	Register Name	Description		Default	Unit	R/W
0x2C	ZCTarget	Bit[7:4]	Reserved	6	clock	R/W
		Bit[3:0]	Six-step startup count before entering normal state			
0x2E	FilterMax	Bit[7:6]	FilterMax[9:8]	0	clock	R/W
		Bit[5:0]	Reserved			
0x2F	FilterMax	Combine with bit[7:6] of sub-address 0x2E, to form 10-bit of FilterMax[9:0]. FilterMax is the deglitch time period both for the hall sensor/hall element signal.		100	clock	R/W
0x30	PASlope	Bit[7]	HallPwrEn, HB power output control 0: Turn off HB output during power-off mode, 1: HB output is always enable.	0		R/W
		Bit[6:5]	OCPLSlope, OCPL update rate selection when the OCPL event happens. 0: 6ms, 1: 12ms, 2:23ms, 4:47ms	2		
		Bit[4]	PAAuto, Phase leading adjustment selection, 0: manually, 1: auto	1		
		Bit[3:0]	PASlope, when PAAuto set to 1, there are 16 slope curves selection according to the rotation speed. Please check figure 5 and 6 for further explanation. The sixteen slope of phase advance per 10Hz is 4.5, 3.93, 3.56, 3.18, 3.0 ,2.8, 2.6, 2.43, 2.25, 2.06, 1.87, 1.68, 1.5, 1.12, 0.75, 0.37 degree.	7		
0x31	RSyncAng	Bit[7]	HallSel, Hall effect sensor type selection 0:Hall sensor IC, 1: Hall element	0		R/W
		Bit[6:0]	Hall sensor synchronization angle for the reversion rotation.	45	1.5 deg	
0x32	SyncAng	Bit[6:0]	Hall sensor synchronization angle for the forward rotation	45	1.5 deg	R/W
0x33	CTRise /CTFall	Bit[7:4]	Maximum time period before entering normal mode. If startup period exceed this period, lock-on number plus one and restart again.	2	sec.	R/W
		Bit[3:0]	Rest time period between each startup.	1	sec.	
0x34	MaxExptNum	The maximum exception number before entering dead-lock state. The exception include OCPH and lock-on. When entering dead-lock state, PT2511 release it only by system power on again.		20	times	R/W
0x39	SPDCtrl	Bit[7]	HSMOS, high side MOS type selection 0:NMOS, 1:PMOS	0		R/W
		Bit[6]	HallCode, Hall effect sensor position 0: 60 degree spacing, 1: 120 degree spacing	0		
		Bit[3]	SpdEn : 0: duty control voltage, 1: duty control speed, please check figure 1	0		
		Bit[1:0]	SpdSel, four different slope curve to choose maximum rotation speed 0:64Hz, 1: 128Hz, 2:512Hz, 3:1024Hz, please check Figure 1 for further explanation.	2		

Address	Register Name	Description		Default	Unit	R/W
0x3B	MaxPA	Maximum phase advance limitation		30	1.5 deg.	R/W
0x3C~ 0x4A	PAM10HZ~ PAM150HZ	Phase advance adjusted manually from 10Hz to 150Hz according the rotation speed.		2,4,6,8,10,12,13, 15,17,18 ,20,21,23,24,25	1.5 deg	R/W
0x4B	CLKTrim	CLKTrim[5:0] provide 6 bit for precise basic clock output.		35	level	R/W
0x4C	PRT_LVL	Bit[7:4]	Over voltage/temperature protection level(V_{PRTL}) selection, range from 1.0V~2.24V(0x0~0xE), 15 level settings.	0xD	level	R/W
		Bit[3:0]	Over current protection level(OCPL/OCPH) selection, range from 0.16V/0.26V to 0.41V/0.69V, 16 level settings.	0x0		
0x4D	OCPHFiltr [9:0]	Combine with bit[1:0] of sub-address 0x4E, to form 10-bit of deglitch time period for the OCPH signal, range from 0.4us to 0.4ms.		256	clock	R/W
0x4E	OCPLFiltr [5:0]	Bit[7:2]	Deglitch time period for the OCPL signal, range from 0.4us to 25.6us.	8	clock	R/W
		Bit[1:0]	OCPHFiltr[9:8]			
0x4F	UWSel	Bit[7:6]	UPWSel : Upwind startup setting, the motor brake until the speed reach: 0:4Hz, 1:6Hz, 2:8Hz, 3:12Hz, then start up with six-step till the motor in the forward direction.	0		R/W
		Bit[5:0]	Reserved			
0x50	UPWNum	ExptNum add 1 if the low-side braking time exceed UPWNum*0.5 second		20	number	R/W
0x51	MDuty	Bit[7]	Reserved	0	duty	R/W
		Bit[6:0]	MinDuty : The motor is activated until the duty setting exceed MinDuty			
0x52	OVOTSEL/ FWRSW	Bit[7]	FWRSW, direct set PT2511 to 0: forward rotation, 1: reverse rotation in the 28 pin SSOP package, This bit won't work in the 32 pin LQFP package version.	0		R/W
		Bit[4]	OVOTSEL, 1: over temperature selection, 0: over voltage selection.	0		
0x53	FGCTRL	Bit[7:3]	Reserved			R/W
		Bit[2:1]	FGDiv : FG divide setting, 00_b:1, 01_b:2, 10_b:4, 11_b:8	00_b		
		Bit[0]	XOREn : FG XOR enable setting, 0:disable, 1:enable	0_b		

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply voltage range	V_{DD}	5	30	V
I/O voltage	–	-0.3	5	V
Operating temperature range	T_A	-40	+85	°C
Storage temperature range	T_{STG}	-55	+125	°C

ELECTRICAL CHARACTERISTICS

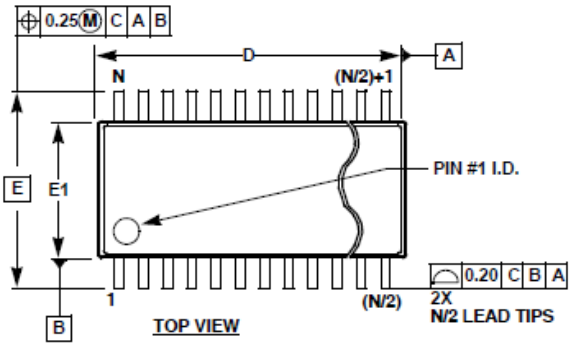
Nominal conditions: V_{DD} =24.0V, GND=0, T_A = +27°C.

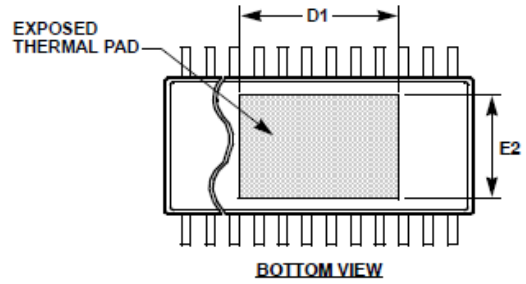
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply voltage	V_{DD}		7	24	28	V
Current consumption	I_{DD}			5	8	mA
Regulator output voltage*	V_{REG}		4.98	5	5.02	V
Regulator output current	I_{REG}	(V_{NOLOAD} - $V\_{LOAD20mA}$)/ V_{NOLOAD} < 5%		20		mA
Parameters Setting						
Low protection voltage**	V_{PRTL}	VSEN pin		2.0		V
High protection voltage	V_{PRTH}	VSEN pin	2.0	2.5		V
Over current protection voltage level low (OCPL, current limit)***	V_{OCPL}	RF pin		0.15		V
Over current protection voltage level high (OCPH, lock protection)	V_{OCPH}	RF pin		0.24		V
External oscillator	F_{OSC_1K}	OSCC= 470pF		1		KHz
External oscillator range	F_{OSC_C}	OSCC pin	0.1	-	10	KHz
Integrated MOSFET						
R_{DSON} series resistance (HS + LS)	R_{DSON}	VDD = 24 V; VG = 28.5 V; Iout = 1 A		0.45		Ω
Swing-head Driver Characteristics						
Voltage drop in full bridge driver		SWO1, SWO2, V_{DD}=15V, I=200mA		1	2	V
Hall Element Amplifier Characteristics						
Common-mode input range	V_{HCM}	Using hall element	+0.5		V_{REG} - 0.5	V
Hall input sensitivity	V_{HSEN}			80		mV
HB output voltage	V_{HB}	I_{HB}= 10mA	4.5			V
I/O Interface						
Logic output high level	V_{OH}	FG, RD	4.0	4.5	5.5	V
Logic output low level	V_{OL}	FG, RD		0	0.3	V
DC for speed control input range	V_{DC}	DC input (VSP pin)	0.5		3.3	V
PWM input high level	V_{PWMH}	PWM input (VSP pin)	3.5			V
PWM input low level	V_{PWML}	PWM input (VSP pin)			0.3	V
PWM input clock	F_{PWM_IN}	PWM input (VSP pin)	15	20	25	KHz
THERMAL SHUTDOWN						
Shutdown temperature	T_{SDN}			155		℃
Hysteresis window	T_{SDN_HYS}			40		℃

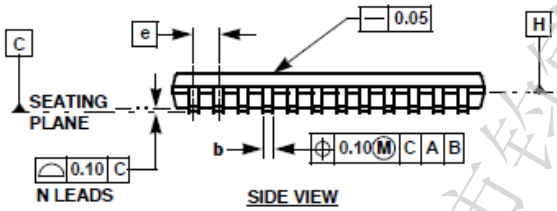
* V_{REG} is adjustable with I^2C interface.
**High and Low protection voltage can be worked as OVP(Over Voltage Protection) trigger voltage, and it is adjustable with I^2C interface
***V_{OCPH}, V_{OCPL} is adjustable with I^2C interface

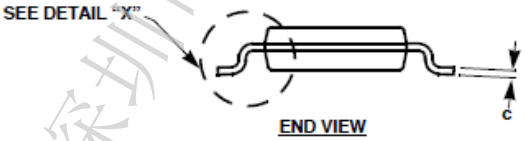
PACKAGE INFORMATION

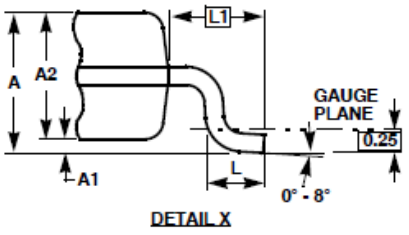
28 Pins, HTSSOP 173MIL











MDP0048

HTSSOP (HEAT-SINK TSSOP) FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	20 LD	24 LD	28 LD	38 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.075	0.075	0.075	0.075	0.075	±0.075
A2	0.90	0.90	0.90	0.90	0.90	+0.15/-0.10
b	0.25	0.25	0.25	0.25	0.22	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	6.50	7.80	9.70	9.70	±0.10
D1	3.2	4.2	4.3	5.0	7.25	Reference
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
E2	3.0	3.0	3.0	3.0	3.0	Reference
e	0.65	0.65	0.65	0.65	0.50	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference
N	14	20	24	28	38	Reference

Rev. 3 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at Datum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Notes :
1. Refer to JEDEC MO-137
2. Unit : mm

IMPORTANT NOTICE

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REVISION HISTORY

Date	Revision	Modification	Author
08/10/2016	PT2501 PRE1.2	1. Add OVP/OTP/OCP description and registers. 2. VOCPL from 0.3 to 0.16, VOCPH from 0.5 to 0.26 3. Add 0x0~0x8 registers description 4. Add I2C diagram and timing as PT2502 5. Update some analog spec	Vincent
08/12/2016	REF 1.0	1. Reference from PT2501 PRE1.2 2. Initial Version of PT21511	Warren